CMOS Analog VLSI Design

Natural

Can you think of a digital signal in the world?

World around you is analog. Sound light Color

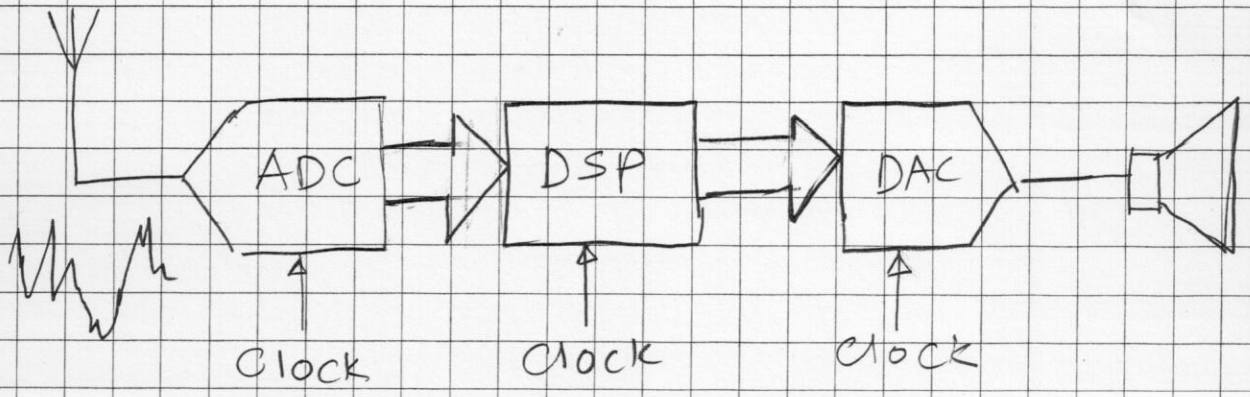
Signal processing in Analog is very difficult.

Digital Signal processing — Bits - Code.

— Repeatable - Reliable.

— Convert to digital as soon as possible

Example



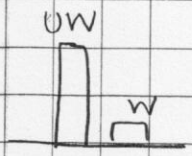
Example — 2.4GHz Wifi

→ At least 10G Clock frequency

→ Huge # of bits Needed to capture Strongest & Weakest signal.

→ Impractical

Analog Design



- Take continuous-time signal (from sensor)
- Remove unwanted signals.
- Sift out only desired signals.
- May be Shift them to lower frequen
- Amplify and condition the signals.
- ADC with lowest sampling rate
  - Save power - area.

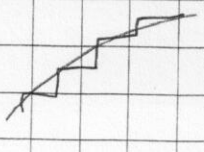
Then DSP takes over

On the other Side

Take digital signal.

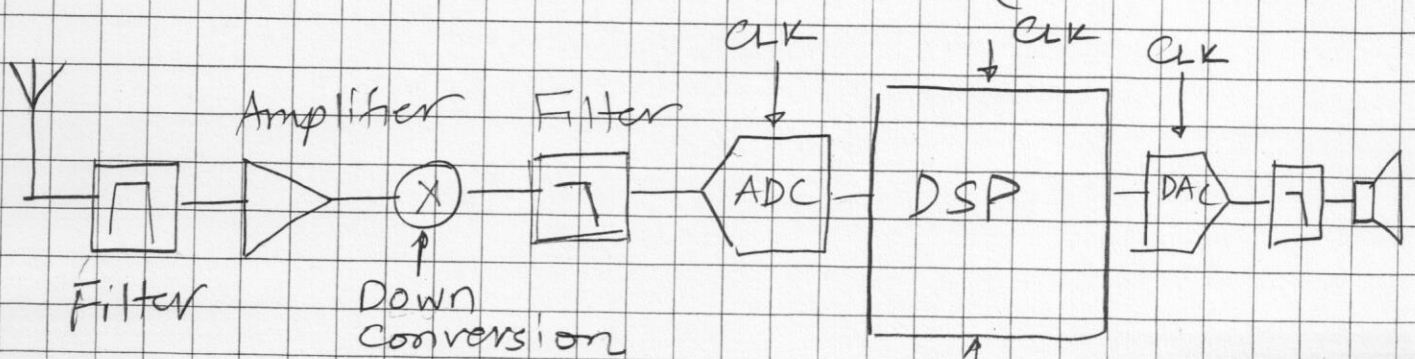
→ Convert to analog

→ Remove digital artifacts.



→ Amplify / condition signal

→ Drive speakers - other devices. (Actuators)

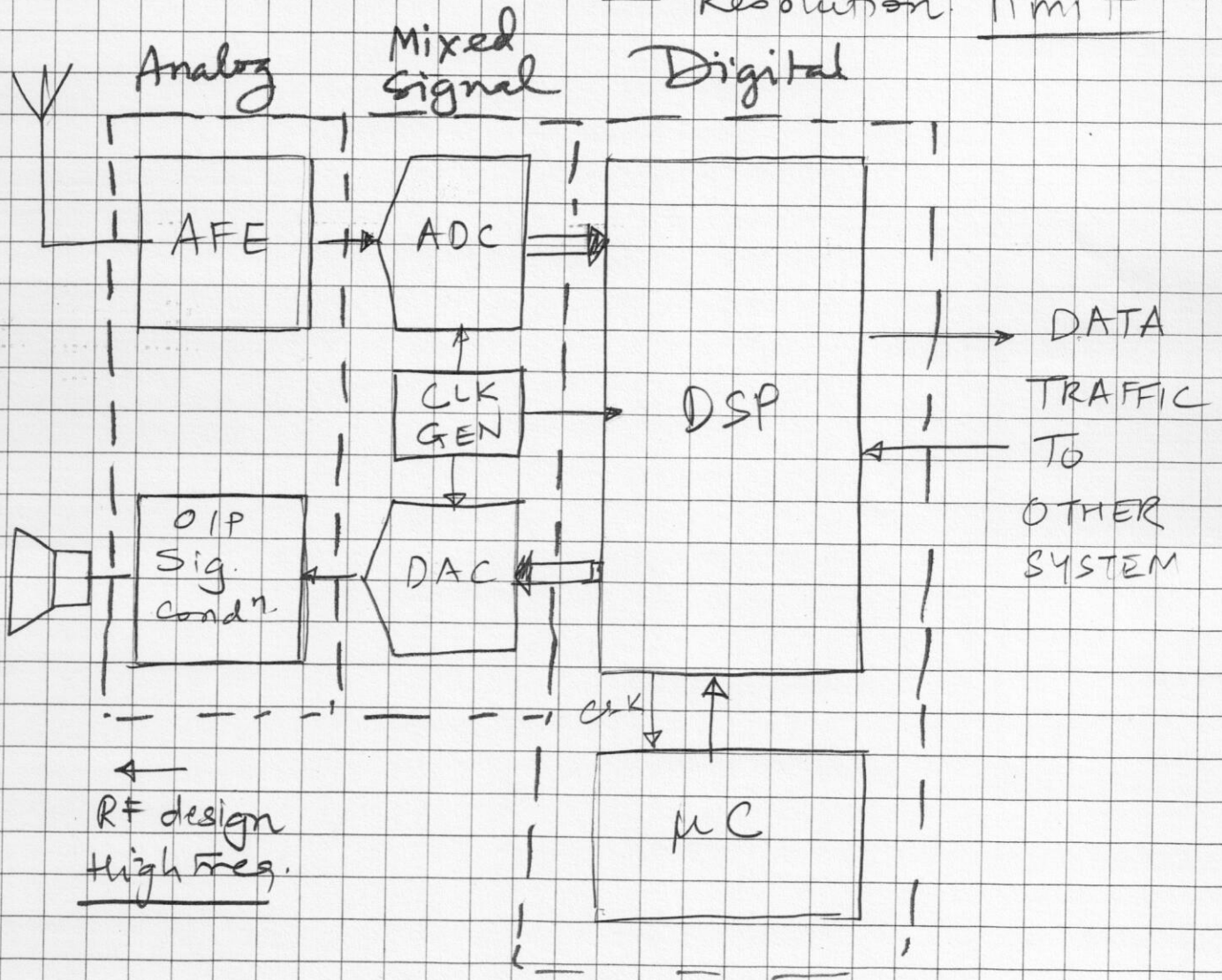


Analog TV example – Gradual Degradation of SNR

Digital TV – Near perfect picture till just it dies.

Analog signal – susceptible to Noise

Digital signal – # of bits you process → Resolution limit



All together System-on-chip.

→ Implications Noise coupling

ANALOG DESIGN CHALLENGES

① Device ← NOISE, LINEARITY → Performance Degradation

② Digital drives → Feature size → (Bad analog beh)
supply voltage downwards.
↳ Analog dynamic range ↓

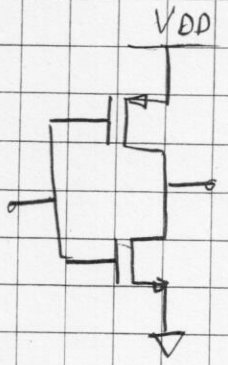
③ Circuit complexity high. to make analog performance independet of
PVT → operating Temperature
process variations
Supply voltage Variation

④ 65nm Technology → 28nm Technology
Digital will scale - Automated to most extent
Analog Handcrafted artwork
→ Redo

Analog-Mixed-Signal - RF designers always in high demand.
— commanding in job prospect
— Experience imp if you are good

CMOS Technology

◎ Show crosssection here



Main Driver → 2 devices for inverter
→ Zero static power
→ scalable (dimensions)
→ minimum # of mask
→ Vdd ↓ lower power
CV^2f

Bipolar - vertical devices - supersmall base width region
└ superfast - HF

$V_{BE} = 0.7V$

$V_{DD} = \sim 2V$ min

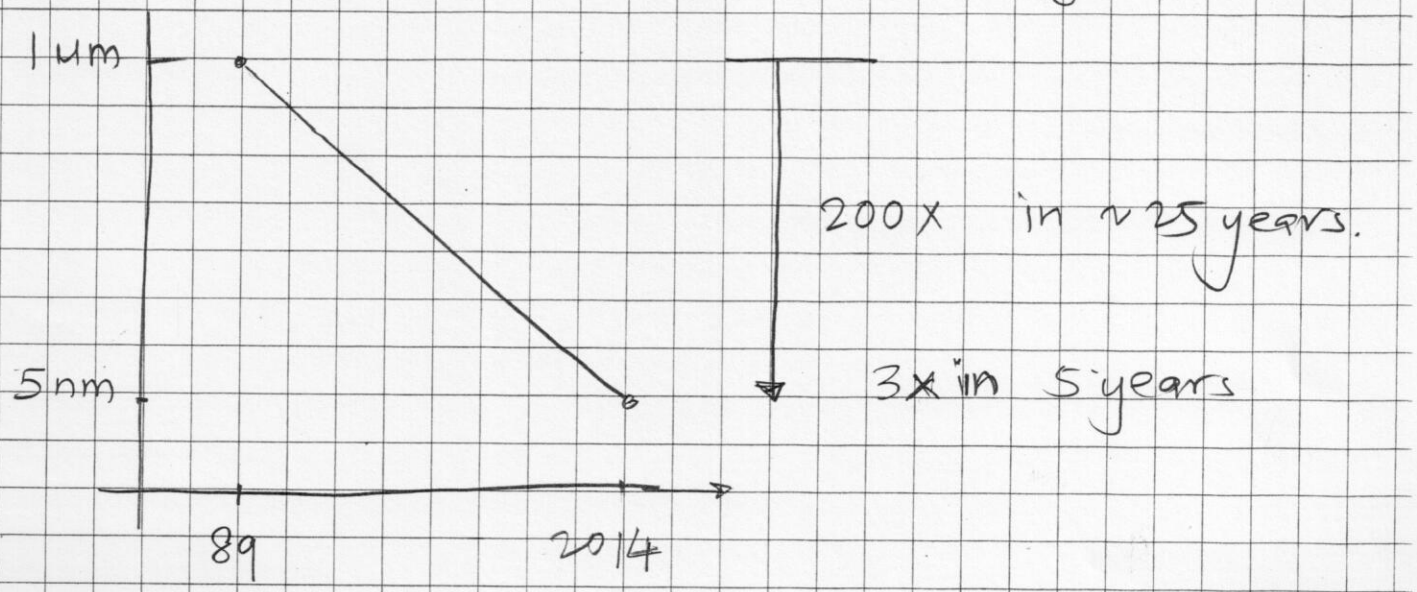
CMOS - action happens laterally - gate length
- slower compared to Bipolar.
- with scaling Lmin 28nm - going down to 5nm
- Speed matches Bipolars. f_T 100GHz +
- analog performance of transistors suffers with scaling
- Digital free - use to compensate analog ckt imperfection.

Vdd ↓ to 1V
↓
lower power designs

Analog + digital integration advantage.

→ Process complexity
→ Models accuracy
→ supply voltage. - challenge to do HV design

CMOS Feature Size → (min Gate length)



As Analog Girl / Guy

→ Creativity must to solve tough problems due to reducing supply voltage & transistor dimensions

→ In SOC (System-on-chip) - Sensitive Analog must co-exist with very Noisy digital.

- Noise insensitive architecture (diff ckts)
- Effect of Substrate / bondwire / magnetic / electrical Coupling
- Effect of Packaging. - must take into account at beginning
- Floorplanning very important

Analog parts - often run on high voltage
→ Device reliability - Important

- Device modeling
- Layout dependent effects.
  - Transistor matching
  - Layout parasitics
  - Electro-migration in metals.

A lot of Neurons

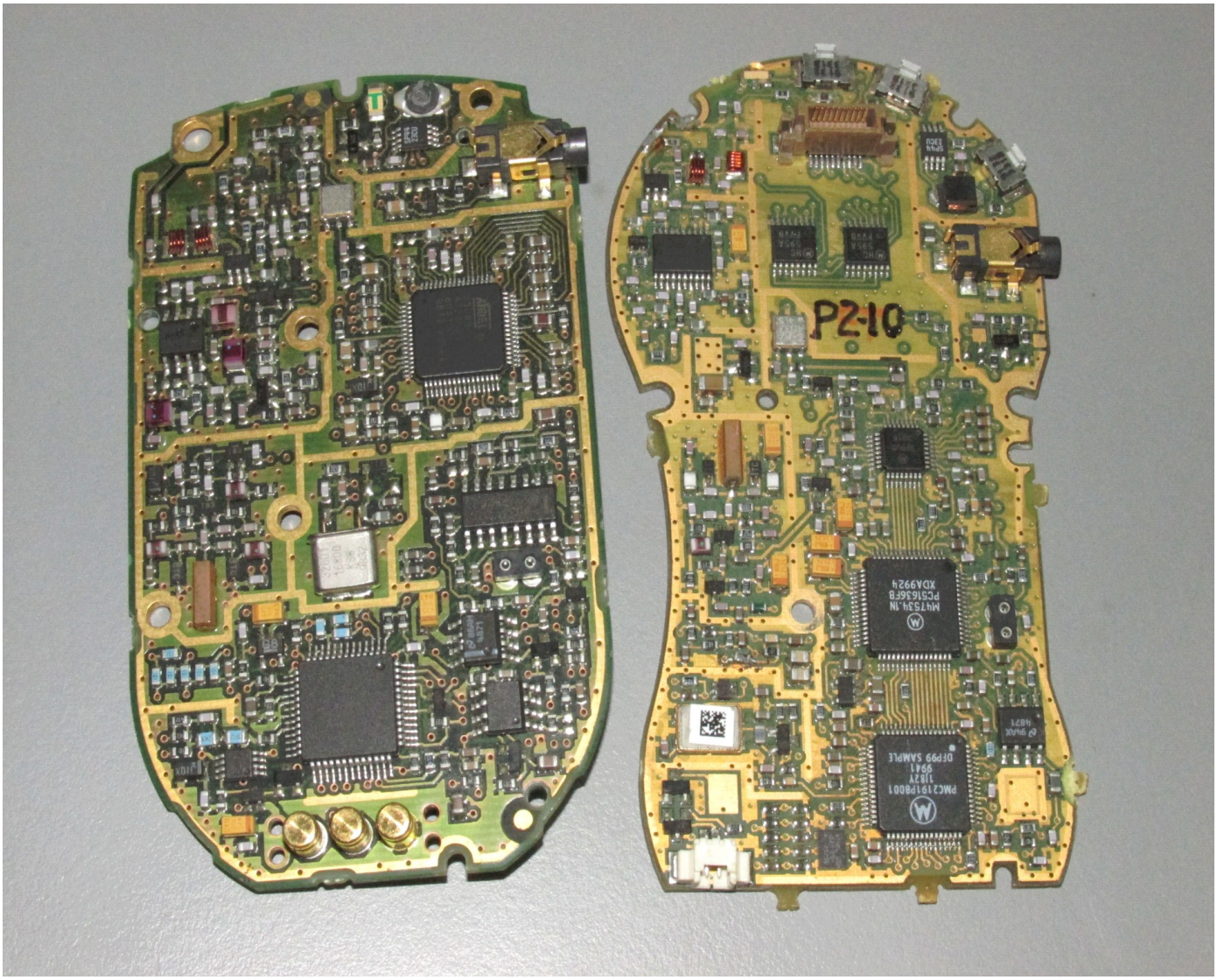
Efforts

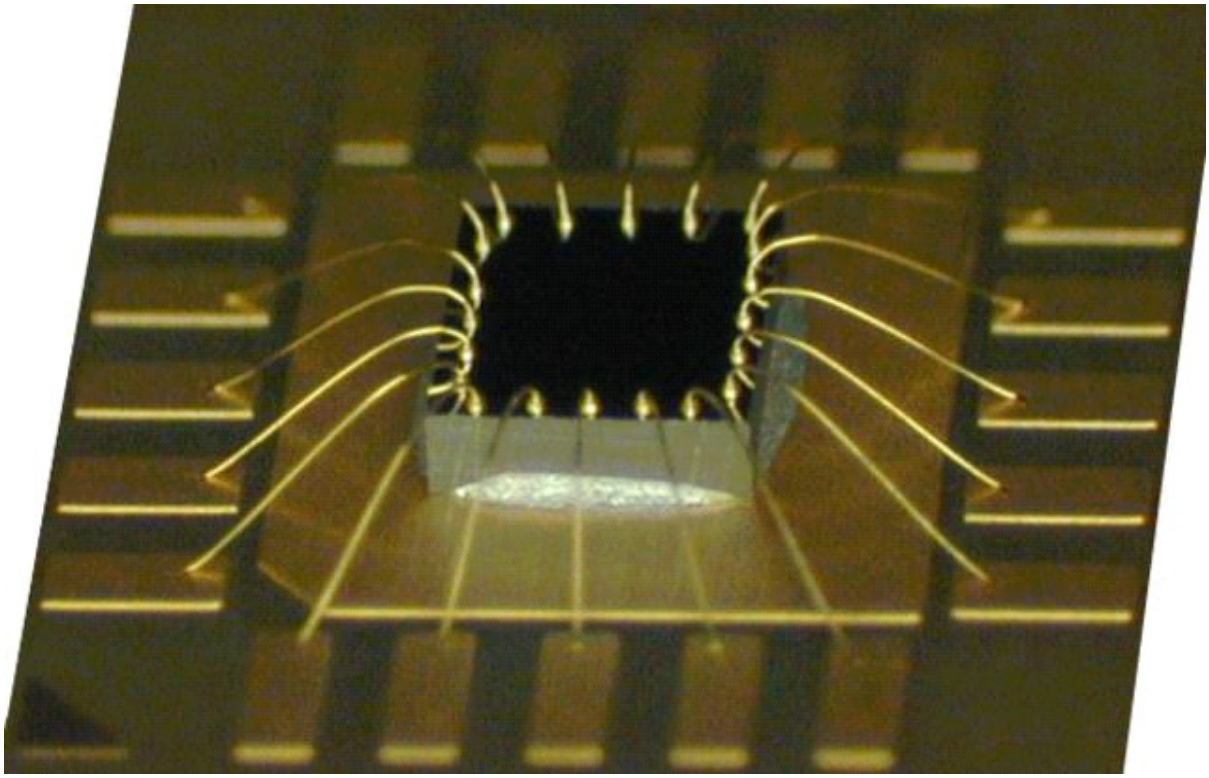
1/3	1/3	1/3
schematic design	Layout effects	Measurement & debug

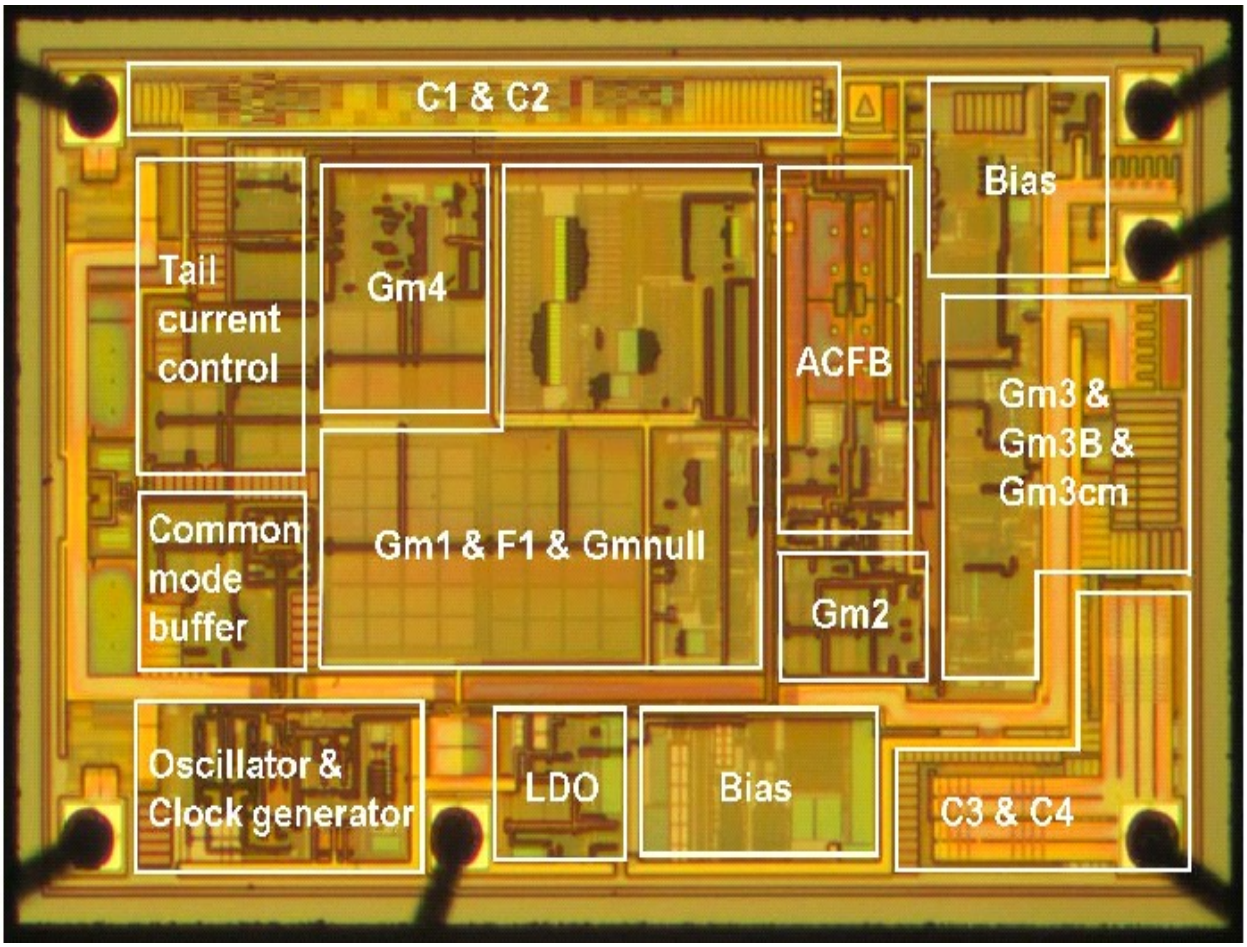
SHOW & TELL

TEXT BOOK

- Design of Analog CMOS ICs
  - B. Razavi (1st or 2nd Edition)
- Various papers for specific topics.


P2-10





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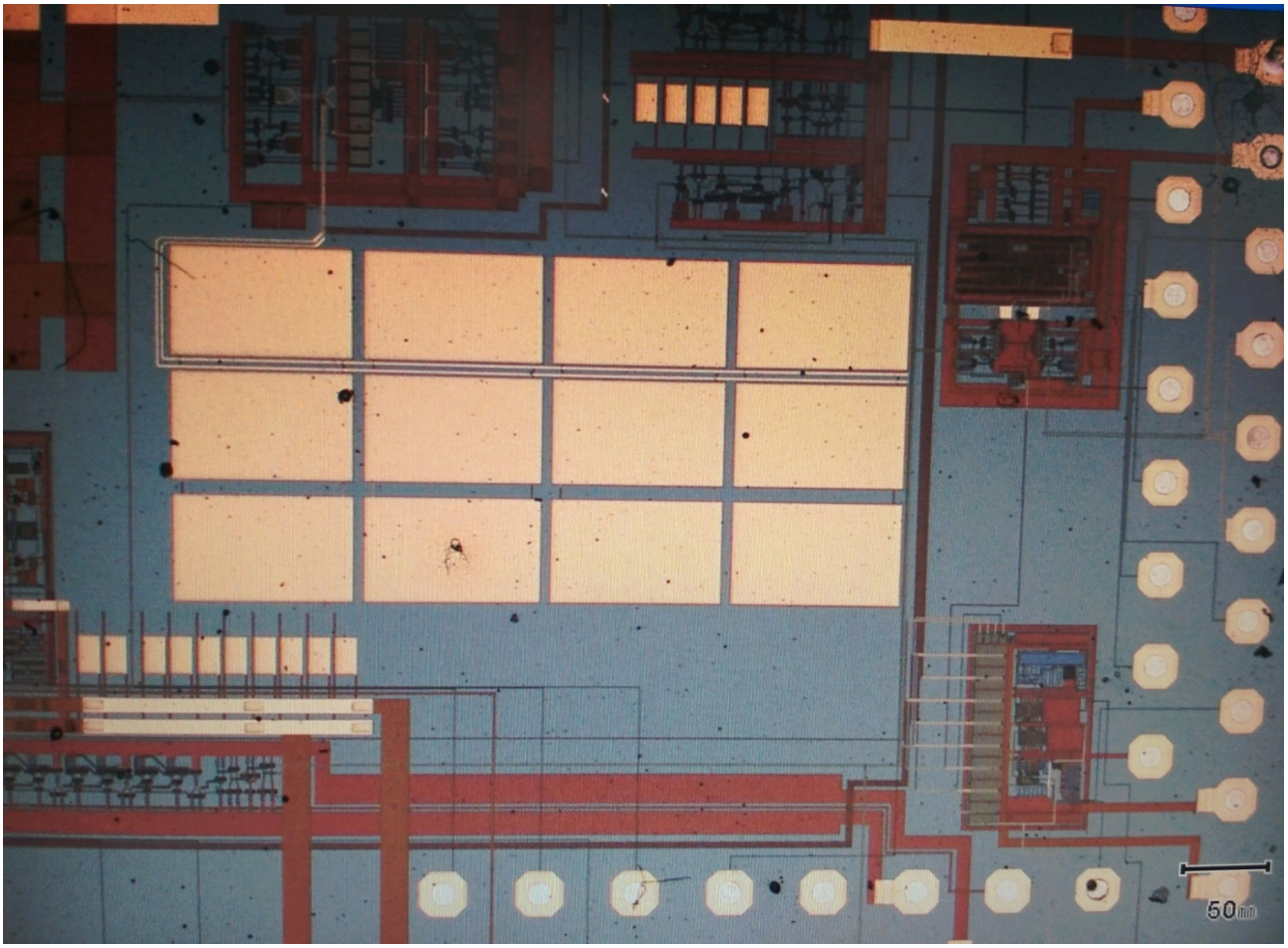
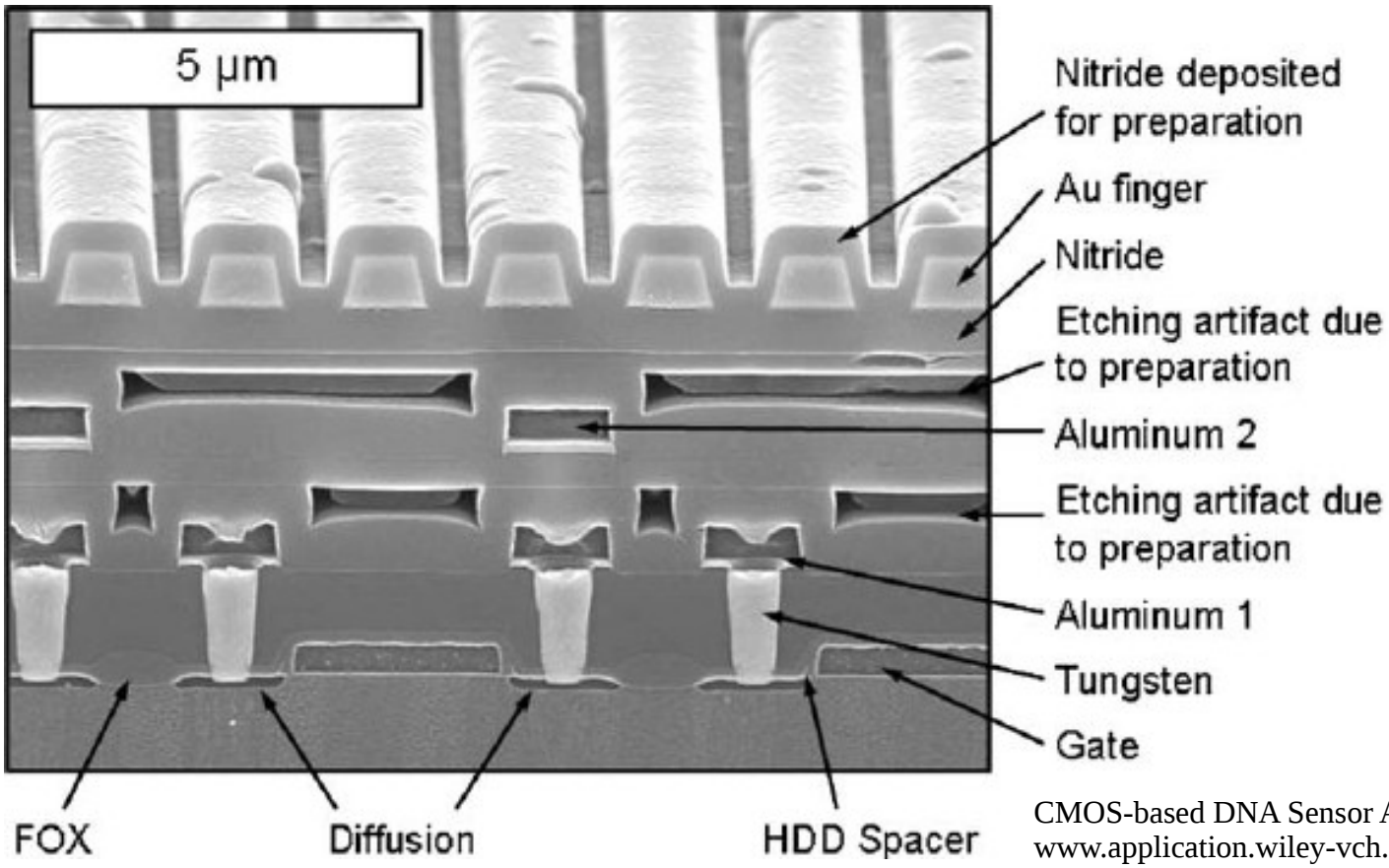
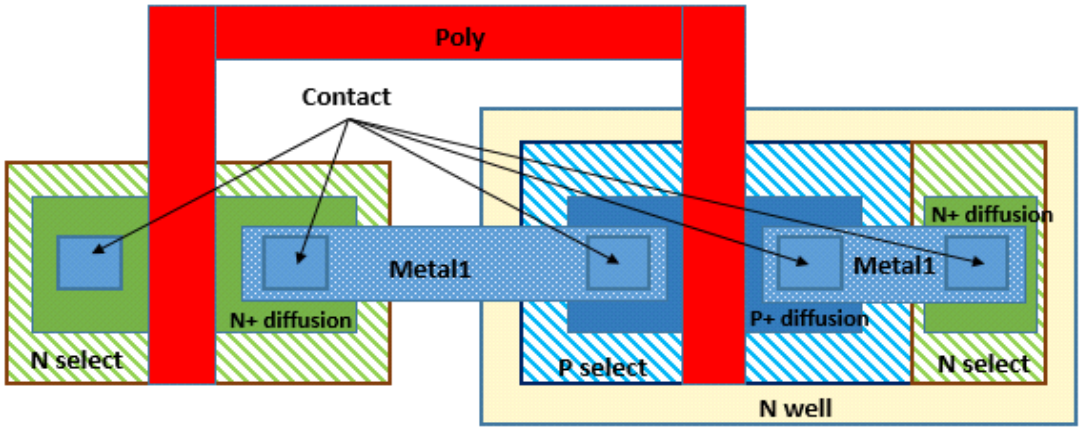


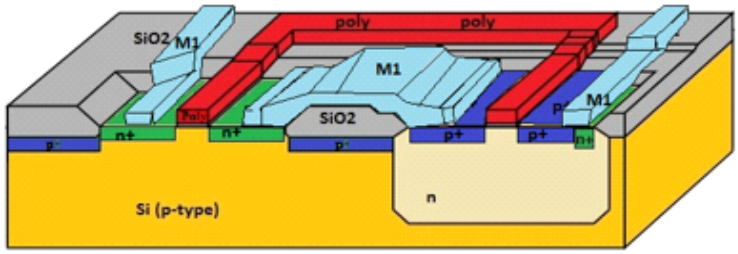


CMOS-based DNA Sensor Arrays
www.application.wiley-vch.de

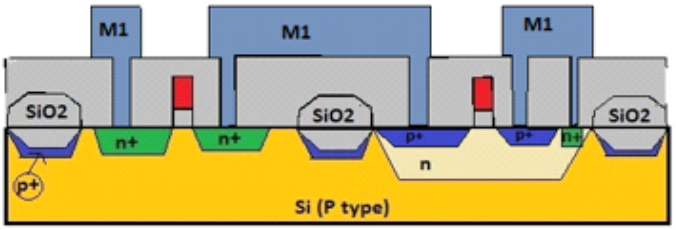
Top View



3D View

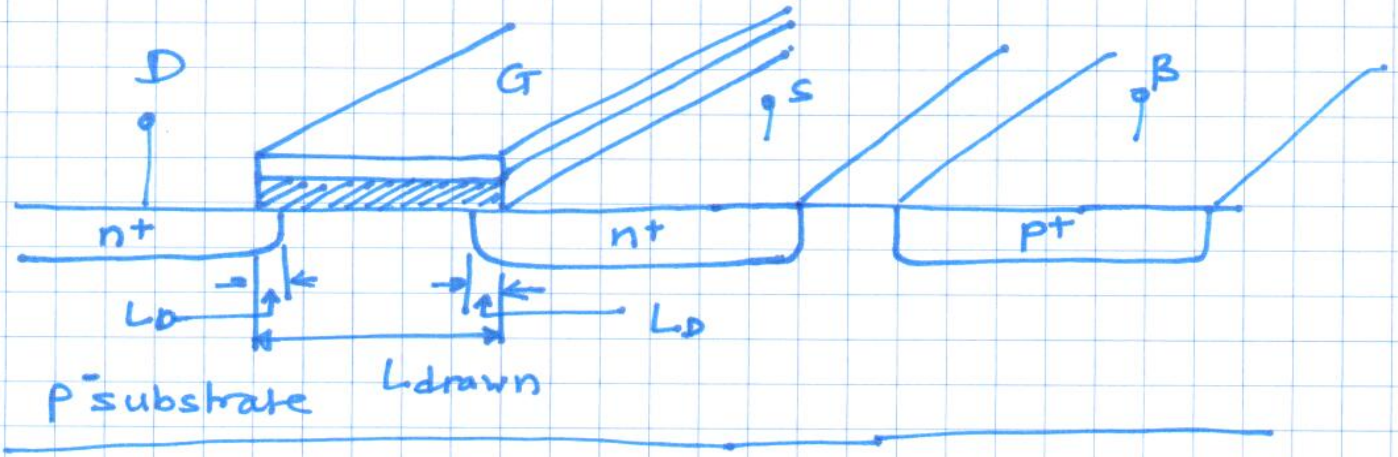


Side View



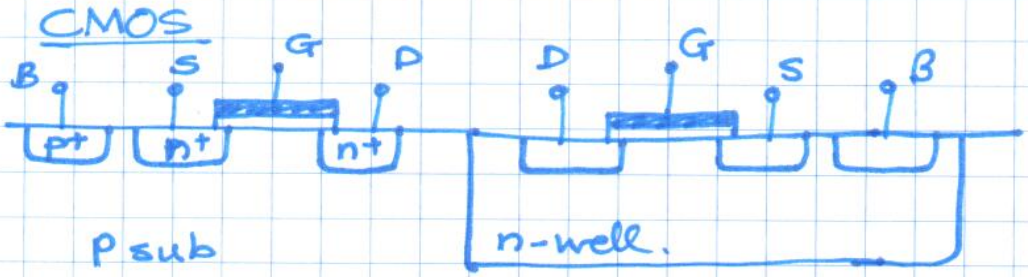
2AUG2019

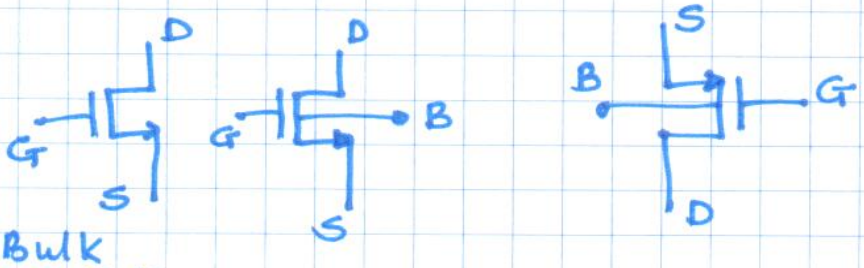
NMOS transistor



* L_D due to side diffusion
* $L_{eff} = L_{drawn} - 2.L_D$.
* S-D interChangable
* S- source of charge carriers
  D - drain - collects charge carriers & removes them.

CMOS





Bulk implicit gnd.

Bulk connection implicit Vdd.

* Why polysilicon instead of Metal for gate

→ Polysilicon – allows transistor gate definition very accurately – self aligned process. → smaller & faster transistor.

→ doping process – high temp

→ poly can withstand high temp. Metal/AL melt

→ V_T reduction ϕ_{ms} ← poly to s work function.

with Metal. – high V_T.

$$\phi_{ms} = \phi_{F_{sub}} - \phi_{F_{gate}}$$

n type poly.

$$= \frac{KT}{q} \ln\left(\frac{n_i}{N_A}\right) - \frac{KT}{q} \ln\left(\frac{N_D}{n_i}\right)$$

N_A – psub

$$= \frac{KT}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right)$$ ← can be changed.

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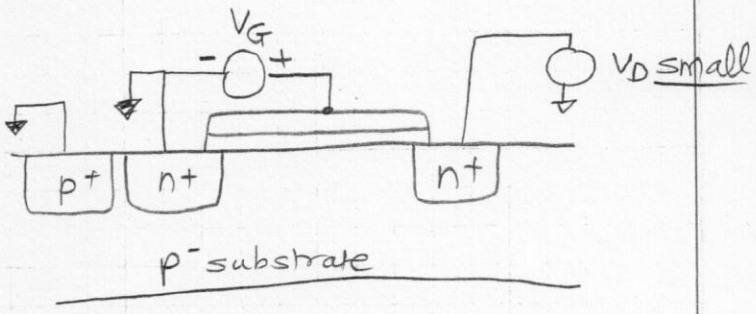
ANALOG CMOS IC DESIGN

MOS DEVICE PHYSICS BASICS

NMOS crosssection



As V_G ↑, holes in p-substrate repelled leaving behind -ve ions. (depletion region). As V_G ↑ further width of depletion region increases. Cap divider effect between gate - oxide interface - substrate. When V_G increases beyond V_{TH} sufficient positive value, e^- flow from source to the interface & drain - channel formed. (Inversion)

V_{TH} - Threshold voltage $= \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}$

Φ_{MS} - work function difference bet^n gate & sub.

Surface potential $\Phi_F = \frac{KT}{q} \ln\left(\frac{N_{sub}}{N_i}\right)$ → doping density; → e^- density in undoped Si

Q_{dep} = Charge in depletion region.

$= \sqrt{4q\epsilon_{si}|\Phi_F|N_{sub}}$

ϵ_{si} ~ dielectric constant

C_{ox} - Gate Oxide cap.

$\epsilon_{si} = 11.68$

$\epsilon_{SiO_2} = 3.97$

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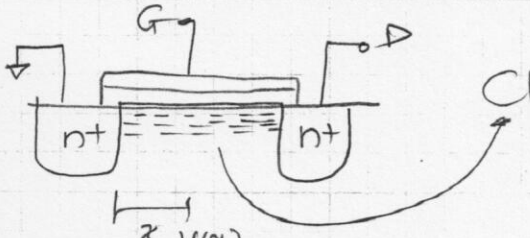
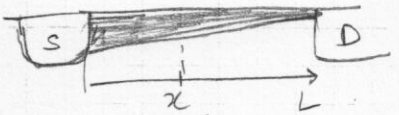


$Q_d = W C_{ox} (V_{GS} - V_{TH})$ @ $V_{GS} = V_{TH}$ Channel Begins to form.

$$Q_d(x) = W C_{ox} [V_{GS} - V(x) - V_{TH}]$$



↑ Channel potential @ position x from source.

$$I_{DS}(x) = -W C_{ox} [V_{GS} - V(x) - V_{TH}] v \leftarrow \text{Charge velocity}$$

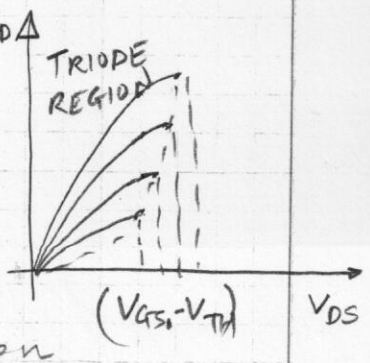
$$= \mu_n E = \mu_n \frac{dV(x)}{dx}$$

$$I_{DS} = W C_{ox} [V_{GS} - V(x) - V_{TH}] \mu_n \frac{dV(x)}{dx}$$

$$\int_0^L I_{DS}\, dx = \int_0^{V_{DS}} \mu_n W C_{ox} [V_{GS} - V(x) - V_{TH}]\, dV(x)$$

$$L \cdot I_{DS} = \mu_n C_{ox} W \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$



TRIODE Region

for $V_{DS} \ll 2(V_{GS} - V_{TH})$

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$$

$$R_{ON} = \left(\frac{\partial I_{DS}}{\partial V_{DS}} \right)^{-1} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_{TH})}$$

Linear Region

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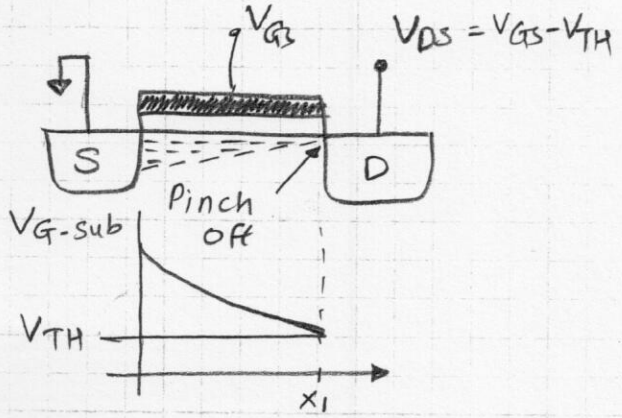
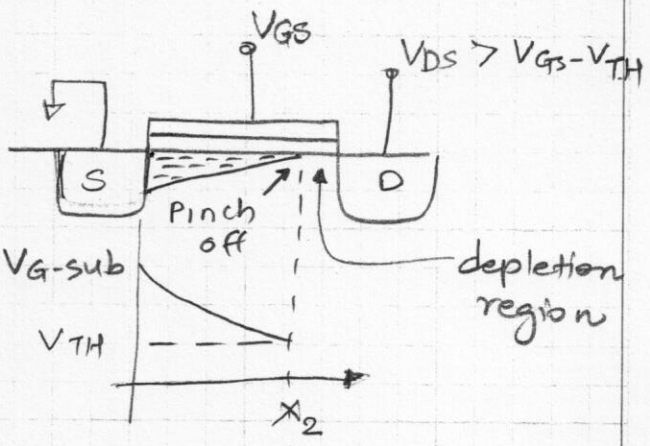
When $V_{DS} > V_{GS} - V_{TH}$





$V(x_1) = V_{GS} - V_{TH}$

Remember $Q_d(x) = W C_{ox} [V_{GS} - V(x) - V_{TH}]$

@ pinch off point $Q_d(x) = 0$ $V(x) = V_{GS} - V_{TH}$

As e^- (carriers) approach pinch-off point, their velocity rises big time. ($v = I/Q_d$) → electrons shoot through the depletion region. & arrive @ drain.

After pinch-off - device is in saturation region.

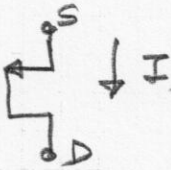
$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L'} (V_{GS} - V_{TH})^2$$

{ integration from $V(x) = 0 \rightarrow (V_{GS} - V_{TH})$

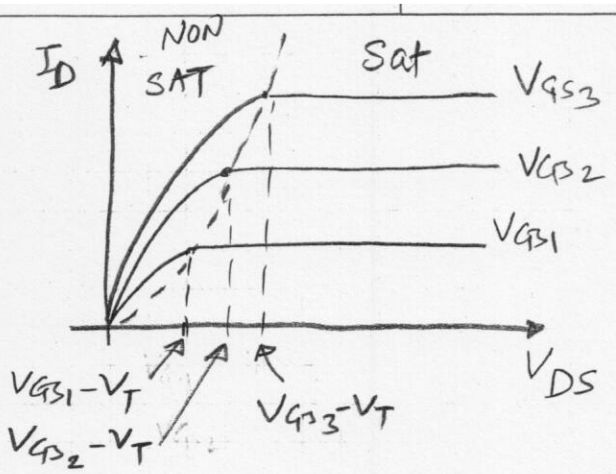
L' where channel pinches off

$V_{GS} - V_{TH}$ ⇒ called V_{dsat}

$V_{DS} > V_{dsat}$ Required for Saturation region op.

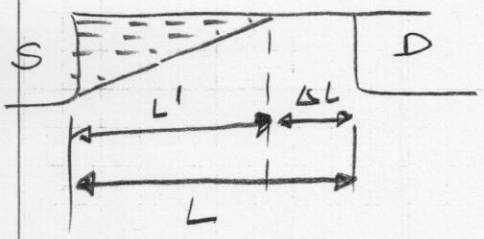
* PMOS devices 

$$I_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L'} (V_{SG} - |V_{THp}|)^2$$



Channel length Modulation

Recall pinch-off in saturation



L' is function of V_{DS}

$$\frac{\Delta L}{L} = \lambda V_{DS} \quad \text{(in saturation)}$$

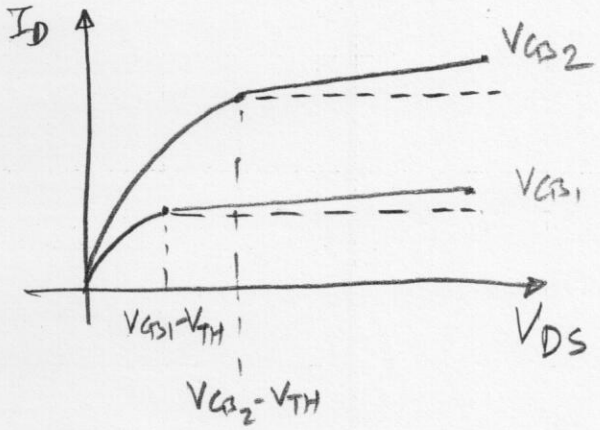
$$\frac{L'}{L} = \frac{L-\Delta L}{L} = (1-\lambda V_{DS})$$

$$\frac{1}{L'} = (1+\lambda V_{DS})\frac{1}{L}$$

$\lambda \rightarrow$ Channel length modulation coeff.

Substituting in sat equation

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$



$$\frac{\Delta L}{L} = \lambda V_{DS}$$

Relative variation in length, due to V_{DS}

Longer L

Smaller λ

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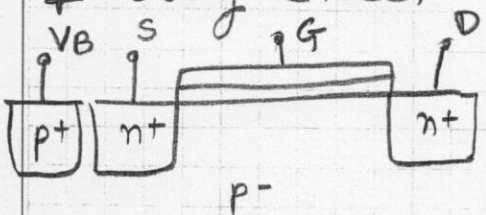
★ Body Effect



Body - backgate acts like another gate affecting channel

$\uparrow V_{SB} \rightarrow \uparrow V_T$

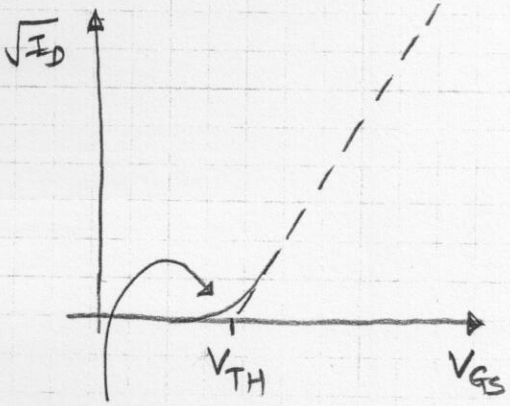
$$V_{TH} = V_{TH_0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right) \qquad \gamma = 2$$

Body Effect Coefficient $\gamma = \dfrac{\sqrt{2q\epsilon_{Si}N_{sub}}}{C_{ox}} \sim 0.3\text{-}0.4\ \sqrt{V}$

$\uparrow V_{BS}$ $\downarrow V_T$ can be used to reduce V_T by forward biasing V_{BS}.

→ make sure current is limited after forward biasing.

★ Subthreshold Conduction.



Subthreshold (weak inversion)

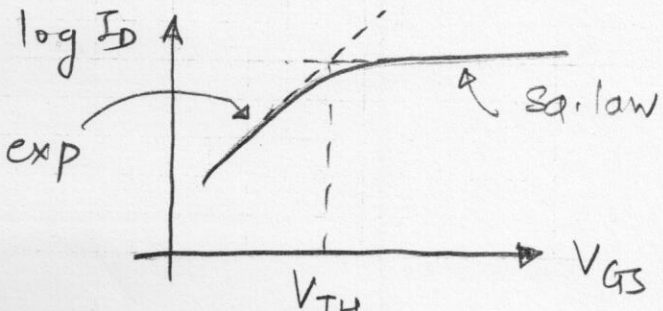
Even for $V_{GS} < V_{TH}$

— finite I_D - exponential dependence on V_{GS}

$$I_D = I_0 \exp\frac{V_{GS}}{\xi V_T}$$

$\xi > 1$; $V_T = \dfrac{kT}{q}$

Similar to $I_C - V_{BE}$ of bipolar transistor



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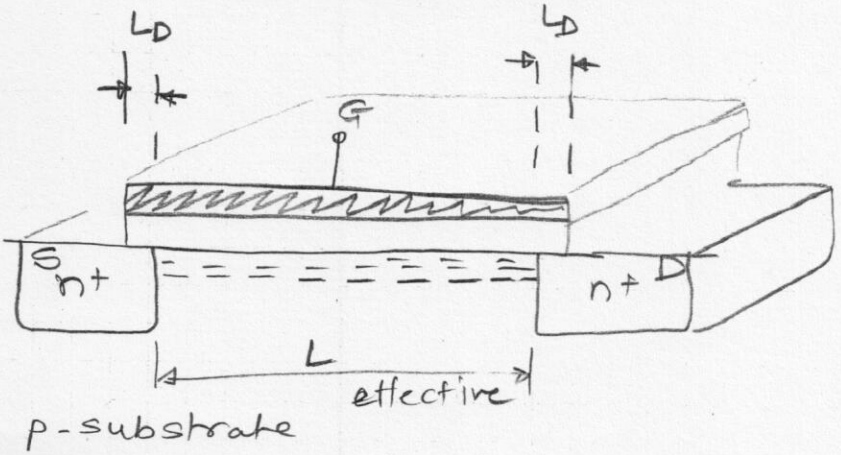
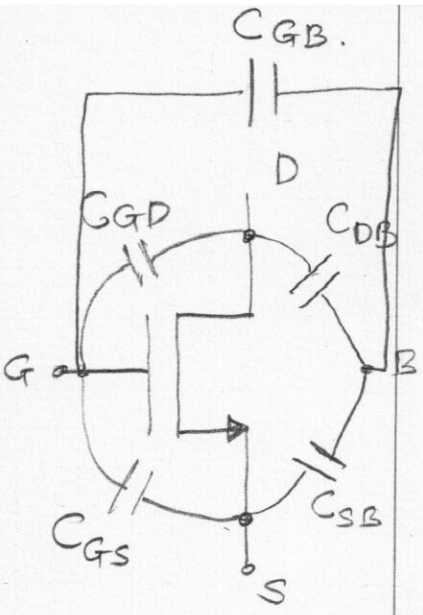
MOS device Capacitances





Device is off

$C_{GD} = C_{GS} = C_{ov} \cdot W$ ($C_{ov} = L_D \cdot C_{ox}$)

$C_{GB} = C_{ox} WL$ series with C_d ← depletion sub. cap. $= WL\sqrt{q\epsilon_{si}\frac{N_{sub}}{\phi_F}}$

Device is in triode region — $WL\,C_{ox}$ equally divided both gate & source/drain term.

$$C_{GD} = C_{GS} = \frac{WL\,C_{ox}}{2} + W\,C_{ov}$$

($C_{ov} = L_D \cdot C_{ox}$)

$C_{GB} = 0$

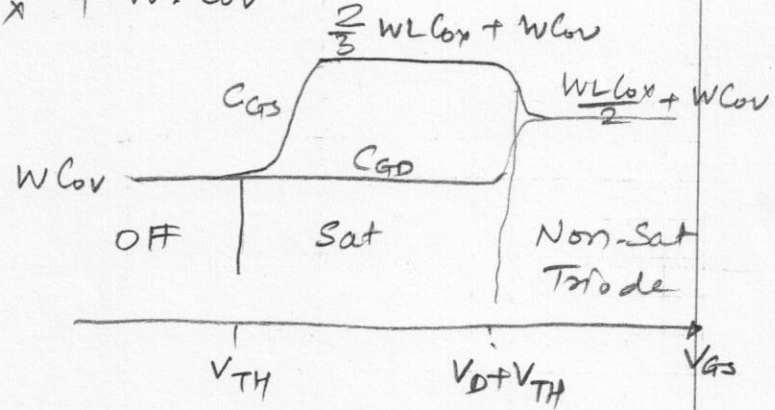
Device is in saturation region — pinch off channel

$C_{GD} = C_{ov} \cdot W$

$C_{GS} = \frac{2}{3} WL\,C_{ox} + W \cdot C_{ov}$ ($C_{ov} = L_D \cdot C_{ox}$)

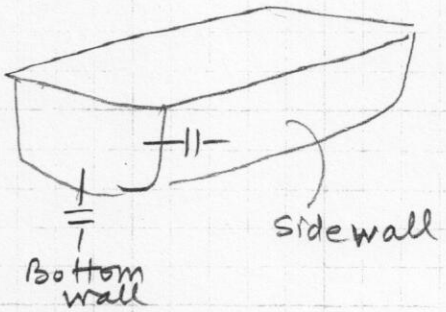
Muller Kamins proof ←

$C_{GB} \approx 0$



Drain / source → bulk cap.

$$C_{DB} = \underbrace{\frac{C_J \cdot A_D}{\left(1 + \frac{V_{DB}}{P_B}\right)^{MJ}}}_{\text{Bottomwall}} + \underbrace{\frac{C_{JSW} \cdot P_D}{\left(1 + \frac{V_{DB}}{P_B}\right)^{MJSW}}}_{\text{Sidewall}}$$



$$C_{SB} = \frac{C_J \cdot A_S}{\left(1 + \frac{V_{SB}}{P_B}\right)^{MJ}} + \frac{C_{JSW} \cdot P_S}{\left(1 + \frac{V_{SB}}{P_B}\right)^{MJSW}}$$

C_J → source/drain bottomplate j^n cap/area F/m²

C_{JSW} → sidewall F/m

P_B → source/drain junction built-in potential V

MJ, MJSW → exponents (unitless) 0.3 to 0.4

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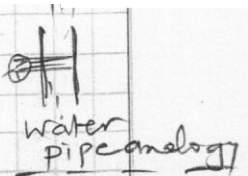
MOS small-signal MODEL in saturation

✱ Transconductance $g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}\text{ constant sat}}$



$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

V_{dsat}

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \cong \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})$$

$$g_m = \frac{2I_D}{(V_{GS}-V_{TH})} \quad \boxed{\text{EXACT}}$$

$$g_m \cong \sqrt{2\mu_n C_{ox}\frac{W}{L}\cdot I_D}$$

IMP. to commit to memory g_m transconductance

Insight Bipolar transistor $I_C = I_0 \cdot \exp\left(\frac{V_{BE}}{V_T}\right)$

Bipolar $g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{V_T} \leftarrow 26\,mV$ $\quad \boxed{V_T = \frac{kT}{q}}$

Compare with MOS $g_m = \frac{I_D}{(V_{GS}-V_{TH})/2} = \frac{I_D}{100\,mV}$

$V_{dsat} \longrightarrow (V_{GS}-V_{TH})/2 \sim 200\,mV$

Bipolar g_m is 4x higher than MOS g_m for same current.

✱ Backgate transconductance

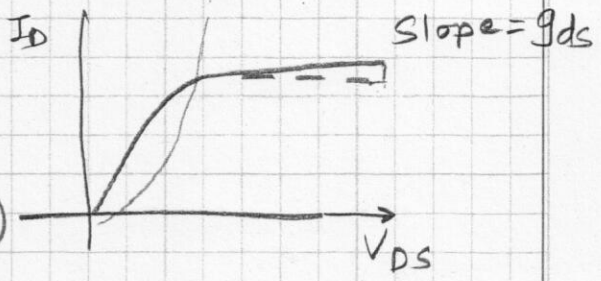
$$g_{mbs} = \frac{\partial I_D}{\partial V_{BS}} = \frac{\partial I_D}{\partial V_{TH}}\cdot\frac{\partial V_{TH}}{\partial V_{BS}} = \frac{\gamma}{2\sqrt{V_{SB}+2\phi_F}}\cdot g_m$$

$\frac{\partial I_D}{\partial V_{TH}} = -g_m$

$$= \eta\, g_m \quad (\eta \approx 0.25)$$

$$V_{TH} = V_{TH_0} + \gamma\left(\sqrt{V_{SB}+2\phi_F} - \sqrt{2\phi_F}\right)$$

Output conductance g_{ds}



$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

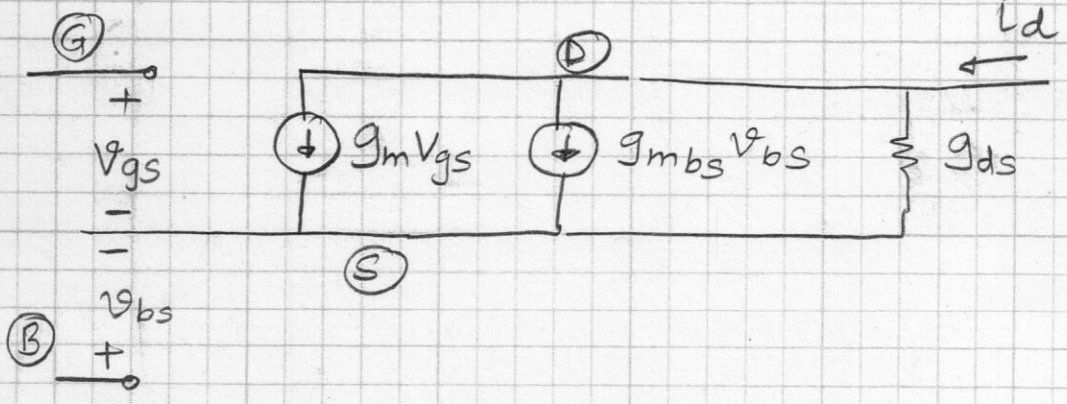
$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{TH})^2 \cdot \lambda = \frac{\lambda I_D}{(1+\lambda V_{DS})}$$

$$g_{ds} \simeq \lambda I_D \quad (\text{since } \lambda V_{DS} \ll 1)$$

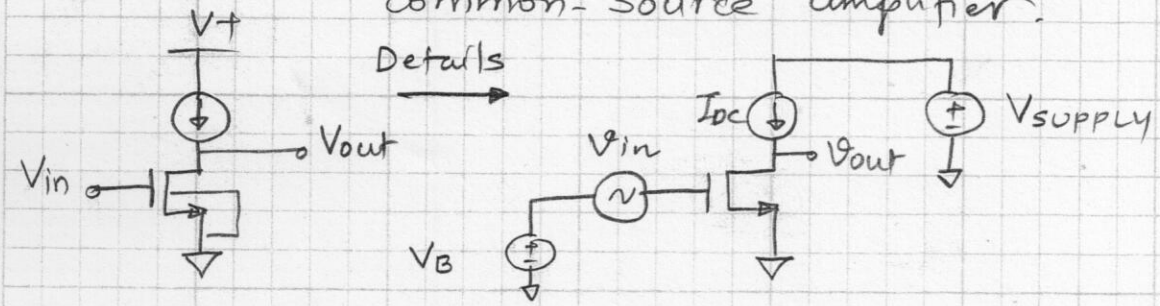
$$r_{ds} = \frac{1}{g_{ds}} = \frac{1}{\lambda I_D}$$

small signal parameter

MOS DC Small Signal Model. (low frequency)



Example - small-signal L.F voltage gain for common-source amplifier.



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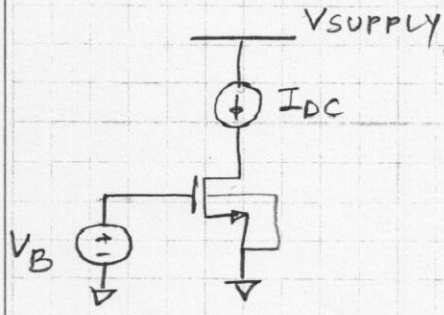
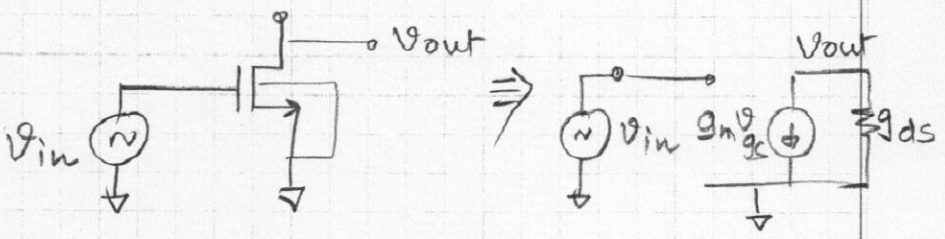
DC circuit



AC circuit



$$v_{out} = -g_m v_{in} \cdot \frac{1}{g_{ds}}$$

open ckt gain

self gain

$$\text{gain} \quad a_v = \frac{v_{out}}{v_{in}} = -\frac{g_m}{g_{ds}}$$

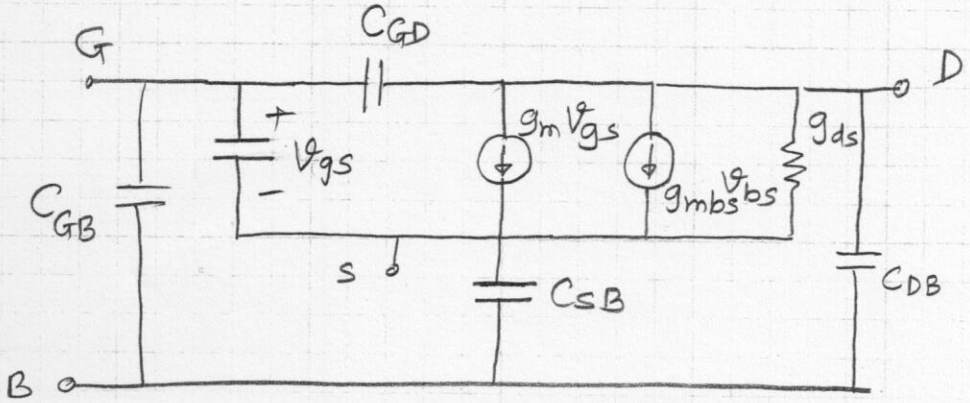
$$a_v = -\frac{g_m}{g_{ds}} = \frac{-\sqrt{2\mu_n C_{ox}(W/L) I_D}}{\lambda I_D} \propto \frac{1}{\sqrt{I_D}}$$

$$= -\frac{g_m}{g_{ds}} = \frac{2 I_D/(V_{GS}-V_{TH})}{\lambda I_D} = \frac{2}{\lambda (V_{GS}-V_T)}$$

insight large channel length → small λ → high gain

small $(V_{GS}-V_{TH})$ → higher gain

High frequency small-signal Model



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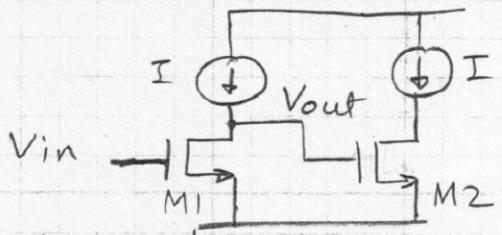
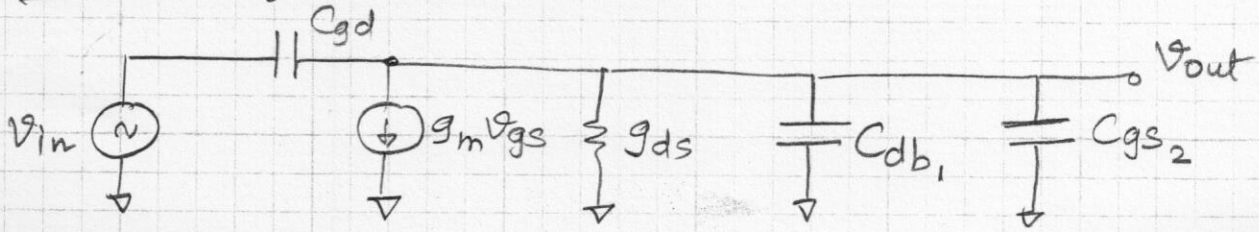
Speed of CMOS



C_{gs_1}, C_{gb_1} – ignore – source driven

g_{mbs}, C_{sb} – ignore. (No backgate effect)

Small Signal model.



KCL @ Vout

$$sC_{gd}(V_{in} - v_{out}) = g_m v_{in} + g_{ds} v_{out} + s(C_{gs} + C_{db}) v_{out}$$

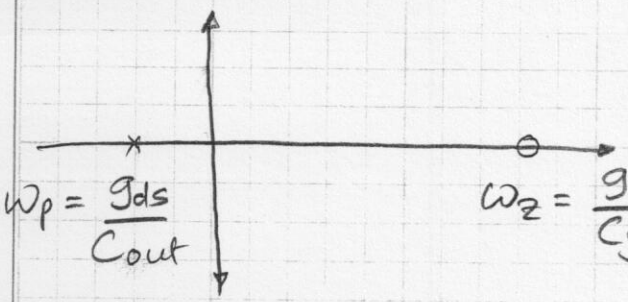
$$-(g_m - sC_{gd}) v_{in} = v_{out}\left[g_{ds} + s(C_{gs} + C_{db} + C_{gd}) \right]$$

$$A_V(s) = \frac{v_{out}}{v_{in}} = -\boxed{\frac{g_m}{g_{ds}}} \frac{\left(1 - s\frac{C_{gd}}{g_m}\right)}{\left(1 + s\frac{(C_{gs} + C_{gd} + C_{db})}{g_{ds}}\right)}$$

← RHP zero

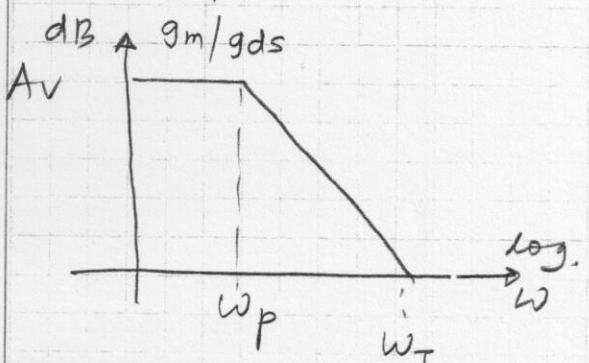
DC gain

$C_{out} = C_{gs} + C_{gd} + C_{db}$ ← LHP pole



Assume $\omega_z >> \omega_p$

& $C_{gs} >> C_{db} + C_{gd}$.



$$A_V(s) = -\frac{g_m}{g_{ds}} \frac{1}{\left(1 + s\frac{C_{gs}}{g_{ds}}\right)}$$

Transition frequency ω_T.

ω_T = gain ; BW product.

$$\omega_T = \frac{g_m}{g_{ds}} \cdot \frac{g_{ds}}{C_{gs}} = \frac{g_m}{C_{gs}} \text{ (rad/s.)}$$

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$$\omega_T = \frac{g_m}{C_{gs}} = \frac{\mu_n C_{ox}(W/L)\cdot(V_{GS}-V_{TH})}{\frac{2}{3} C_{ox}\cdot(W\cdot L)} \qquad V_{dsat}$$

$$= \frac{3}{2}\cdot\frac{\mu_n (V_{GS}-V_{TH})}{L^2}$$

Example: $\mu_n = 350\ cm^2/V/s$

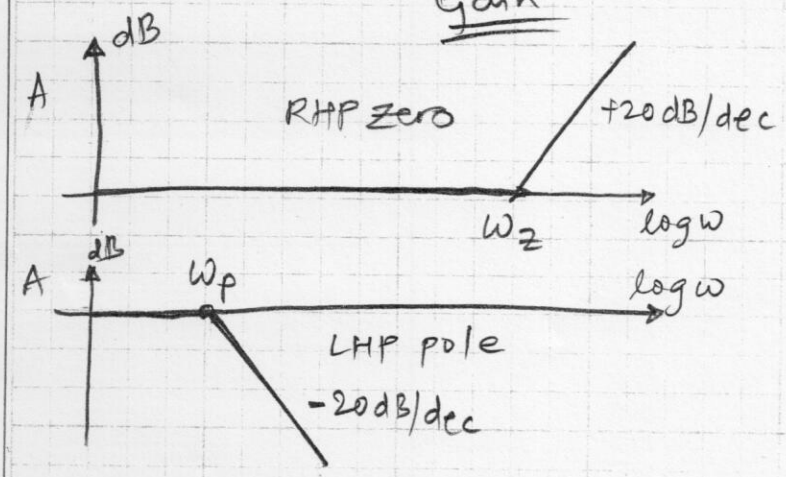
$V_{GS}-V_{TH} = 200\,mV$

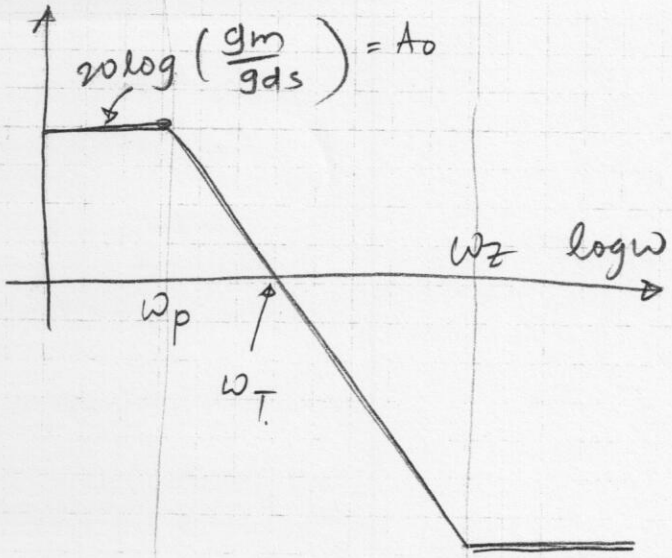
$L = 100nm.$

$$f_T = \frac{3}{2}\cdot\frac{350\times 0.2}{2\times\pi\times(100\times 10^{-7})^2} = 167.1\ GHz.$$

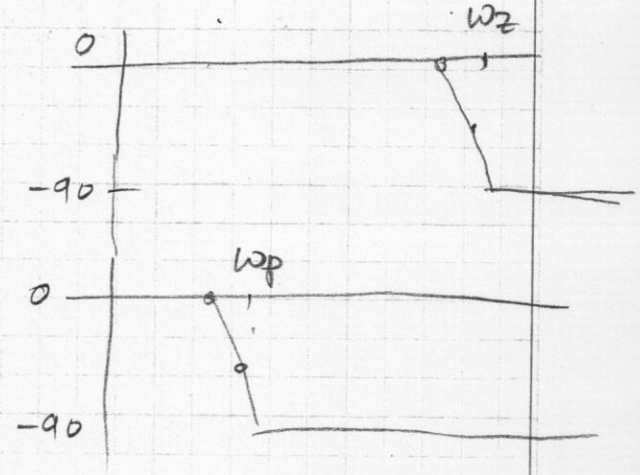
Bode Plot

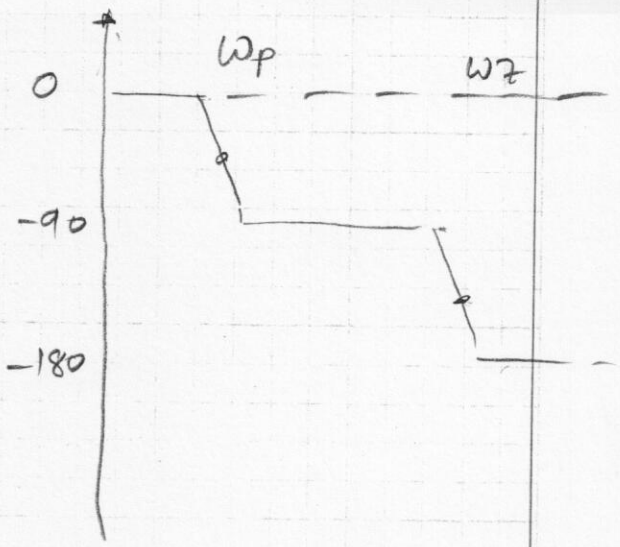
Gain





Phase





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Example values for all transistor parameters

Example process $L_{min} = 0.5\mu m$

	NMOS	PMOS
VTO (V) Threshold voltage	+0.5	−0.6
GAMMA (body Effect coef $V^{-1/2}$)	0.45	0.4
TOX (A)	90	90
UO (mobility $cm^2/V/s$)	350	100
LAMBDA (λ - ch. length modulation Coef V^{-1})	0.1	0.2
PHI ($2\phi_F$) V	0.9	0.8

$$C_{ox} = \frac{\epsilon_{ox}\epsilon_0}{t_{ox}} = \frac{3.97 \times 8.85 \times 10^{-12}\ (F/m)}{(90 \times 10^{-10})\ m} = 3.9 \times 10^{-3}\ F/m^2$$

$$= 3.9\ fF/\mu m^2$$

$$\lambda_n = \frac{0.1\ V^{-1} \times 0.5\mu m}{L_n} = \frac{0.05}{L_n}\ V^{-1} \leftarrow L_n \text{ in } \mu m$$

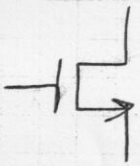
$$\lambda_p = \frac{0.2 \times 0.5}{L_p} = \frac{0.1}{L_p}\ V^{-1} \leftarrow L_p \text{ in } \mu m$$

$$\mu_n C_{ox} = 350\ cm^2/V/s \times 3.9\ fF/\mu m^2$$

$$= 350 \times 10^{-4} \times 3.9 \times \frac{10^{-15}}{10^{-12}}\ A/V^2 = 136.5\ \mu A/V^2$$

$$\mu_p C_{ox} = 39\ \mu A/V^2$$

Example



$$g_m = \sqrt{2 \cdot \mu_n C_{ox} \frac{W}{L} \cdot I_D}$$

$$= \sqrt{2 \times 136.5 \times 10^{-6} \times \frac{10}{0.5} \times 100 \times 10^{-6}}$$

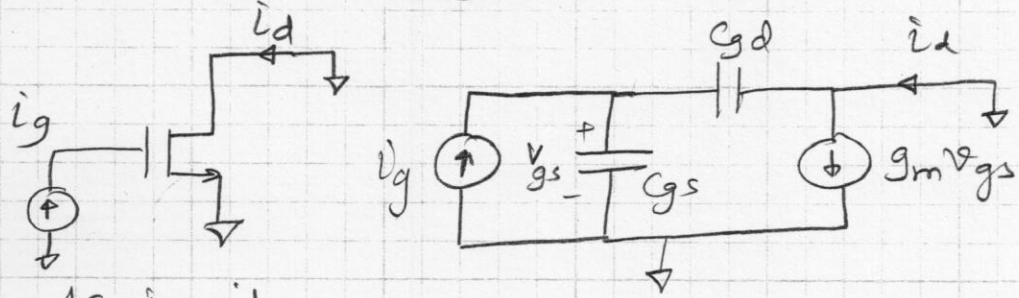
$$= 738\ \frac{\mu A}{V} = 738\ \mu S$$

$$g_{ds} = \lambda_n I_{DS} = 0.1 \times 100 \times 10^{-6} = 10\ \mu S$$

Engineer's Computation Pad

High Frequency Figure of Merit

f_T - Transition Frequency – frequency @ which current gain is unity.



AC circuit

$$i_g = s(C_{gs}+C_{gd})\,v_{gs} \Rightarrow v_{gs} = \frac{i_g}{s(C_{gs}+C_{gd})}$$

$$i_d = g_m v_{gs} = \frac{g_m\, i_g}{s(C_{gs}+C_{gd})}$$ { ignore C_{gd} contribⁿ to o/p current

For f_T (ω_T) $\left|\frac{i_d}{i_g}\right| = \frac{g_m}{\omega_T(C_{gd}+C_{gs})} = 1$

$$\omega_T = \frac{g_m}{(C_{gs}+C_{gd})} \approx \frac{g_m}{C_{gs}}$$ { $C_{gs} \gg C_{gd}$ for long-ch devices

$$f_T = \frac{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})}{2\pi\cdot\frac{2}{3}C_{ox}\,W\cdot L} = \frac{3}{4}\frac{\mu_n (V_{GS}-V_{TH})}{\pi L^2}$$

$f_T \propto (V_{GS}-V_{TH})$ $\quad v_{dsat}$

$f_T \propto \frac{1}{L^2}$ $\quad f_T$ improves with process. $L \downarrow \Rightarrow f_T \uparrow\uparrow$

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{gs}} = \frac{\sqrt{2\mu_n C_{ox}\frac{W}{L} I_D}}{2\pi\frac{2}{3}C_{ox}\cdot W\cdot L} = \frac{1}{2\pi}\frac{3}{\sqrt{2}}\sqrt{\frac{\mu_n}{C_{ox}L^2}\left(\frac{I_D}{W}\right)}$$

($\frac{I_D}{W}$: current density)

f_T improves with current density

EE618 (Zele)

Body Effect and Sub-threshold Conduction

Body Effect

Consider the simplified NMOS shown in Fig. 1 part (A). A voltage V_{GS} is applied between gate and source whereas a voltage V_{SB} is applied between the source and bulk of the NMOS. For this explanation, we consider that the bulk is a p-well so that we can separately bias it (NMOS in a chip may lie in substrate and substrate of the whole chip will be tied to ground). We consider the following two cases -

CASE 1: $V_{GS} = V_{TH}$ **and** $V_{SB} = 0$ **V**

As shown in Fig. 1 part (B), Due to positive V_{GS} the holes in the channel region move out leaving negatively charged ions behind. The electrons that form the inversion layer comes from the n+(very high concentration) source region. The current in the device will be due to drift of these electrons when a V_{DS} is applied.

CASE 2: $V_{GS} = V_{TH}$ **and** V_{SB} **>0 V**
In this case we are increasing V_{SB} (can be achieved by decreasing the bulk voltage keeping source voltage constant). Due to a net positive voltage on the source as compared to the bulk, some of the electrons present in the channel will be attracted back in the source as shown in of Fig. 1 part (C). Hence to achieve the same charge density as in CASE1 we need a more positive charge on the gate. Therefore we can say that increasing V_{SB} increases threshold voltage.

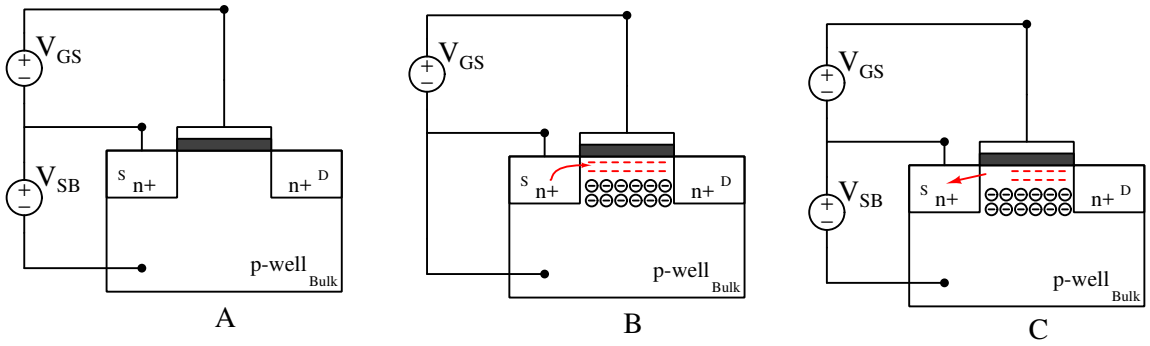


Figure 1: Body effect in MSOFETS

Effect of V_{DS} in Subthreshold Region

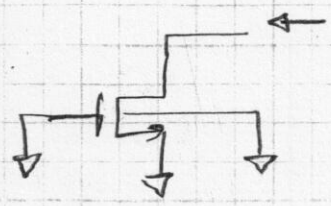
- The region where V_{GS} of the device is less than or close to V_{TH} is known as sub-threshold region.
- Due to diffusion of minority charge carrier electrons, some leakage current may flow in the device even when V_{GS} is less than V_{TH}.
- For a constant V_{DS}, the current equation in subthereshold region is given as

$$\mathrm{I}_{subth} = I_O \times \ exp(\tfrac{V_{GS}}{\zeta V_T}) \times (1 - exp(\tfrac{-V_{DS}}{V_T}))$$

  where ζ is a non-ideality factor greater than 1 and V_T = KT/q
- For $V_{DS} = 0$, the current $I_{subth} = 0$.
- For V_{DS} >$4V_{TH}$ or $5V_{TH}$ the equation reduces to

$$\mathrm{I}_{subth} = I_O \times \ exp(\tfrac{V_{GS}}{\zeta V_T})$$

Small Signal Mos terminal impedances

① 

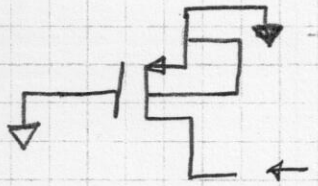
$g = g_{ds}$

$C = C_{gd} + C_{db}$

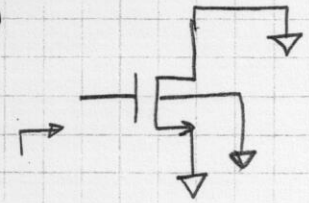
High impedance

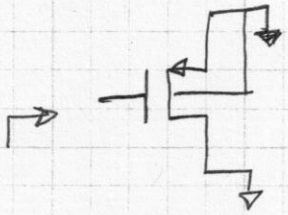
⏚ ← ac ground

DC proper biasing to keep transistor in sat.



Looking into drain

② 

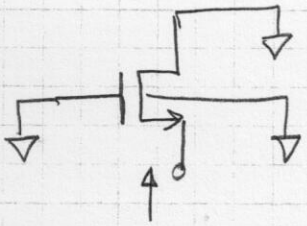


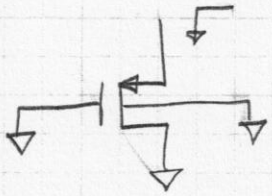
LOOKING into Gate

$g = 0$

$C = C_{gs} + C_{gd}$.

— High Impedance —

③ 



Looking into Source.

$g = g_m + g_{mbs} + g_{ds}$

$C = C_{gs} + C_{sb}$

Low impedance.

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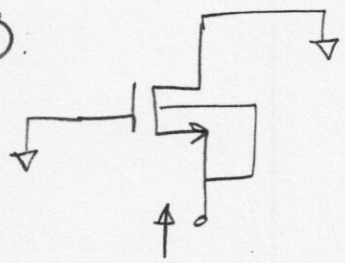
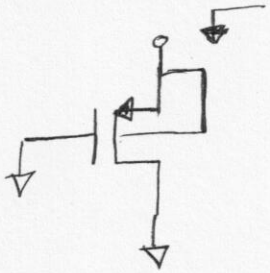
Engineer's Computation Pad

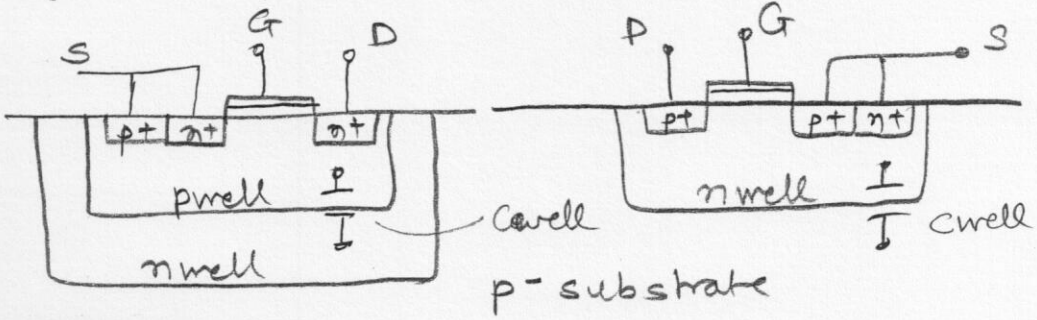
④



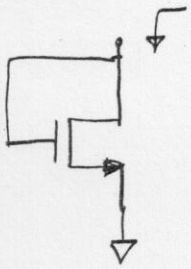


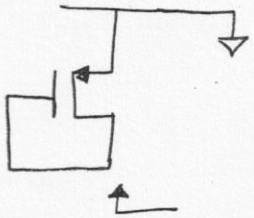
Looking into source (self biased well)

$g = g_m + g_{ds}$ $\quad C = C_{gs} + C_{gb} + C_{db} + C_{well}$



⑤





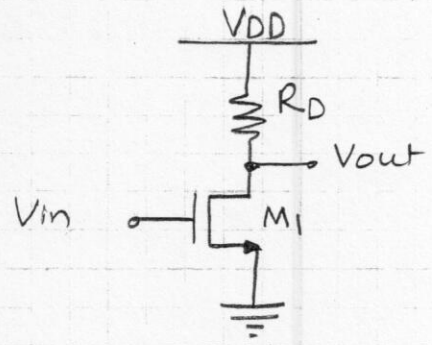
$g = g_m + g_{ds}$ $\quad C = C_{gs} + C_{db}$

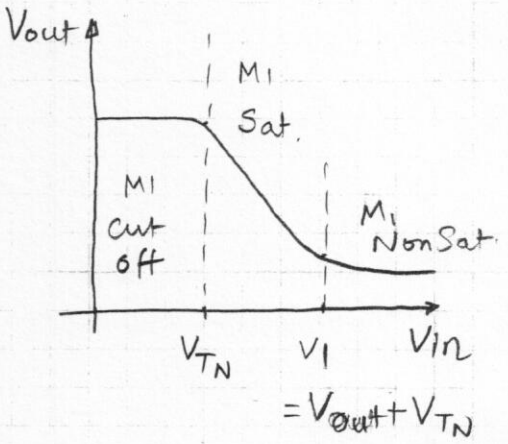
Called <u>diode connected</u> device.

STAEDTLER® NO. 937 01 IE Engineer's Computation Pad

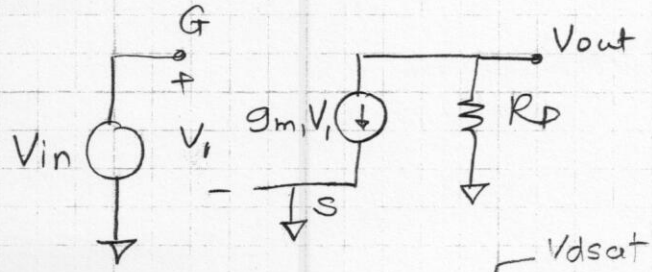
Amplifiers

1. Common-Source amplifier





Small Signal Model in sat. region (ignoring r_o)



$$V_{out} = \underbrace{-g_{m1} R_D}_{A_V \text{ voltage gain}} V_{in}$$

V_{dsat}

$$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)(V_{GS} - V_{TN}) = \frac{2 I_D}{(V_{GS} - V_{TN})} = \sqrt{2 \mu_n C_{ox} \left(\frac{W}{L}\right) I_D}$$

Small Signal Quantity

I_D, V_{GS} = Bias values

key observation

If i/p signal is large $(V_{GS} - V_{TN})$ & hence g_m & hence gain of the circuit changes a lot.

Gain varies with signal swing.

$\Rightarrow$ Distortion

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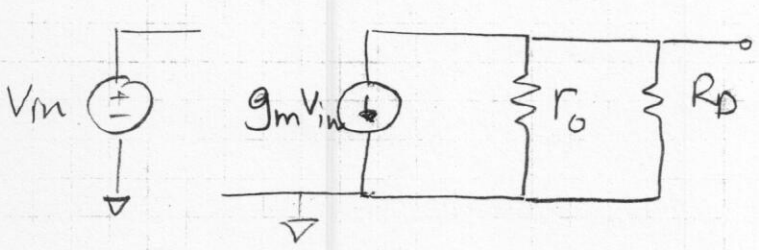
Including Channel length modulation (r_o) effect_



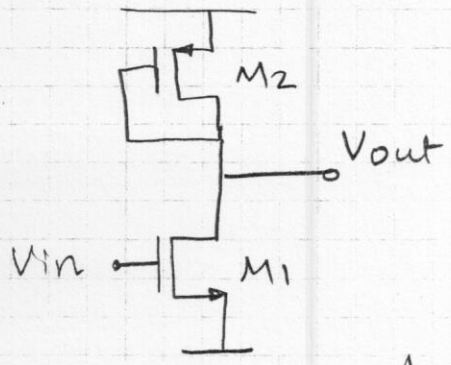
$$A_V = \frac{V_{out}}{V_{in}} = -g_m \frac{r_o R_D}{r_o + R_D}$$

$$A_V = -g_m \cdot (r_o \parallel R_D) = -\frac{g_{m(driver)}}{g_{out\uparrow} + g_{out\downarrow}}$$

g_m ↑ Driver g_m ; $(r_o \parallel R_D)$ Effective output impedance

CS Amp with diode load

①



By inspection

$$A_v = -\frac{g_{m(driver)}}{g_{out\uparrow} + g_{out\downarrow}}$$

$$A_v = -\frac{g_{m1}}{g_{m_2} + g_{ds_2} + g_{ds_1}}$$

$$\approx -\frac{g_{m1}}{g_{m2}} = -\frac{\sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_N I_D}}{\sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_p I_D}}$$

$$\approx -\sqrt{\frac{\mu_n \left(\frac{W}{L}\right)_N}{\mu_p \left(\frac{W}{L}\right)_p}}$$

→ Low voltage gain ~ 2 - 6

→ Low o/p swing $V_{omin} = V_{DSAT1}$ (0.25 V)

$$V_{OMax} = V_{DD} - |V_{GSp}| = V_{DD} - (|V_{Tp}| - |V_{DSAT_2}|)$$

$1.2V - 0.6 - 0.25V = (0.35V)$

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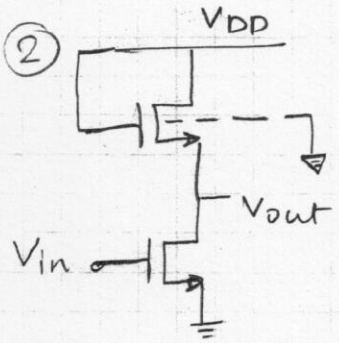
② 

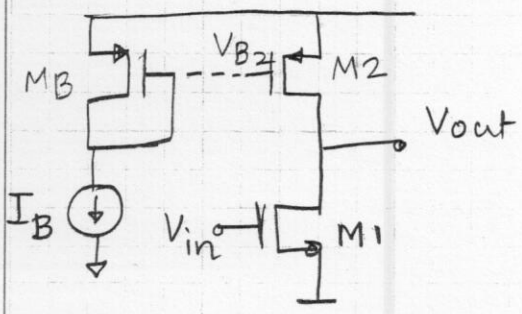
$$A_V = \frac{-g_m(\text{driver})}{g_{out\uparrow} + g_{out\downarrow}}$$

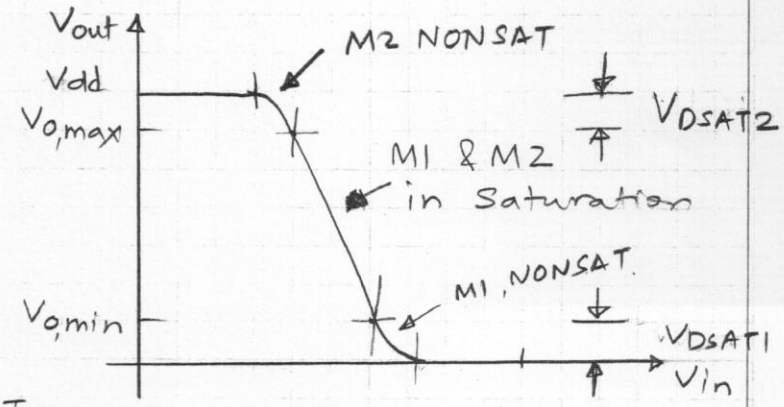
$$A_V = \frac{-g_{m1}}{g_{m2} + g_{mbs2} + \underbrace{g_{ds2} + g_{ds1}}_{\text{ignore}}}$$

$$A_V = -\frac{g_{m1}}{g_{m2} + \underbrace{g_{mbs2}}_{\text{body effect } 0.25\cdot g_{m2}}} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \cdot \frac{1}{1+\eta}$$

Low gain & Low swing.

C-S Amplifier with current source load.





$$(W/L)_B = (W/L)_2 \Rightarrow I_1 = I_2 = I_B$$

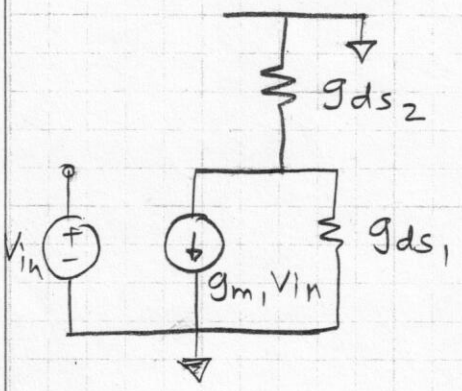
$$V_{B2} = V_{DD} - (|V_{Tp}| + V_{DSAT2})$$

$$V_{B1} = V_{TN} + V_{DSAT1}$$

$$V_{DSAT1} = \sqrt{\frac{2I_B}{\mu_n C_{ox} (W/L)_1}}$$

$$V_{DSAT2} = \sqrt{\frac{2I_B}{\mu_p C_{ox} (W/L)_2}}$$

When Both M1 & M2 are in saturation
— small signal analysis



$$A_V = -\frac{g_{m_1}}{g_{ds_1} + g_{ds_2}}$$

$$= -\frac{2I_B/(V_{GS}-V_T)_N}{\lambda_N I_B + \lambda_p I_B}$$

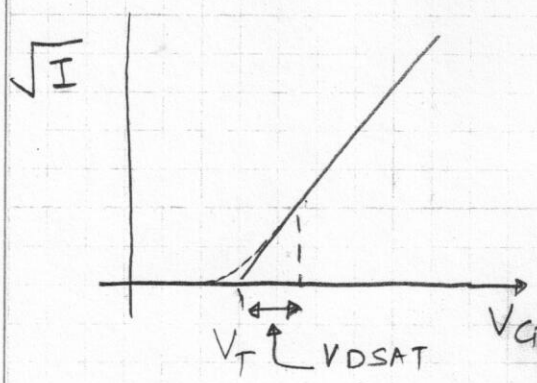
$$= -\frac{2}{V_{DSAT_1}(\lambda_N + \lambda_p)}$$

Insight To increase gain, reduce V_{DSAT_1} & increase channel length to reduce λ_N, λ_p

★ Can you keep on reducing V_{DSAT} & ↑ gain?

$$V_{DSAT_1} = V_{GS}-V_T = \sqrt{\frac{2I}{\mu C_{ox}\left(\frac{W}{L}\right)}}$$

{ for given I, as you ↑ W/L, V_{DSAT} ↓



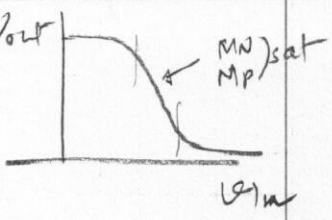
$$I = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_T)^2$$

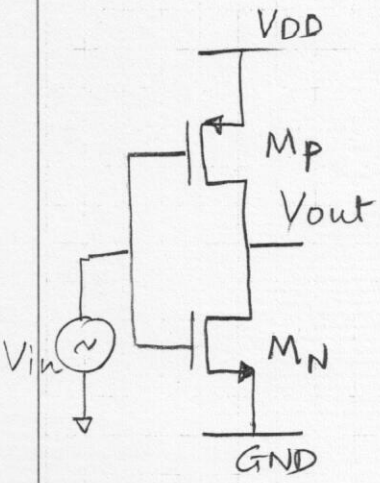
As you keep on reducing $V_{DSAT} = (V_{GS}-V_T)$, V_{GS} very close to V_T

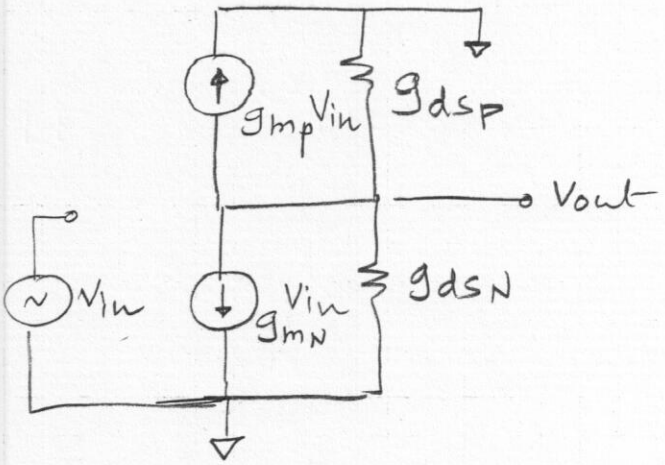
→ sub-threshold operation

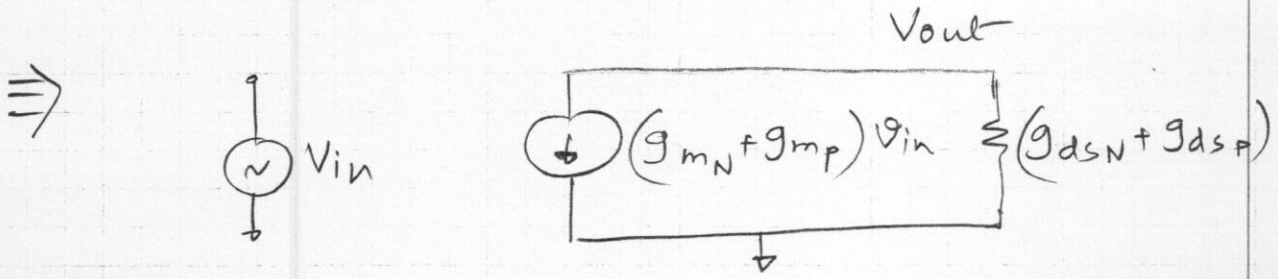
To allow for i/p signal swing & to keep out of sub.thrsh region $V_{DSAT} > 150mV$ (gen. design

CS Amp with Active Load









$$A_v = -\frac{(g_{mN} + g_{mp})}{(g_{dsN} + g_{dsp})}$$

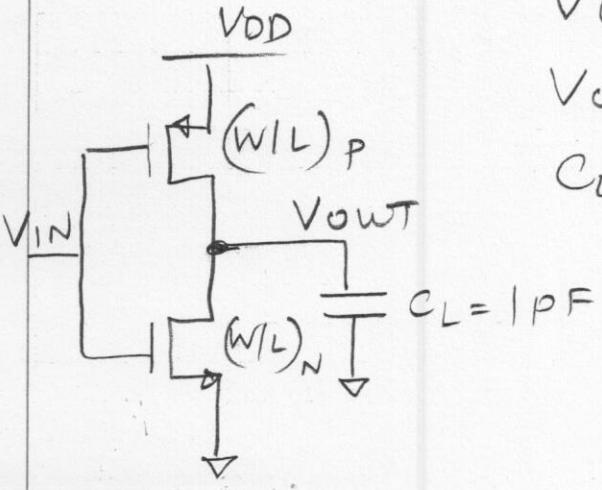
Num. Example:

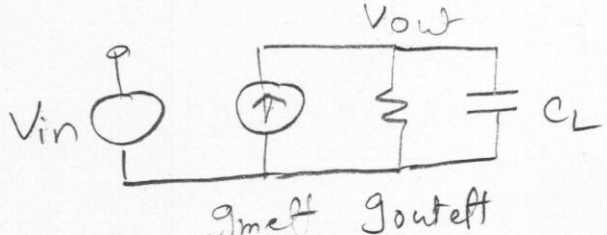
gain $A_v \geq 100$

$V_{out_{min}} = 250mV$

$V_{OUT_{max}} = Vdd - 250mV$

$C_L = 1pF$: $f_u = 100MHz$ unity gain frequency





ignoring transistor internal caps. ($<< 1pF$)

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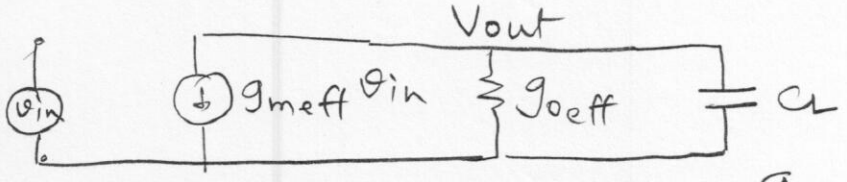
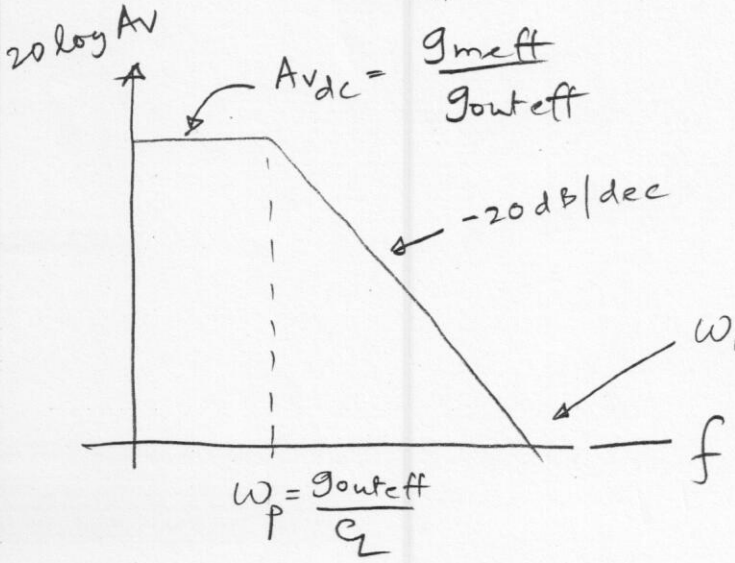


$$v_{out} = \frac{-g_{meff} v_{in}}{(g_{oeff} + sC_L)} = \frac{-\frac{g_{meff}}{g_{outeff}}}{\left(1 + \frac{s}{g_{outeff}/C_L}\right)}$$

DC gain

$\omega_p =$



$|A_v| = 1$

$$f_u = \frac{\omega_u}{2\pi} = \frac{1}{2\pi} \cdot \frac{g_{meff}}{C_L} = 100MHz$$

$$g_{meff} = 2\pi C_L * 100MHz = 2 \times \pi \times 1 \times 10^{-12} \times 10^{8} \text{ S}$$

$$= 628 \ \mu S \quad \text{—— (1)}$$

Symmetric o/p voltage swing $V_{DSATN} = V_{DSATp} = 250m$

$$\sqrt{\frac{2I}{K_N\left(\frac{W}{L}\right)_N}} = \sqrt{\frac{2I}{K_p\left(\frac{W}{L}\right)_p}} \Rightarrow \left(\frac{W}{L}\right)_p = \frac{K_N}{K_p}\left(W/L\right)_N$$

$$K_N = \mu_N C_{ox} = 136.5 \ \mu A/V^2$$

$$K_p = \mu_p C_{ox} = 39 \ \mu A/V^2$$

$$\left(\frac{W}{L}\right)_p = \frac{136.5}{39}\left(\frac{W}{L}\right)_N = 3.5\left(\frac{W}{L}\right)_N. \quad \text{—— (2)}$$

$$g_{m1} = g_{mp} = \frac{2I}{}$$

$g_{meff} = g_{mN} + g_{mp} \Rightarrow g_{mN} = g_{mp} = 314\,\mu S$

$\frac{2I}{V_{DSAT}} = 314\,\mu S \Rightarrow I = \frac{314\,\mu S \times 250\,mV}{2}$

$I = 39.25\,\mu A$ ——— (3)

To maximize voltage gain

$A_v = \frac{g_{mN} + g_{mp}}{g_{dsN} + g_{dsp}} \Rightarrow g_{dsN} = g_{dsp}$

$g_{dsN} = \lambda_N I = \frac{0.05}{L_n\,(\text{in }\mu m)} I$

$g_{dsp} = \lambda_p I = \frac{0.1}{L_p\,(\text{in }\mu m)} I$

$\Rightarrow L_p = 2 L_n$ (Channel Length)

$A_v = \frac{628\,\mu S}{2 \cdot g_{ds}} = 100 \Rightarrow g_{ds_{N,P}} = 3.14\,\mu S.$

$\frac{0.05 \times I}{L_n} = 3.14\,\mu S \Rightarrow L_n = \frac{0.05 \times 39.25\,\mu A}{3.14\,\mu S}$

(L_n in μ)

$L_N = 0.625\,\mu m.$

$L_p = 2 \cdot L_N = 1.25\,\mu m$

0.5 μm Technology → grid 0.25 μm

Round up L values to get on grid & make sure $A_v > 100$

$L_N = 0.75\,\mu m \quad L_p = 1.5\,\mu m$

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$$V_{DSAT_N} = \sqrt{\frac{2I}{K_N (W/L)_N}} < 0.25\,V$$

$$\left(\frac{W}{L}\right)_N > \frac{2I}{K_N \cdot (0.25)^2} = \frac{2 \times 39.25\,\mu A}{136.5\,\mu A/V^2 \times (0.25)^2 V^2}$$

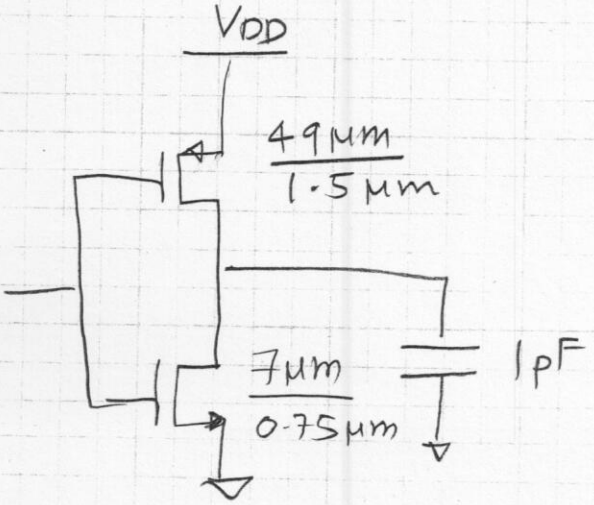
$$= 9.2$$

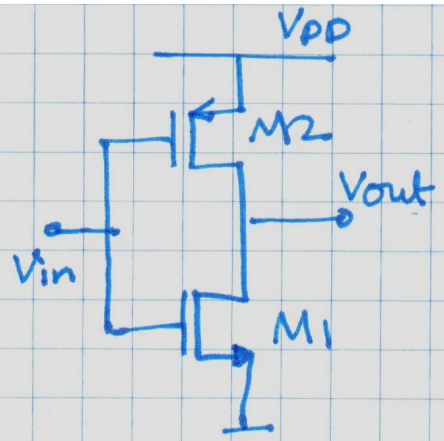
$$W_N > 9.2 \times 0.75\,\mu m = 6.9\,\mu m$$

$$W_N = 7\,\mu m$$

$$\left(\frac{W}{L}\right)_p = 3.5 \times \left(\frac{W}{L}\right)_N \Rightarrow W_p = 3.5 \times \frac{7}{0.75} \times 1.5$$

$$W_p = 49\,\mu m$$





Represents AC behavior of circuit.

DC circuit – different

$V_{Dsat_N} = V_{Dsat_P} = 0.25\,V$

$\therefore V_{GS_N} = V_{T_N} + V_{Dsat_n} = 0.5 + 0.25$

$= 0.75\,V$

$V_{SG_P} = |V_{T_P}| + V_{Dsat_P} = 0.6 + 0.25$

$= 0.85\,V$

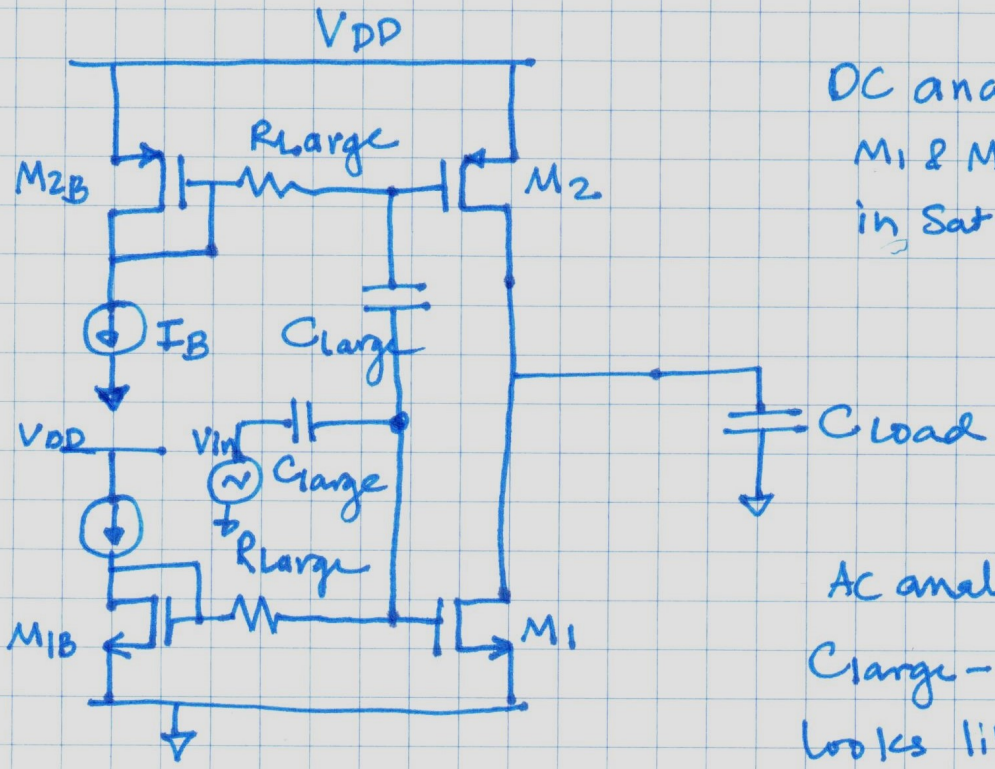
DC condition

$V_{DD} = V_{SG_P} + V_{GS_N}$

$= 0.85 + 0.75 = 1.6\,V$

Satisfied only for $V_{DD} = 1.6\,V$.

Actual circuit implementation DC & AC

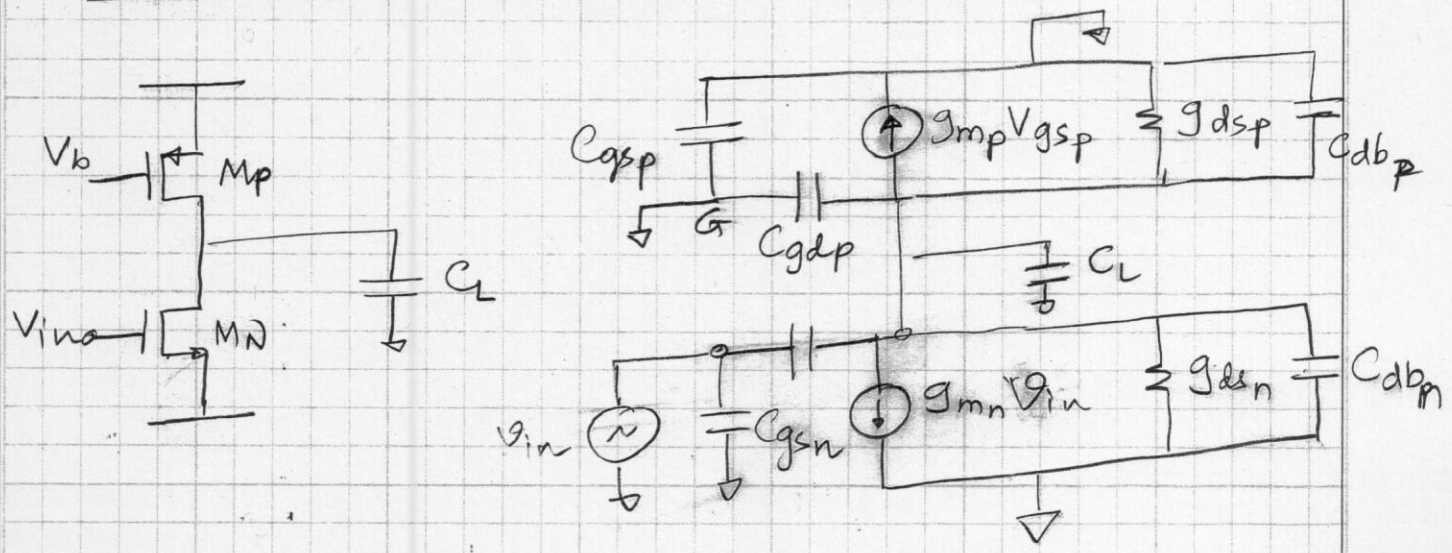


DC analysis
M1 & M2 are biased in Sat with I_B

AC analysis
CLarge – short
looks like inverter amplifier.

C-S Amplifier with Current source load.

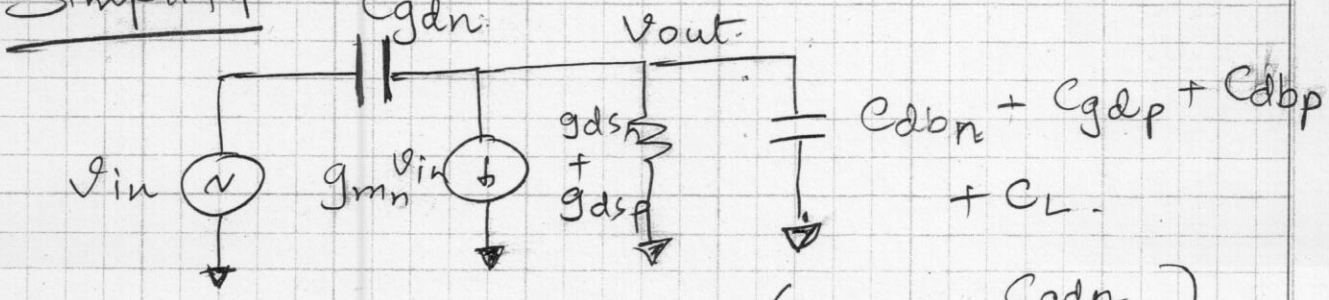
FREQUENCY RESPONSE – Detailed



Neglect g_{mp}, g_{mbsn}, g_{mbsp} – No sig.

Neglect C_{gsn}, C_{gsp} – driven by v_{in}

Simplify



$$A_v = \frac{v_{out}}{v_{in}} = -\frac{g_{mn}}{g_{dsn}+g_{dsp}} \cdot \frac{\left(1 - s\frac{C_{gdn}}{g_{mn}}\right)}{\left(1 + s\left(\frac{C_{gdn}+C_{gdp}+C_{dbn}+C_{dbp}+C_{gdp}+C_L}{g_{dsn}+g_{dsp}}\right)\right)}$$

RHP zero $\quad \omega_z = +\frac{g_{mn}}{C_{gdn}}$

LHP pole $\quad \omega_p = -\frac{g_{out}}{C_{out}} = -\frac{g_{dsn}+g_{dsp}}{C_{gdn}+C_{gdp}+C_{dbn}+C_{dbp}+C_L}$

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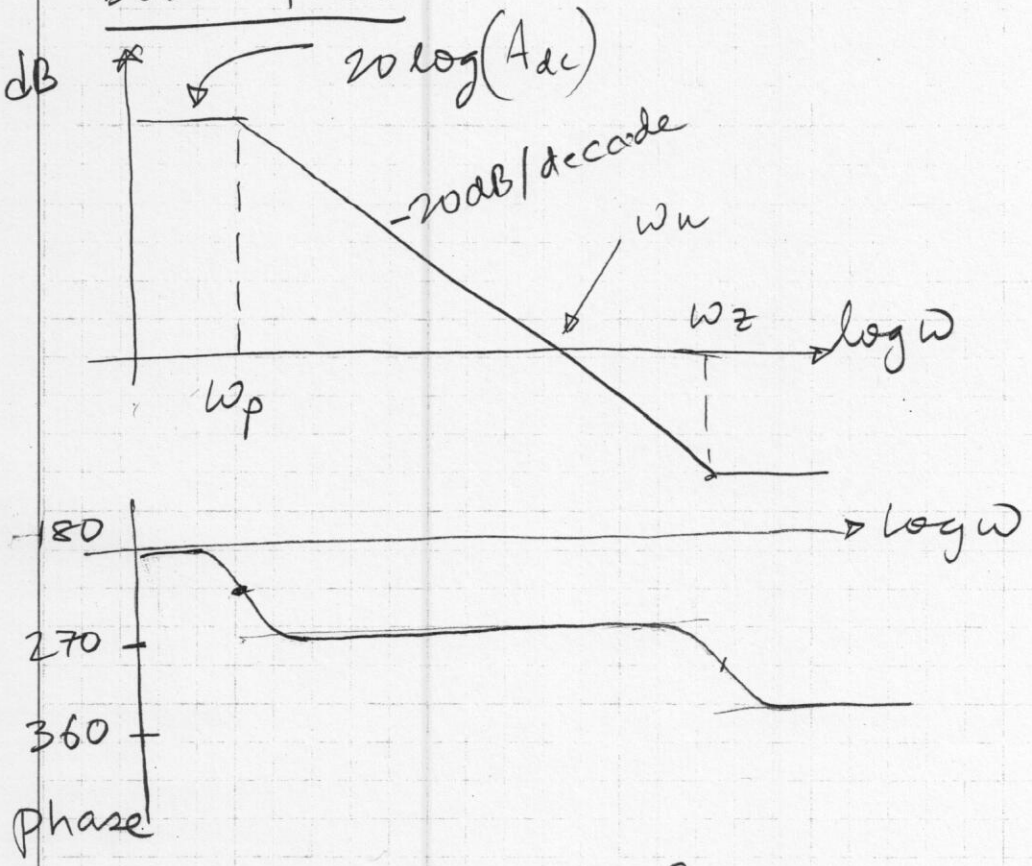
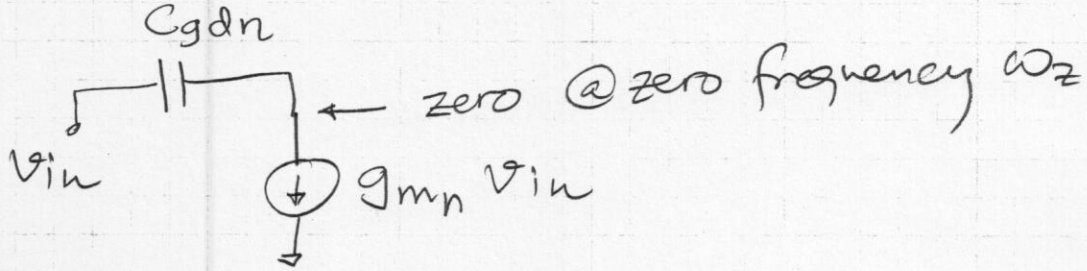
Bode Plots



In Closed-loop feedback system (Study Later)

RHP zero

- keeps gain high @ high freq.
- phase shift degrades @ high freq.



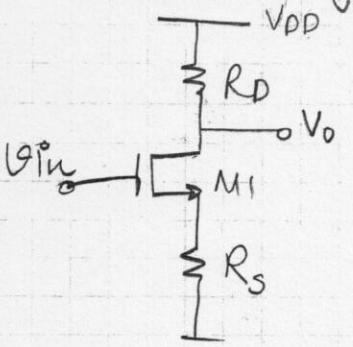
$$s_z C_{gdn} \cdot V_{in} = g_{mn} V_{in}$$

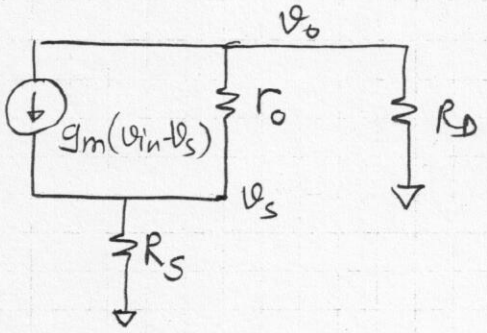
$$s_z = \frac{g_{mn}}{C_{gdn}} \leftarrow \text{Real \& +ve RHP.}$$

Quick way to analyse.

cap across inverting stage → RHP zero
cap across non inverting stage

Source degeneration





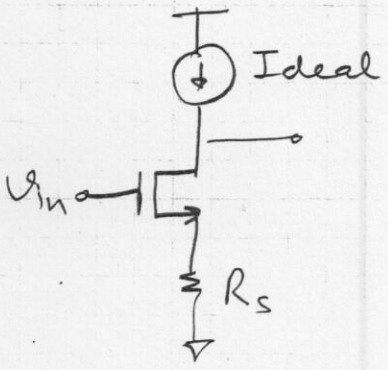
$$g_m(v_{in}-v_s)+\frac{v_o-v_s}{r_o}=\frac{v_s}{R_s} \quad \Big\| \quad \text{Also} \quad \frac{v_s}{R_s}=-\frac{v_o}{R_D} \Rightarrow v_s=-\frac{R_s}{R_D}v_o$$

$$g_m v_{in}+\left[g_m+\frac{1}{r_o}+\frac{1}{R_s}\right]v_s+\frac{v_o}{r_o}=0$$

$$g_m v_{in}+\left(g_m+\frac{1}{r_o}+\frac{1}{R_s}\right)\frac{R_s}{R_D}v_o+\frac{v_o}{r_o}=0$$

$$g_m r_o R_D v_{in}+\left[\left(g_m r_o+1+\frac{r_o}{R_s}\right)R_s+R_D\right]v_o=0$$

$$\boxed{\frac{v_{out}}{v_{in}}=\frac{-g_m r_o R_D}{R_D+r_o+R_s(g_m r_o+1)}}$$



$$\frac{v_{out}}{v_{in}}=-g_m r_o \quad \Big\{ R_D=\infty.$$

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Theorem

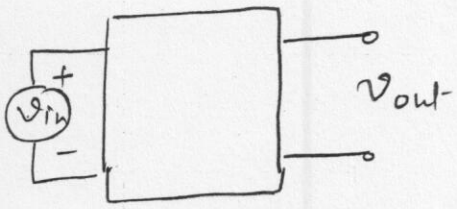
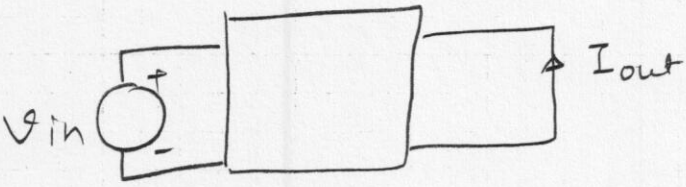


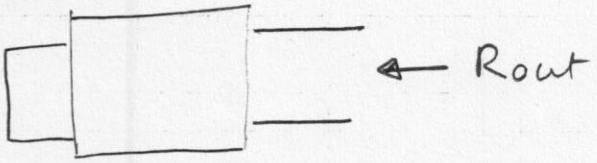
Figure out Voltage gain $\frac{v_{out}}{v_{in}}$

① Short ckt Gm.



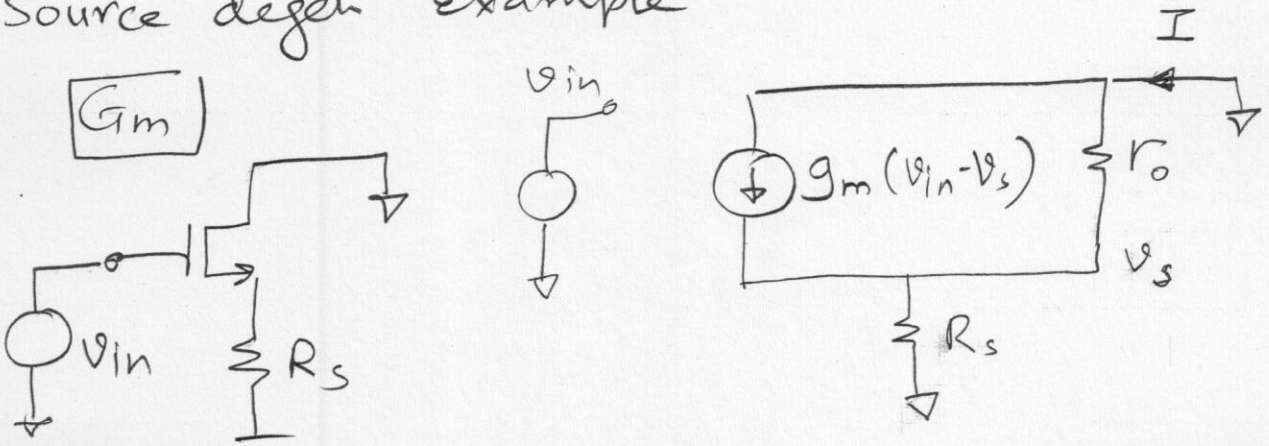
$$G_m = \frac{I_{out}}{v_{in}}$$

② Rout calculation



Voltage Gain $\frac{v_{out}}{v_{in}} = -G_m R_{out}$

Source degen Example



$$g_m(v_{in} - v_s) - \frac{v_s}{r_o} - \frac{v_s}{R_s} = 0$$

$$g_m v_{in} = \left(g_m + \frac{1}{r_o} + \frac{1}{R_s}\right) v_s$$

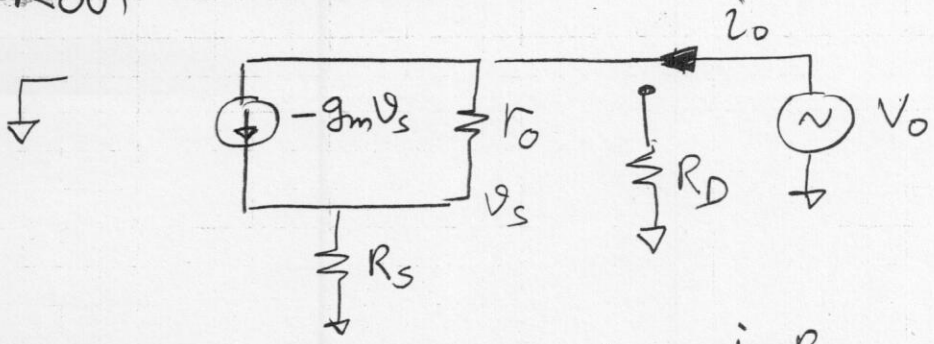
$$I = \frac{v_s}{R_s} = \frac{g_m v_{in}}{R_s\left(g_m + \frac{1}{r_o} + \frac{1}{R_s}\right)}$$

$$G_m = \frac{I}{v_{in}} = \frac{g_m}{g_m R_s + 1 + \frac{R_s}{r_o}}$$

$\Rightarrow$ if r_o is large $\quad \boxed{G_m \approx \frac{g_m}{g_m R_s + 1}}$

$$\boxed{G_m = \frac{g_m r_o}{(g_m r_o + 1) R_s + r_o}}$$

R_{OUT} Calculation



① W/o R_D.

$$v_s = i_o R_s$$

$$g_m v_s + i_o = \frac{v_o - v_s}{r_o}$$

$$\left(g_m i_o R_s + i_o\right) r_o = v_o - i_o R_s$$

$$\frac{v_o}{i_o} = \left[(1 + g_m r_o) R_s + r_o\right]$$

$$\approx g_m r_o R_s + r_o$$

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including $\| R_D$

$$R_{out} = \frac{[(1 + g_m r_o) R_s + r_o] R_D}{R_D + r_o + (1 + g_m r_o) R_s}$$

$$\frac{V_{out}}{V_{in}} = -G_m R_{out}$$

$$= -\frac{g_m r_o}{(g_m r_o + 1) R_s + r_o} \times \frac{[(g_m r_o + 1) R_s + r_o] R_D}{R_D + r_o + (1 + g_m r_o) R_s}$$

$$= -\frac{g_m r_o R_D}{R_D + r_o + (1 + g_m r_o) R_s} \leftarrow$$

Same as what we directly derived !!!

If we ignore r_o

$$G_m = \frac{g_m}{1 + g_m R_s} \quad ; \quad R_{out} = R_D$$

$$\frac{V_{out}}{V_{in}} = -\frac{g_m R_D}{1 + g_m R_s}$$

} (Quick Calculation)

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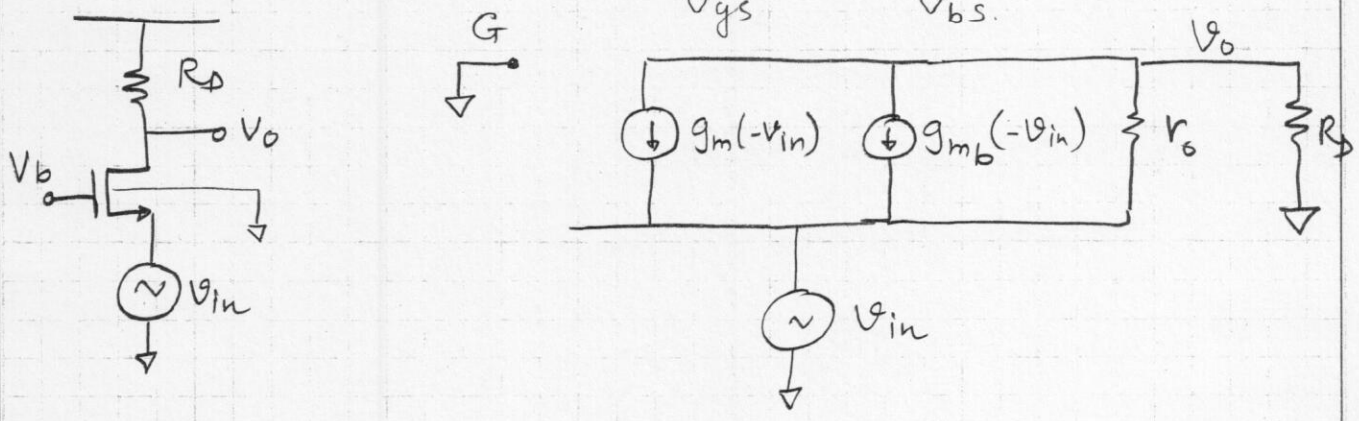
Common Gate amplifier



$$\frac{v_o}{R_D} = g_m v_{in} + g_{mb} v_{in} + \frac{v_{in} - v_o}{r_o}$$

$$\frac{v_o}{}\left(\frac{1}{R_D} + \frac{1}{r_o}\right) = (g_m + g_{mb}) v_{in} + \frac{v_{in}}{r_o}$$

$$\frac{v_o}{v_{in}} = \frac{\left((g_m + g_{mb}) r_o + 1\right)}{(r_o + R_D)} R_D$$

If we ignore body effect

$$\frac{v_o}{v_{in}} = \frac{g_m r_o + 1}{(r_o + R_D)} R_D \longrightarrow \text{✡}$$

$$Z_{in} = \frac{v_{in}}{I_{in}} = \frac{v_{in}}{V_o / R_D} = \frac{R_D \cdot (r_o + R_D)}{(g_m r_o + 1) R_D}$$

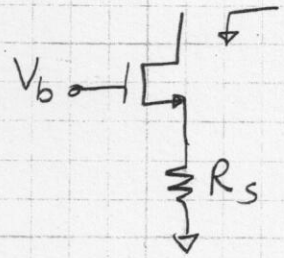
$$Z_{in} = \frac{r_o + R_D}{(g_m r_o + 1)} \simeq \frac{r_o + R_D}{g_m r_o}$$

Drain impedance div by $(g_m r_o)$ ↓

ONLY WHEN $R_D \ll r_o$

$Z_{in} \cong$ ro/(gm ro)=1/gm (low impedance)

In case of source degeneration



$$R_{out} \cong (g_m r_o) R_s + r_o$$

R_{out} ↑ by $(g_m r_o)$

Cascode from Vacuum tubes
1939 - Frederick HUNT
Cascode of two triodes instead of pentode
Iguitar amp

Cascode CS Amplifier

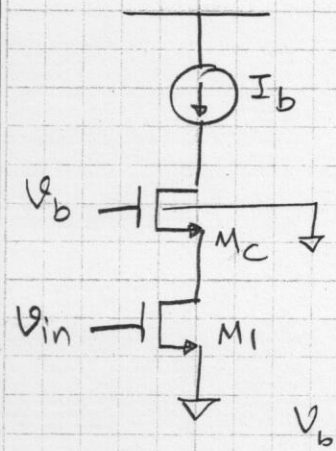
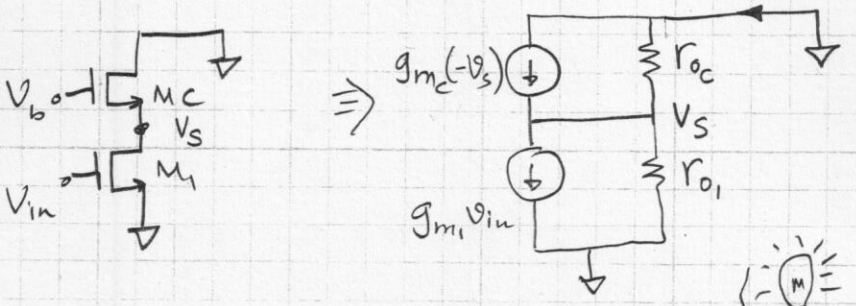


Figure out Gm & Rout

$$A_v = -G_m R_{out}$$

Gm calculation



Use g_{ds} & r_o interchan for convenien

$$g_{m_1} v_{in} + \frac{v_s}{r_{o_1}} + g_{m_c} v_s + \frac{v_s}{r_{o_c}} = 0$$

$$g_{m_1} v_{in} + v_s \left(\frac{1}{r_{o_1}} + \frac{1}{r_{o_c}} + g_{m_c} \right) = 0$$

g_{ds_1} g_{ds_c}

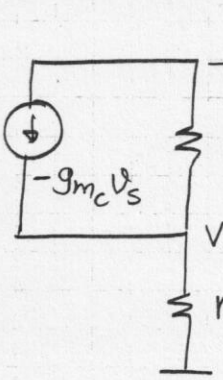
$$v_s = \frac{-g_{m_1} v_{in}}{(g_{ds_1} + g_{ds_c} + g_{m_c})}$$

$$i_{out} = g_{m_1} v_{in} + v_s g_{ds_1} = g_{m_1} v_{in} - \frac{g_{m_1} v_{in} g_{ds_1}}{(g_{ds_1} + g_{ds_c} + g_{m_c})}$$

$$\frac{i_{out}}{v_{in}} = \frac{g_{m_1}\left(g_{ds_1} + g_{ds_c} + g_{m_c} - g_{ds_1}\right)}{\left(g_{ds_1} + g_{ds_c} + g_{m_c}\right)}$$

$$\boxed{G_m \approx g_{m_1}}$$

Rout Calculation



$$v_s = i_o r_{o_1}$$

$$i_o = -g_{m_c} v_s + \frac{(v_o - v_s)}{r_{o_c}}$$

$$i_o = -g_{m_c} i_o r_{o_1} + \frac{(v_o - i_o r_{o_1})}{r_{o_c}}$$

$$i_o r_{o_c} = -g_{m_c} i_o r_{o_1} r_{o_c} + v_o - i_o r_{o_1}$$

$$R_{out} = \frac{v_o}{i_o} = \underbrace{\left(g_{m_c} r_{o_c} r_{o_1}\right)}_{\text{large}} + \underbrace{r_{o_1} + r_{o_c}}_{\text{small}}$$

$$R_{out} \approx \left(g_{m_c} r_{o_c}\right) r_{o_1}$$

Cascode self gain multiplier effect

$$\boxed{A_v = \left(g_{m_1} r_{o_1}\right)\left(g_{m_c} r_{o_c}\right) \approx \left(g_m r_o\right)^2}$$

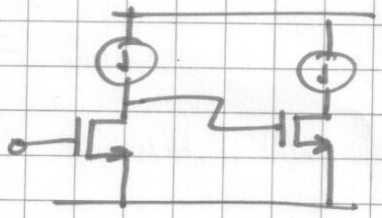
Benefits of cascoding

- (+) Rout → self gain of cascode multiplication
  - can be used for high o/p impedance current source
- (+) gain ↑ squared
- (-ve) Headroom Reduced to keep two transistors in saturation

$$V_{out_{min}} = V_{dsat_1} + V_{dsat_c}$$

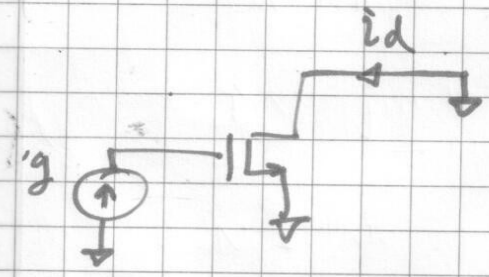
f_T discussion

Transition frequency —



voltage gain = 1

$$\omega_T = \frac{g_m}{C_{gs}}$$



Current gain = 1

$$\omega_T = \frac{g_m}{C_{gs}}$$

Give an idea of Raw speed capability of transistor

Why Transit frequency ?

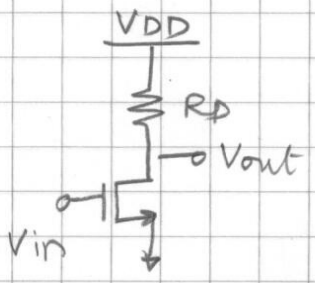
$$\omega_T f_T = \frac{g_m}{C_{gs}} = \frac{\mu_n C_{ox} \frac{W}{L}(V_{GS}-V_{TH})}{\frac{2}{3} C_{ox} W \cdot L} = \frac{\left[\frac{3}{2}(V_{GS}-V_{TH})\right]\mu_n}{L}$$

$$= \frac{\mu_n [E_{channel}]}{L} = \frac{v}{L} = \frac{1}{\tau_T}$$

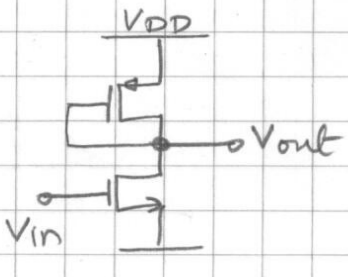
τ_T : Transit Time from source to drain

$f_T \Rightarrow$ gives an idea of intrinsic delay of device.

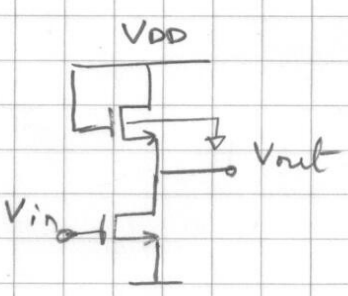
Recap f_T discussion. — Why Transit frequency



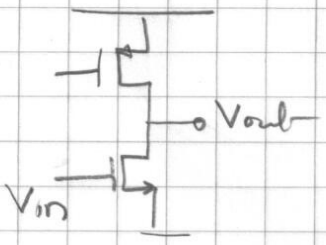
$$\frac{V_{out}}{V_{in}} \cong -g_m (r_o \| R_D)$$



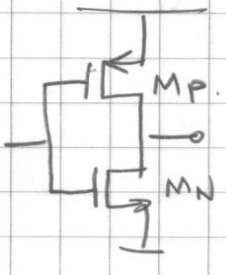
$$\frac{V_{out}}{V_{in}} \cong -\frac{g_{m_1}}{g_{m_2}}$$



$$\frac{V_{out}}{V_{in}} = \frac{-g_{m_1}}{g_{m_2} + g_{mbs_2}}$$

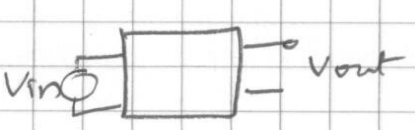


$$\frac{V_{out}}{V_{in}} = -g_{m_1} (r_{o_1} \| r_{o_2})$$



$$\frac{V_{out}}{V_{in}} = -\frac{(g_{mN} + g_{mP})}{(g_{dsN} + g_{dsP})}$$

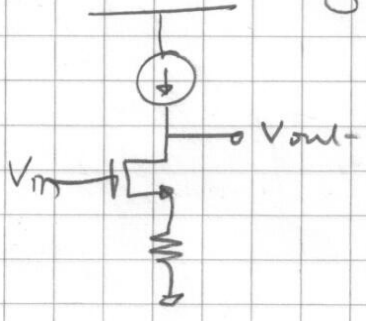
XF Theorem



Short Ckt G_m & R_{out}

$$\frac{V_{out}}{V_{in}} = -G_m R_{out}$$

Source degeneration

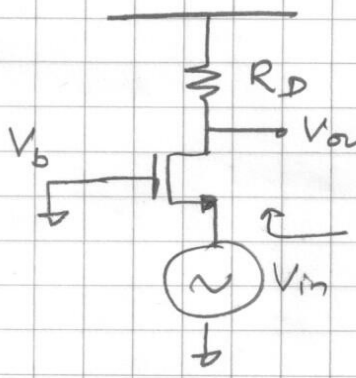


$$G_m \cong \frac{g_m}{1+g_m R_s}$$

$$R_{out} = g_m r_o R_s + r_o$$

$$\frac{V_{out}}{V_{in}} \approx -G_m R_{out} = -g_m r_o$$

Common Gate Amplifier

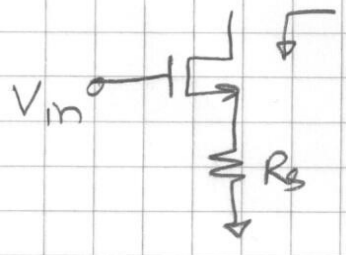


$$\frac{V_{out}}{V_{in}} = \frac{g_m r_o}{(r_o + R_D)} R_D$$

(Body effect ignored)

$$Z_{in} = \frac{r_o + R_D}{(g_m r_o + 1)} \approx \frac{r_o + R_D}{(g_m r_o)} \approx \frac{1}{g_m}$$

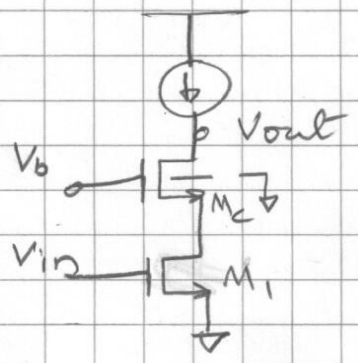
($R_D >>$



$$R_{out} = (g_m r_o) R_s + r_o$$

R_{out} ↑ $(g_m r_o)$ factor

Cascode Common Source Amplifier

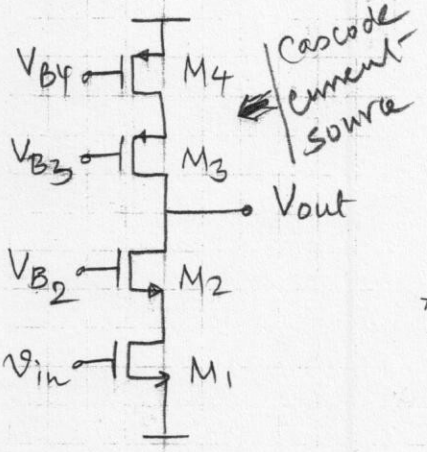


$$A_v = -G_m \cdot R_{out}$$

$$\cong -g_{m_1}\left(g_{m_c} r_{o_c} \cdot r_{o_1}\right)$$

$$\approx -\left(g_{m_1} r_{o_1}\right)\left(g_{m_c} r_{o_c}\right)$$

Cascode Stage with current source



$$G_m = g_{m_1}$$

$$R_{out} = (g_{m_2} r_{o_2}) r_{o_1} \parallel (g_{m_3} r_{o_3}) r_{o_4}$$

Assuming $r_{o_1} = r_{o_2} = r_{o_3} = r_{o_4} = r_o$

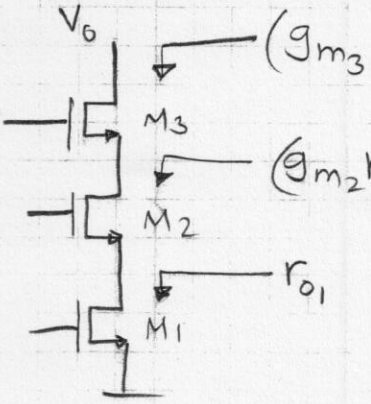
$$g_{m_1} = g_{m_2} = g_{m_3} = g_{m_4} = g_m$$

$$A_v = -\frac{1}{2}(g_m r_o)^2$$

$$V_{out\,min} = V_{dsat_1} + V_{dsat_2}$$

$$V_{out\,max} = V_{dd} - (|V_{dsat_3}| + |V_{dsat_4}|)$$

Tripple Cascode



$(g_{m_3} r_{o_3})(g_{m_2} r_{o_2}) r_{o_1}$ ← Really high o/p impedance

$(g_{m_2} r_{o_2}) r_{o_1}$

r_{o_1}

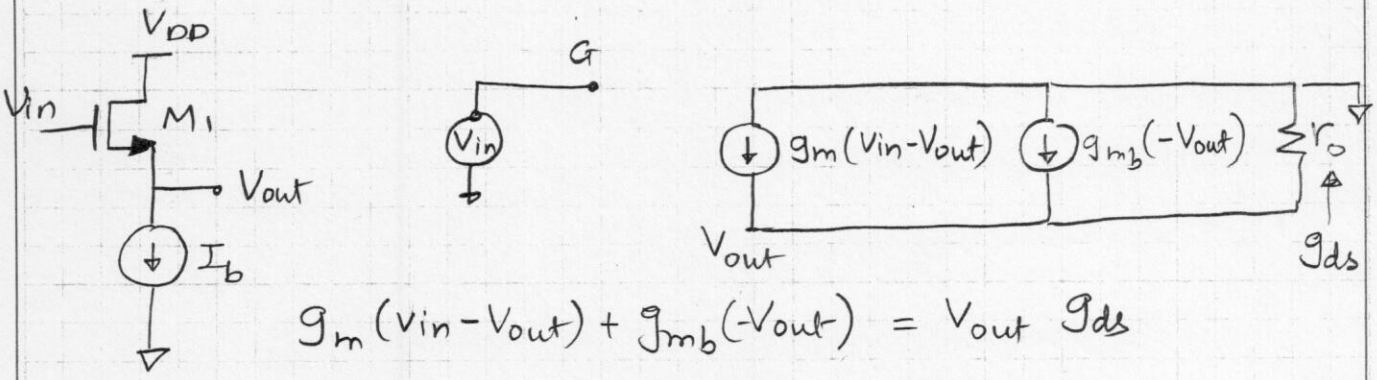
$$V_{o\,min} = V_{dsat_1} + V_{dsat_2} + V_{dsat_3}$$

(with proper biasing.)

Also called

Telescopic Cascode

Common drain Amplifier (Source follower)



$$g_m(V_{in}-V_{out}) + g_{mb}(-V_{out}) = V_{out}\, g_{ds}$$

$$(g_m + g_{mb} + g_{ds})V_{out} = g_m V_{in}$$

$$\frac{V_{out}}{V_{in}} = \frac{g_m}{g_m + g_{mb} + g_{ds}} \approx \frac{g_m}{g_m + g_{mb}} = \frac{1}{1+\eta} \approx 1$$

→ Non-inverting unity gain. amplifier

$r_{in} = \infty$ $\quad r_{out} = \dfrac{1}{g_m + g_{mb} + g_{ds}} \approx \dfrac{1}{g_m}$ Low imp.

→ O/P DC range

$$V_{out} = V_{in} - (V_{T_1} + V_{dsat_1})$$

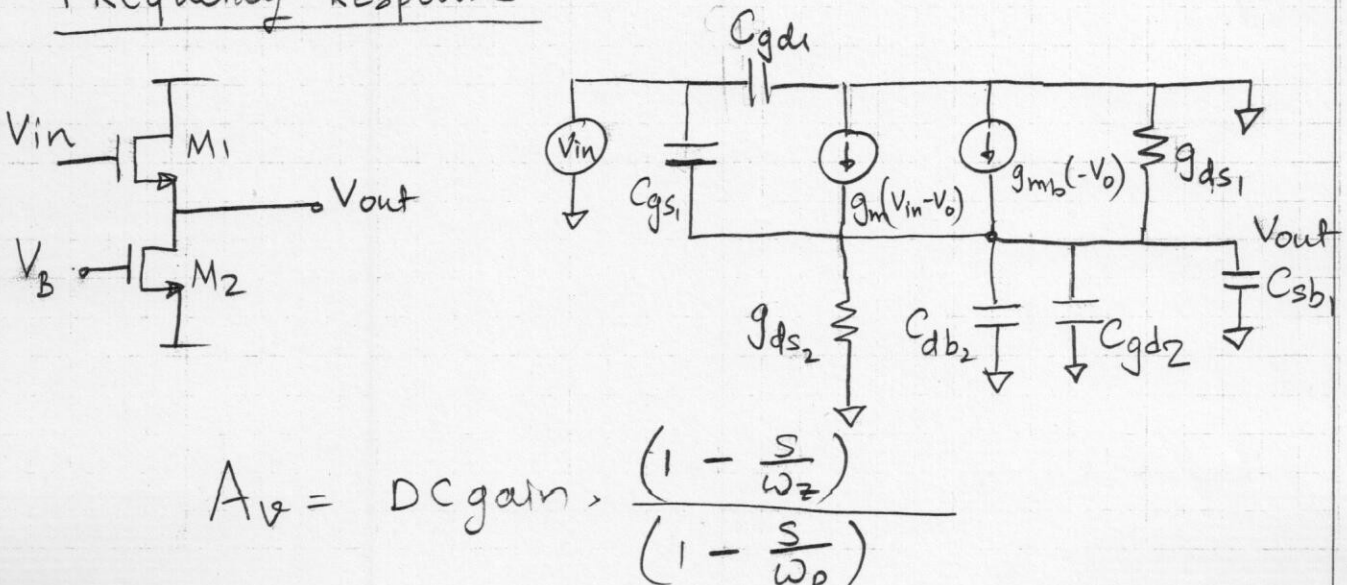
$$V_{out\,max} = V_{DD} - (V_T + V_{dsat})$$

$$V_{in\,max} = V_{DD}$$

$$V_{in\,min} = V_T + V_{dsat} + \underbrace{V_{dsat}}_{cs}$$

→ DC-level shifter & Buffer. (low O/P imp)

Frequency Response



$$A_v = \text{DC gain} \cdot \frac{\left(1 - \frac{s}{\omega_z}\right)}{\left(1 - \frac{s}{\omega_p}\right)}$$

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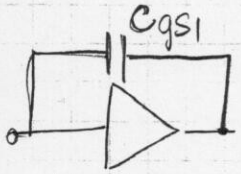
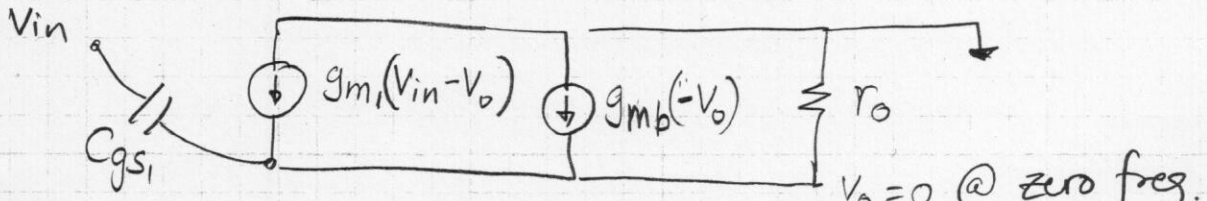
LHP $\omega_p = -\frac{g_{out}}{C_{out}} = -\frac{g_{m_1} + g_{mbs_1} + g_{ds_1} + g_{ds_2}}{C_{gs_1} + C_{sb_1} + C_{db_2} + C_{gd_2}}$



$\Rightarrow$ LHP zero.

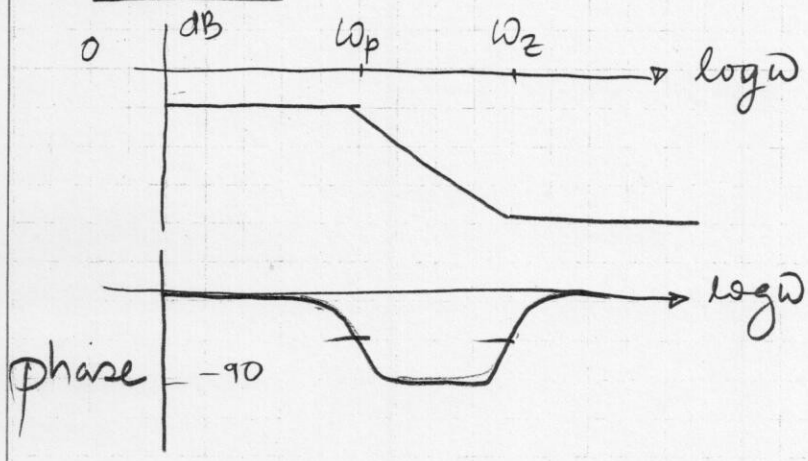


@ Zero frequency ω_z

$$\omega_z C_{gs_1} \cdot v_{in} = -g_{m_1} V_{in} \Rightarrow \boxed{\omega_z = -\frac{g_{m_1}}{C_{gs_1}}}$$

$$A_V = \frac{g_{m_1}}{g_{m_1} + g_{mbs_1} + g_{ds_1} + g_{ds_2}} \cdot \frac{\left(1 + \frac{s}{g_{m_1}/C_{gs_1}}\right)}{\left(1 + \frac{s}{\left(\frac{g_{m_1} + g_{mbs_1} + g_{ds_1} + g_{ds_2}}{C_{gs_1} + C_{sb_1} + C_{db_2} + C_{gd_2}}\right)}\right)}$$

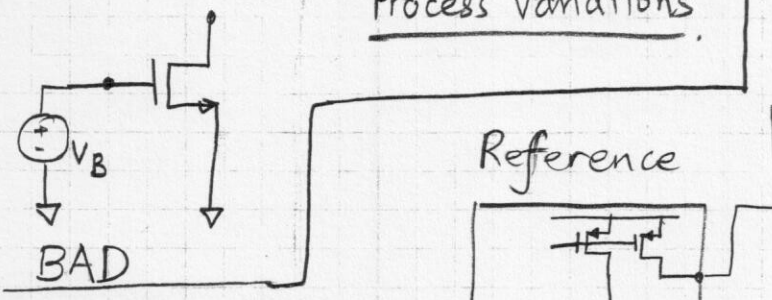
Bode Plot



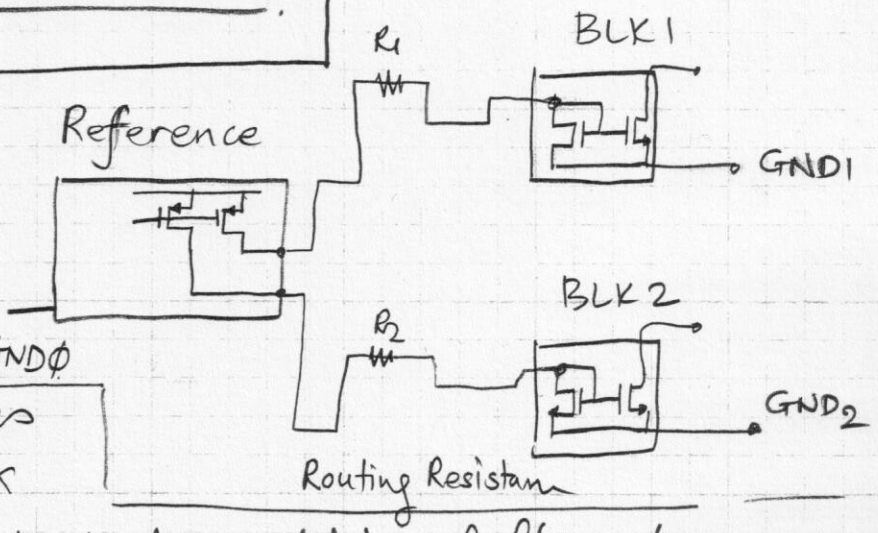
New Topic MOS Current Mirrors / Sources

Novice Biasing

Process variations.



ON CHIP CURRENT DISTRIBUTION



sending voltage as reference XXX

→ Gnd / Vdd potentials could be different

→ transistor properties across the chip change.

Current Sources used for DC biasing,
Active load to get max gain without IR drop.

Specs →
- → Output Resistance
- → voltage compliance (min or max voltage)
- → Accuracy & process independance.
- → DC balance (for mirrors)
- → i/p Resistance (for mirrors)

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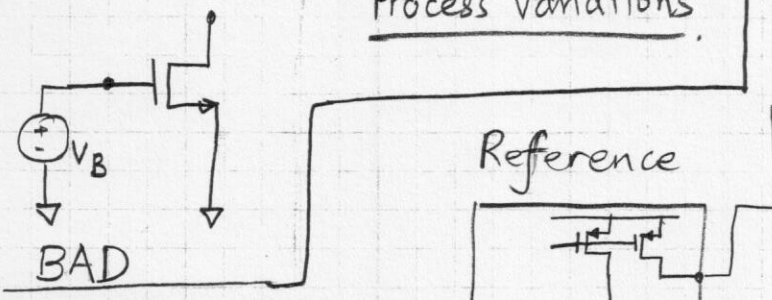
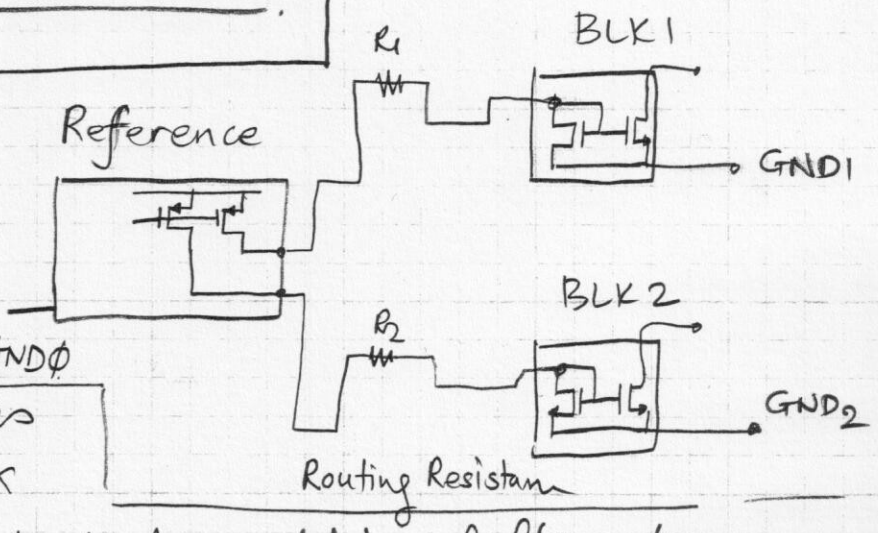
New Topic MOS Current Mirrors / Sources

Novice Biasing

Process variations.



ON CHIP CURRENT DISTRIBUTION



sending voltage as reference XXX

→ Gnd / Vdd potentials could be different

→ transistor properties across the chip change.

Current Sources used for DC biasing,
Active load to get max gain without IR drop.

Specs →
- → Output Resistance
- → voltage compliance (min or max voltage)
- → Accuracy & process independance.
- → DC balance (for mirrors)
- → i/p Resistance (for mirrors)

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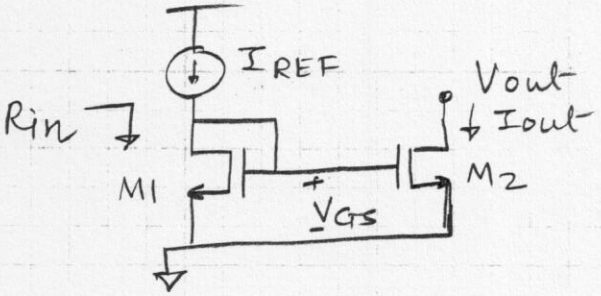
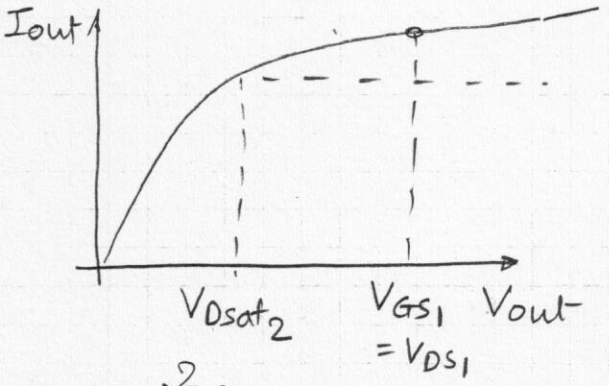
Simple Current mirror



$$R_{in} = \frac{1}{g_{m_1} + g_{ds_1}} \approx \frac{1}{g_{m_1}}$$



$$I_{REF} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{T_1})^2 (1 + \lambda_1 V_{GS_1})$$

$$I_{OUT} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{T_2})^2 (1 + \lambda_2 V_{out})$$

Assume $V_{T_1} = V_{T_2}$

$$\frac{I_{OUT}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1} \frac{(1 + \lambda_2 V_{OUT})}{(1 + \lambda_1 V_{GS})}$$

small

For accurate mirroring, keep L same $\Rightarrow \lambda_1 = \lambda_2$

$$\frac{I_{OUT}}{I_{REF}} = \frac{W_2}{W_1}\left(1 + \lambda (V_{out} - V_{GS})\right)$$

To keep λ small → use long channel device
L large $\gg L_{min}$

$$I_{OUT} = \frac{W_2}{W_1} I_{RFF}$$

For accurate mirroring $W_2 = N W_1$ (N: Integer)

DO NOT SCALE THE TRANSISTOR SIZE.

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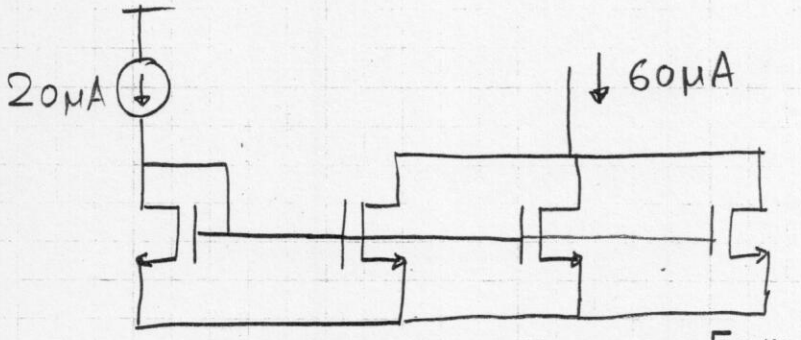
Example

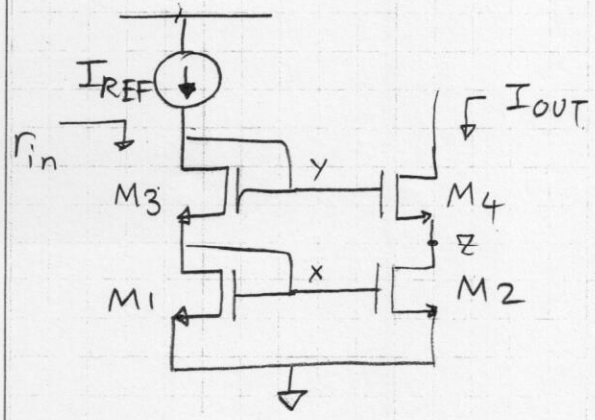


$\frac{W}{L}$	$\frac{5\mu m}{1\mu m}$	$\frac{5\mu m}{1\mu m}$	$\frac{5\mu m}{1\mu m}$	$\frac{5\mu m}{1\mu m}$ ← Large L, $\lambda\downarrow$

$$V_{out\,min} = V_{dsat_2}$$

$$R_{out} = \frac{1}{g_{ds_2}}$$

CASCODE CURRENT MIRROR



$$r_{in} = \frac{2}{g_m}$$

$$r_{out} \cong (g_{m_4} r_{o_4})\, r_{o_2}$$

$$V_y = V_{GS_3} + V_{GS_1}$$

$$V_z = V_{GS_3} + V_{GS_1} - V_{GS_4} = V_{GS_1}$$

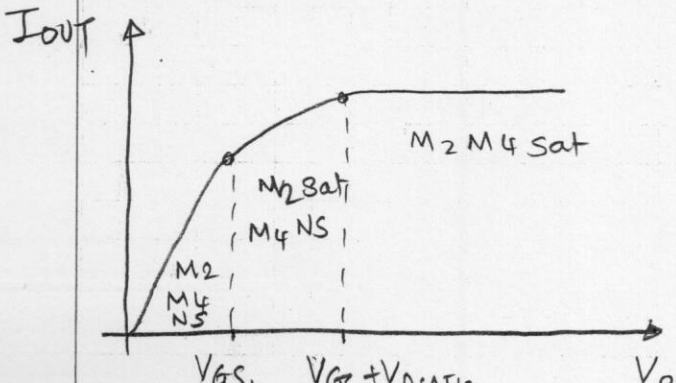
$$V_{OUT\,min} = V_z + V_{dsat_4}$$

$$= V_{GS_1} + V_{dsat_4}$$

$$\cong V_T + 2V_{dsat}$$

$$0.5V + 0.4V = 0.9V$$

NOT SUITABLE for low voltage



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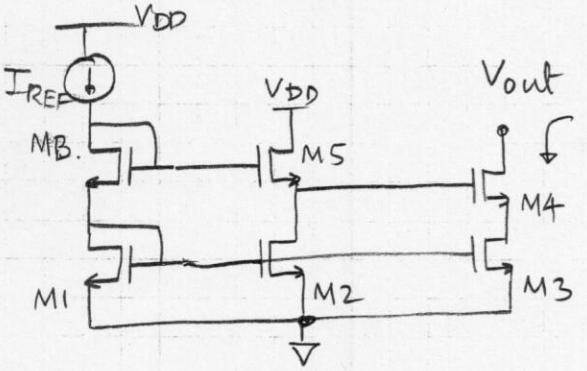
High Swing Cascode CM



DC imbalance M1 ↔ M3 different V_{DS}.

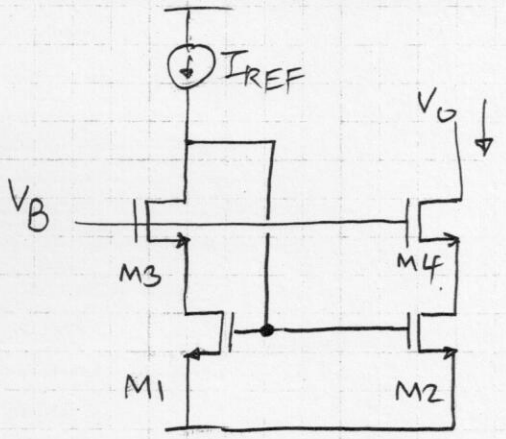
$M_1 - M_5$ identical.

$$\left(\frac{W}{L}\right)_B = \frac{1}{4}\left(\frac{W}{L}\right)_{1\text{-}5}$$

$$\Rightarrow V_{GS_B} = V_T + 2V_{dsat_1}$$

$$V_{OUT\,min} = 2V_{Dsat_1}$$

Low-voltage High swing Cascode CM.



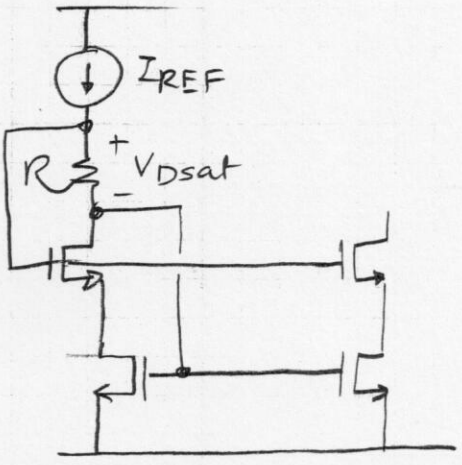
DC balance ✓

$$V_{DS_1} = V_{DS_2} = V_{Dsat}$$

$$V_B = V_T + 2V_{Dsat}$$

$$V_{omin} = 2V_{Dsat}$$

Smart Biasing



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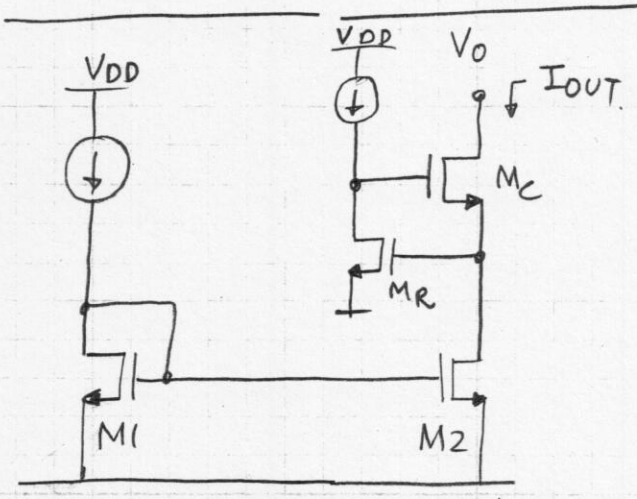
REGULATED CASCODE CM

YANG - ALLSTOT 1990 - CAS Tran



Series feedback

$V_{O_{min}} = V_{GS_R} + V_{Dsat_C}$

$= V_T + 2V_{dsat}$

Feedback loop $M_R - M_C$ - Loop gain $= (g_{m_R} r_{O_R}) \cdot 1$

r_{out} (without feedback) $= r_{O_2} \cdot (g_{m_C} r_{O_C})$

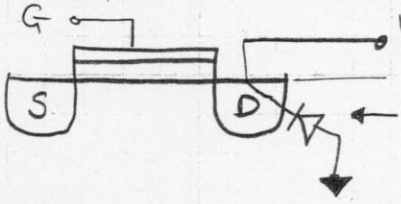
r_{out} (with feedback) $= r_{O_2} (g_{m_C} r_{O_C}) \cdot (g_{m_R} r_{O_R})$

$= (g_m r_O)^2 r_O$

$= (25)^2 \times 10K \approx 6.25\ M\Omega$

Really large

→ In reality r_{out} limited by leakage current due to Drain - Bulk diode of M_C.



← Diode leakage at high temperature

1.5V 500nA → 3MΩ

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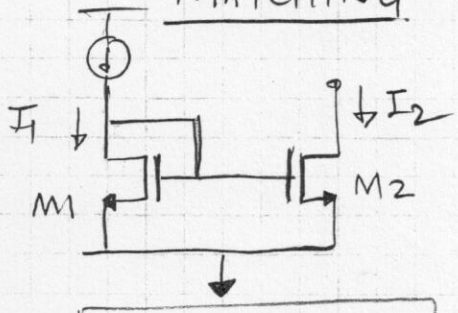
MATCHING CONSIDERATIONS



$$\beta = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)$$

$$I_1 = \beta_1 (V_{GS} - V_{T_1})^2 (1 + \lambda V_{DS_1})$$

$$I_2 = \beta_2 (V_{GS} - V_{T_2})^2 (1 + \lambda V_{DS_2})$$

Variat^n μ_n, C_{ox}, W, L, V_T

$$\frac{I_2}{I_1} = \frac{\beta_2}{\beta_1}$$

(assume all else equal)

Incremental analysis

$$\Delta\beta = \beta_2 - \beta_1$$

$$\beta = \frac{\beta_1 + \beta_2}{2}$$

$$\beta_1 = \beta - \frac{\Delta\beta}{2}$$

$$\beta_2 = \beta + \frac{\Delta\beta}{2}$$

$$I_2 = \frac{\left(\beta + \frac{\Delta\beta}{2}\right)}{\left(\beta - \frac{\Delta\beta}{2}\right)} I_1 = \frac{\left(1 + \frac{\Delta\beta}{2\beta}\right)}{\left(1 - \frac{\Delta\beta}{2\beta}\right)} I_1 \simeq \left(1 + \frac{\Delta\beta}{\beta}\right) I$$

Large β → large $\frac{W}{L}$ → smaller mismatch

V_T variations

$$V_{T_1} = V_T\left(1 + \frac{\Delta V_T}{2V_T}\right); \quad V_{T_2} = V_T\left(1 - \frac{\Delta V_T}{2V_T}\right)$$

$$\frac{I_2}{I_1} = \frac{(V_{GS} - V_{T_2})^2}{(V_{GS} - V_{T_1})^2} = \frac{\left(V_{GS} - V_T + \frac{\Delta V_T}{2}\right)^2}{\left(V_{GS} - V_T - \frac{\Delta V_T}{2}\right)^2}$$

$$= \frac{\left(1 + \frac{\Delta V_T}{2(V_{GS} - V_T)}\right)^2}{\left(1 - \frac{\Delta V_T}{2(V_{GS} - V_T)}\right)^2} = \left(1 + \frac{\Delta V_T}{(V_{GS} - V_T)}\right)\left(1 + \frac{\Delta V_T}{(V_{GS} - V_T)}\right)$$

$$= \left[1 + \frac{2\Delta V_T}{(V_{GS} - V_T)}\right]$$

To reduce mismatches increase $(V_{GS} - V_T)$ or Vdsat

Tradeoff with o/p swing

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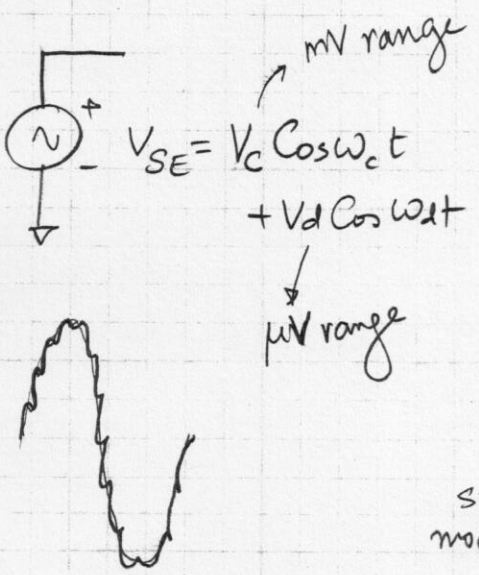
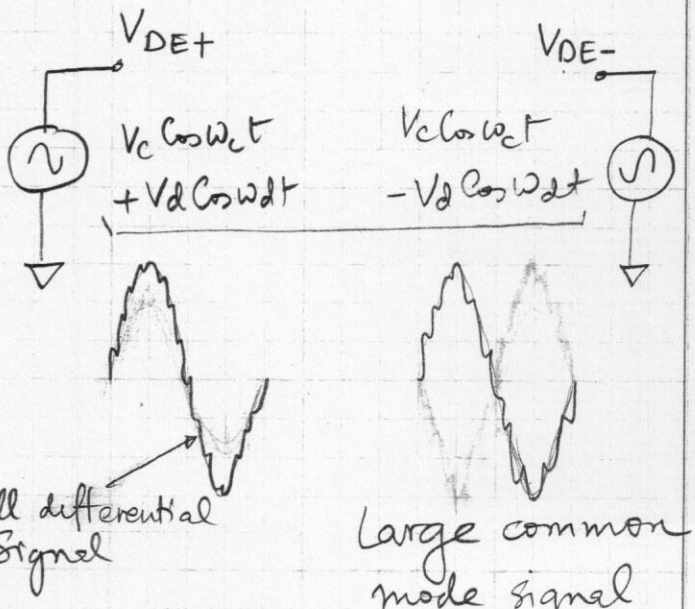
NEW TOPIC DIFFERENTIAL AMPLIFIERS

Why differential amplifier ?

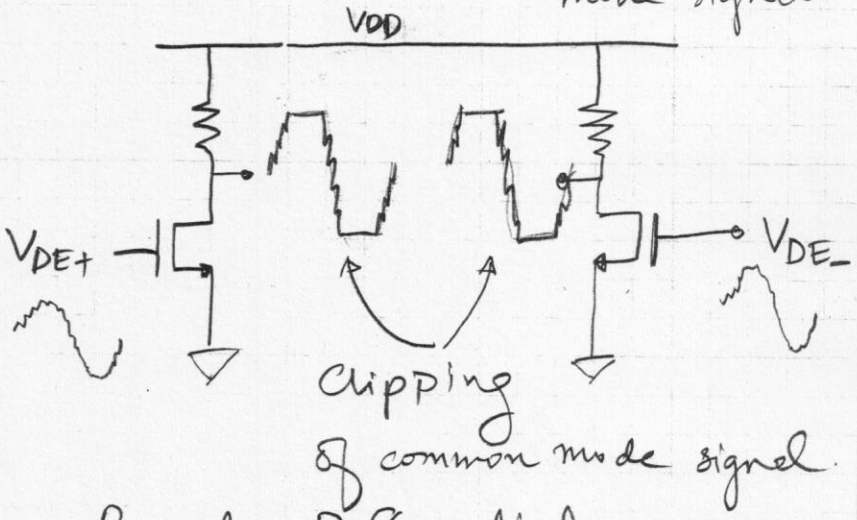
- Example – ECG
  - Detecting very small signal in presence of very large signal
  - Understanding whisper in presence of screaming voice
  - Difference Amplifier

Single Ended & Differential Signal




V_{DE+}
V_{DE-}
$V_c \cos\omega_c t + V_d \cos\omega_d t$
$V_c \cos\omega_c t - V_d \cos\omega_d t$
small differential mode signal
Large common mode signal

Large common mode signal could be 50 Hz Supply hum, – common mode coupling



VDD – Noise

Psuedo – Differential

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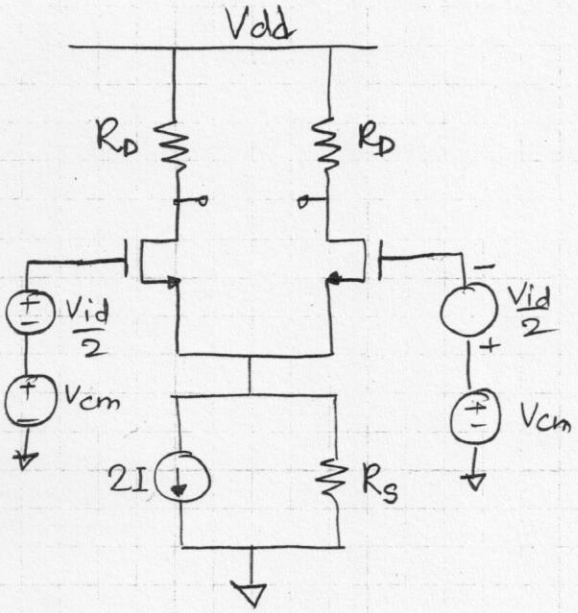
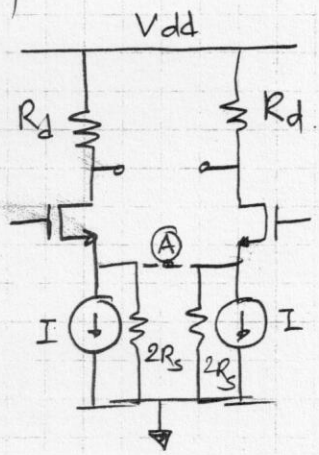


Goal

Large Differential gain
A_{dm}

Small Common-mode gain
A_{cm}
(over large range of V_{cm})

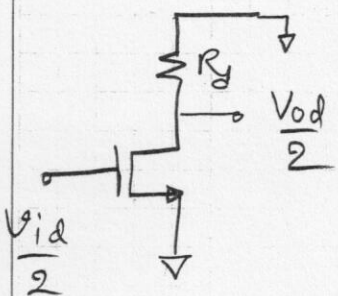
Symmetric Half Ckt



For differential i/p, — NO ac small signal V_{cm} is applied
(only DC V_{cm} bias)

(A) → Virtual ground

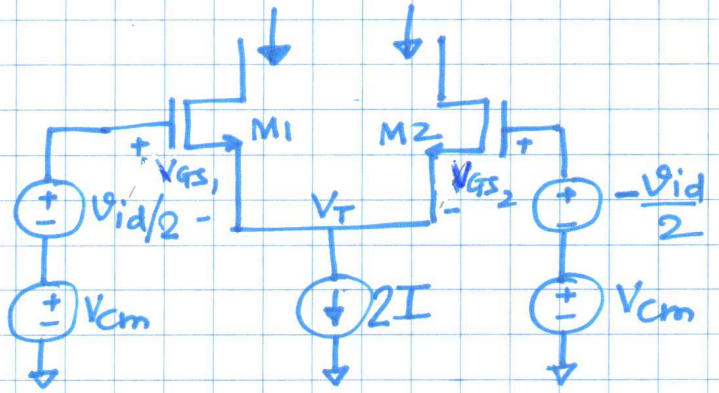
Half ckt analysis



$$A_{dm} = \frac{-g_{m_1}}{g_{ds_1} + \frac{1}{R_d}} = \frac{-g_m R_d}{1 + g_{ds} R_d}$$

Differential Pair Virtual Ground Concept

$I+\Delta i$ $\quad$ $I-\Delta i$ $\quad\leftrightarrow\quad (I+\Delta i)+(I-\Delta i)=2I$ (KCL)



Valid only for differential inputs

Assume V_{GS_1} & V_{GS_2} have equilibrium value of V_{eq}. They change by ΔV_{GS_1} & ΔV_{GS_2} on application of differential signal v_{id}.

Since the circuit is linearized around operating pt.

$(I+\Delta i)+(I-\Delta i)=2I \;\rightarrow\; I_1+I_2=2I$

$g_m\Delta V_{GS_1}+g_m\Delta V_{GS_2}=0 \;\leftarrow$

$$\Rightarrow \Delta V_{GS_1}=-\Delta V_{GS_2} \qquad \text{—①}$$

KVL $\quad V_{cm}+\frac{v_{id}}{2}-\Delta V_{GS_1}-V_{eq}=V_T=V_{cm}-\frac{v_{id}}{2}-\Delta V_{GS_2}-V_{eq}$

$$\Rightarrow \Delta V_{GS_1}-\Delta V_{GS_2}=v_{id} \qquad \text{—②}$$

FROM ① & ② V_T doesn't change.

Differential signal v_{id} is consumed by V_{GS_1} & V_{GS_2}. V_T doesn't change.

Hence Virtual Ground.

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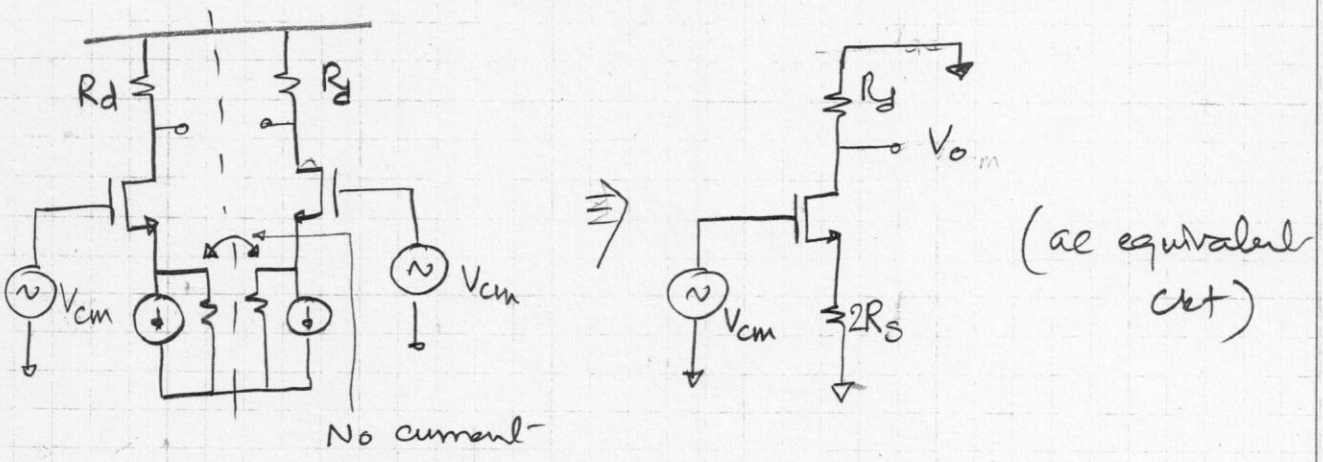
For common mode i/p $v_{id} = 0$, AC current @ V_{cm}



PROVE: $$A_{cm} = \frac{-g_m r_o R_d}{R_d + r_o + 2R_s\left(1 + (g_m + g_{mbs}) r_o\right)}$$

approximating

$$A_{cm} \cong -\frac{g_m r_o R_d}{2R_s g_m r_o} = -\frac{R_d}{2R_s}$$

CMMR - common mode rejection ratio

$$= 20 \log \left| \frac{A_{dm}}{A_{cm}} \right| = 20 \log \left| \frac{g_m R_d r_o \cdot 2R_s}{(r_o + R_d) R_d} \right|$$

$$= 20 \log \left(\frac{2(g_m r_o) R_s}{(r_o + R_d)} \right)$$

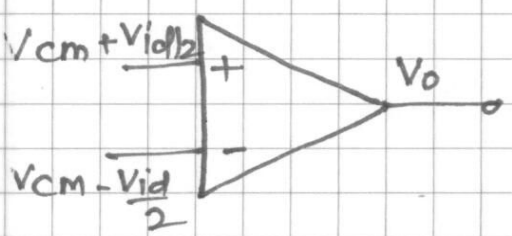
In CMOS implementation $R_d = r_o$ (PMOS)

$$= 20 \log (g_m R_s)$$ ← current source o/p resistance as high as possible

$$g_m R_s = \frac{2I}{(V_{GS} - V_T)} \cdot \frac{V_A}{I} = \frac{2V_A}{(V_{dsat})}$$ ← Early voltage, current src, diff pair.

Current source quality → CMRR

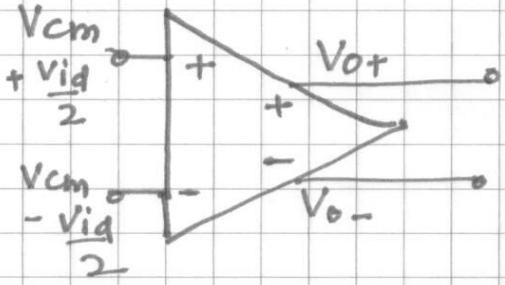
About COMMON-MODE REJECTION.



$$\underbrace{A_{cm} \cdot V_{cm}}_{\text{undesired}} + \underbrace{A_{dm} \cdot V_{id}}_{\text{Desired}}$$

$$CMRR = 20 \log \left| \frac{A_{dm}}{A_{cm}} \right|.$$

Consider amplifier with differential outputs



$$A_{cm} \cdot V_{cm} + A_{dm} \frac{V_{id}}{2} + A_{CMDM}(V_{cm})$$

$$A_{cm} \cdot V_{cm} + A_{dm}\left(-\frac{V_{id}}{2}\right) + A_{CMDM}(-V_{cm})$$

Desired.

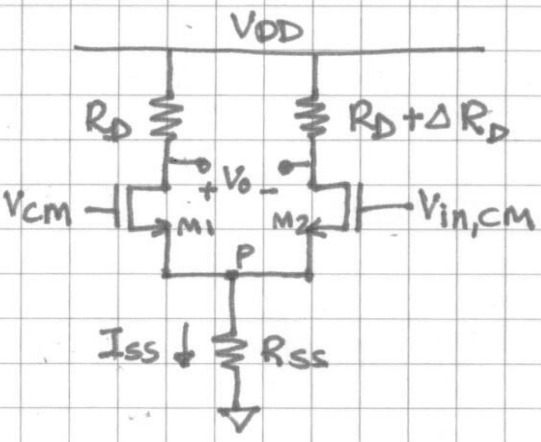
* Will be rejected by Next Diff Amp
* Only changes bias points
  → may alter small signal gain
* Can limit output voltage swing

Common-Mode to Diff. mode conversion

* Corrupts desired differential signal
* Due to ~~Asst~~ Asymmetry due to Mismatches
* Frequency dependent effects.

  Example: High frequency CM → Modifies tail current source ← parasitic cap across tail current.

Example ACM-DM. due to mismatch.



SF concept

$$\Delta V_p = \frac{R_{ss}}{R_{ss} + 1/2g_m}\Delta V_{in,cm} = \frac{2g_m R_{ss}}{1+2g_m R_{ss}}\Delta V_{in,cm}$$

$$\Delta I_{ss} = \frac{2g_m R_{ss}}{1+2g_m R_{ss}} \cdot \frac{\Delta V_{in,cm}}{R_{ss}}$$

↑ Splits equally on both sides

$$\Delta I_{D_1} = \Delta I_{D_2} = \frac{g_m}{1+2g_m R_{ss}}\Delta V_{in,cm}$$

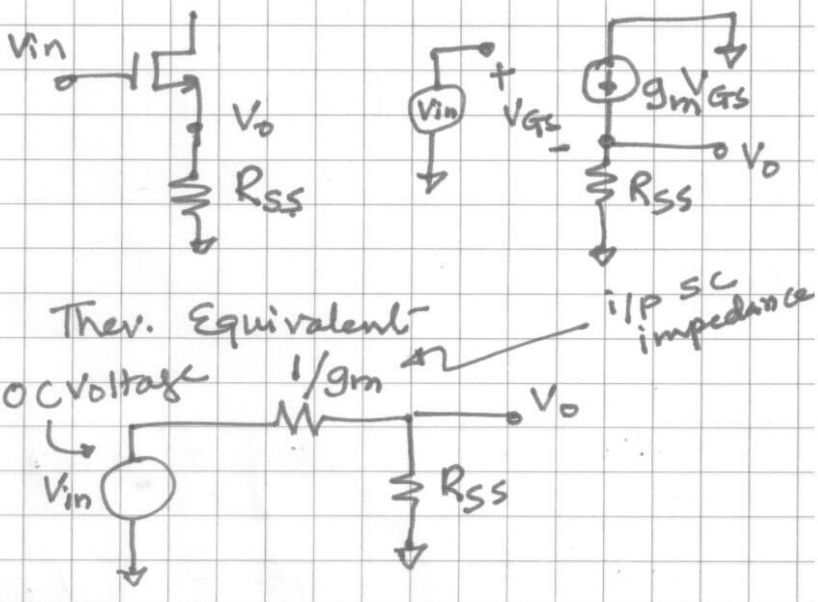
$$\Delta V_{out_{CM-DM}} = -\Delta I_{D_1} R_D - \left[-\Delta I_{D_2}(R_D+\Delta R_D)\right]$$

$$= \Delta I_D \cdot \Delta R_D = \frac{g_m \Delta R_D}{1+2g_m R_{ss}}\Delta V_{in,CM}.$$

$$\therefore A_{CM-DM} = \frac{g_m \Delta R_D}{1+2g_m R_{ss}}.$$

Side Note

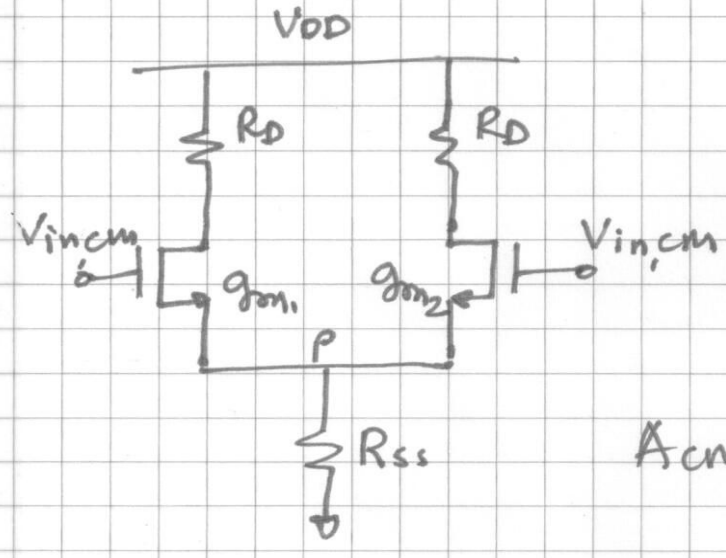
Source Follower



$$\frac{V_o}{V_{in}} = \frac{R_{ss}}{R_{ss} + 1/g_m}.$$

Insight. R_{SS} → Current Source output impedance

R_{SS} should be large to achieve good CMRR.



$g_{m_1} \neq g_{m_2}$ (mismatches)

↪ HW prove.

$$A_{CM-DM} = -\frac{\Delta g_m R_D}{1 + (g_{m_1} + g_{m_2}) R_{SS}}$$

R_{SS} - current source o/p impedance.

For a fully differential circuit:
Input and output both are differential

$$CMRR = \left| \frac{A_{DM}}{A_{CM-DM}} \right|$$

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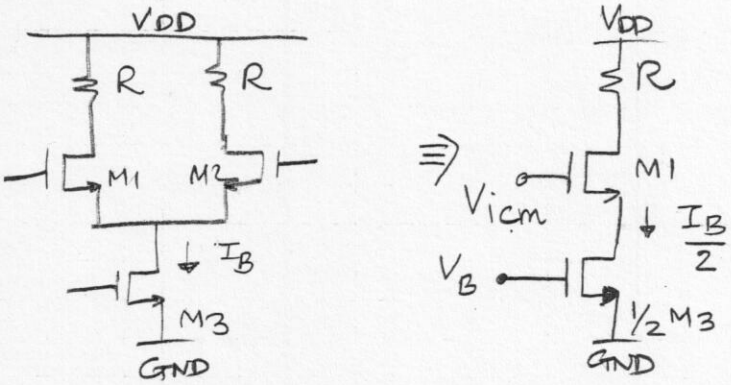
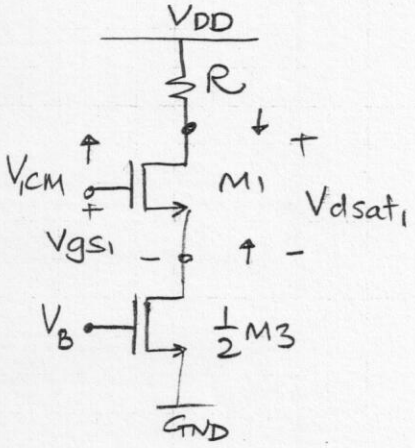
Common-mode Range CMR

– Range of common-mode input voltages for which all devices are in saturation.



Calculating $V_{icm}(max)$



$V_{icm}(max)$ when M1 enters non-sat

$$V_{icm}(max) - V_{gs1} = V_{DD} - \frac{I_B R}{2} - V_{dsat1}$$

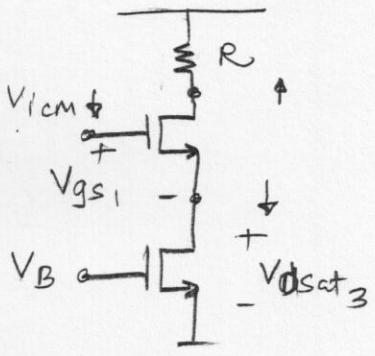
$$V_{icm}(max) = V_{DD} - \frac{I_B R}{2} + V_{gs1} - V_{dsat1}$$

$$= V_{DD} - \frac{I_B R}{2} + V_{T1}$$

DC drop across R.

Typ $V_{icm}(max) = (V_{DD} - V_{dsat})$ [↑ can be larger than V_{DD}]

Calculating $V_{icm}(min)$



$V_{icm}(max)$ – when M3 enters non-sat

$$V_{icm}(min) = V_{gs1} + V_{dsat3}$$

$$= V_{T1} + V_{dsat1} + V_{dsat3}$$

$$\approx V_T + 2V_{dsat}$$

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Example $V_{DD} = 1.8V$ $V_{TN} = 0.5V$ $V_{Tp} = -0.6V$

$V_{dsat} \approx 150mV$

For nmos diff pair – amplifier

$V_{icm(max)} = V_{DD} - V_{dsat} \cong 1.8V - 0.15 = 1.65V$

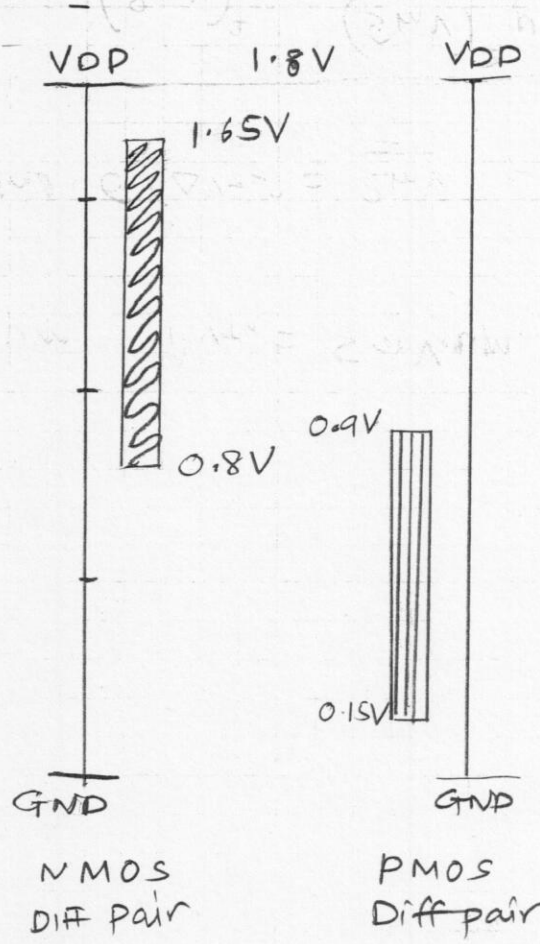
$V_{icm(min)} = V_T + 2V_{dsat} = 0.5V + 0.3V = 0.8V$

For pmos diff pair – amplifier

(-ve dirⁿ) $V_{icm(max)} = 0 + 0.15V = 0.15V$

$V_{icm(min)} = V_{DD} - (V_T + 2V_{dsat}) = 1.8 - (0.6 + 0.3V)$

$= 0.9V.$



For Rail-to-Rail (V_{DD} – GND) V_{ICM}, smart combination of NMOS – PMOS diff pair is used.

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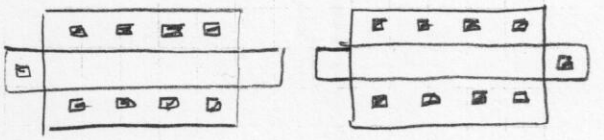
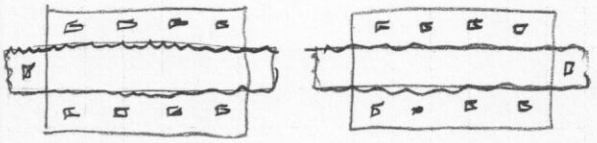
INTRODUCTION TO MISMATCHES



Diff pair transistors (layout tool)



After processing

jagged edges

Random variations. ΔW, ΔL

Intuitively as W & L ↑ Relative mismatch $\frac{\Delta W}{W}, \frac{\Delta L}{L}$ ↓

Mismatches decrease as area of transistor (WL) increases

— example — Breakup transistor in small pieces

→ averaging effect

→ Can be extended to other device parameters also.

$$\sigma(\Delta V_{TH}) = \frac{A_{VTH}}{\sqrt{WL}}$$

$$\sigma^2(\Delta V_{TH}) = \frac{A_{VTH}^2}{WL}$$

(variance)

A_{VTH} (mV μm)

$\cong 5$ (0.18μm process)

[=30 → 2.5μm]

$$\sigma\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta}{\sqrt{WL}}$$

$$\sigma^2\left(\frac{\Delta\beta}{\beta}\right)^2 = \frac{A_\beta}{WL}$$

(variance)

$A_\beta \Rightarrow$ (% μm)

$\cong 1$ (0.18μm proces)

[2.5 → 2.5μm]

good references

- measured values.
- Theory in Pelgrom – JSSC OCT 89
- Lakshmi kumar – JSSC Dec 86
- Kinget – JSSC June 2005

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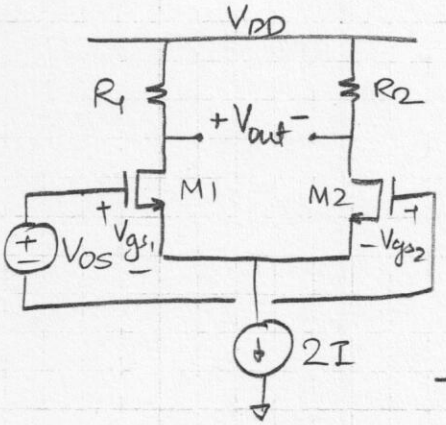
Effect of Mismatches

Allstot Razavi 14.2.1



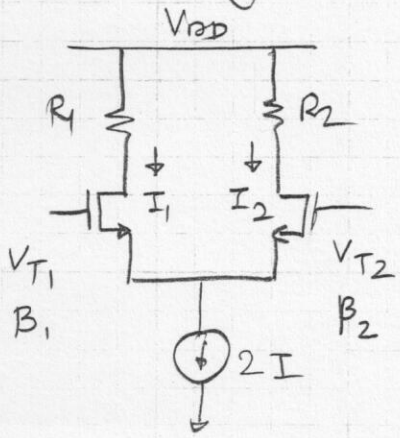
Input referred offset voltage

V_{os} = i/p DC voltage required to make $V_{out} = 0$

→ Systematic offset – Bad design practices → $\left(\frac{W}{L}\right)_1 \neq \left(\frac{W}{L}\right)_2$ or $R_1 \neq R_2$

→ Random offsets — process variations

Calculating Offset voltage



$$I_1 R_1 = I_2 R_2$$

$$V_{os} = V_{GS_1} - V_{GS_2}$$

$$= V_{T_1} + \sqrt{\frac{I_1}{\beta_1}} - V_{T_2} - \sqrt{\frac{I_2}{\beta_2}}$$

Incremental analysis

avg quantity $X = \frac{X_1 + X_2}{2}$

$X_1 = X + \frac{\Delta X}{2}$

$X_2 = X - \frac{\Delta X}{2}$

apply this to I, R, V_T, β

$$V_{T_1} = V_T + \frac{\Delta V_T}{2} \qquad \beta_1 = \beta + \frac{\Delta\beta}{2} \qquad R_1 = R + \frac{\Delta R}{2}$$

$$V_{T_2} = V_T - \frac{\Delta V_T}{2} \qquad \beta_2 = \beta - \frac{\Delta\beta}{2} \qquad R_2 = R - \frac{\Delta R}{2}$$

$$I_1 = I + \frac{\Delta I}{2}$$

$$I_2 = I - \frac{\Delta I}{2}$$

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$$V_{OS} = V_{T1} - V_{T2} + \sqrt{\frac{I_1}{\beta_1}} - \sqrt{\frac{I_2}{\beta_2}}$$

$$= \Delta V_T + \sqrt{\frac{I}{\beta}}\sqrt{\frac{1+\Delta I/2I}{1+\Delta\beta/2\beta}} - \sqrt{\frac{I}{\beta}}\sqrt{\frac{1-\Delta I/2I}{1-\Delta\beta/2\beta}}$$

$$= \Delta V_T + \sqrt{\frac{I}{\beta}}\left[\left(1+\frac{\Delta I}{4I}-\frac{\Delta\beta}{4\beta}\cdots\right)-\left(1-\frac{\Delta I}{4I}+\frac{\Delta\beta}{4\beta}\cdots\right)\right]$$

$$= \Delta V_T + \sqrt{\frac{I}{\beta}}\left(\frac{\Delta I}{2I}-\frac{\Delta\beta}{2\beta}\right)$$

Random quantities - Rms sum all (+)

$$V_{OS} \simeq \Delta V_T + \sqrt{\frac{I}{\beta}}\left(\frac{\Delta I}{2I}+\frac{\Delta\beta}{2\beta}\right) = \Delta V_T + \frac{2I}{g_m}\left(\frac{\Delta I}{2I}+\frac{\Delta\beta}{\beta}\right)$$

$$= \Delta V_T + (V_{GS}-V_T)\left(\frac{\Delta I}{2I}+\frac{\Delta\beta}{2\beta}\right)$$

$$I_1R_1 = I_2R_2 \Rightarrow \left(I+\frac{\Delta I}{2}\right)\left(R+\frac{\Delta R}{2}\right) = \left(I-\frac{\Delta I}{2}\right)\left(R-\frac{\Delta R}{2}\right)$$

$$IR\left(1+\frac{\Delta I}{2I}\right)\left(1+\frac{\Delta R}{2R}\right) = IR\left(1-\frac{\Delta I}{2I}\right)\left(1-\frac{\Delta R}{2R}\right)$$

$$1+\frac{\Delta I}{2I}+\frac{\Delta R}{2R} \simeq 1-\frac{\Delta I}{2I}-\frac{\Delta R}{2R} \Rightarrow \frac{\Delta I}{I} = \frac{\Delta R}{R}$$

$$V_{OS} \simeq \Delta V_T + \frac{2I}{g_m}\left(\frac{\Delta R}{R}+\frac{\Delta\beta}{\beta}\right)$$

$\sigma(V_{OS})^2 = (\ )^2 + (\ )^2 + (\ )^2$

Taking to the next level $\frac{\Delta\beta}{\beta} = \frac{\Delta K'}{K'} + \frac{\Delta W}{W} + \frac{\Delta L}{L}$

$$\frac{\Delta R}{R} = \frac{\Delta\rho_\square}{\rho_\square} + \frac{\Delta L}{L} + \frac{\Delta W}{W}$$

W & L of Resistor

sheet R

→ Many terms contribute to offsets.

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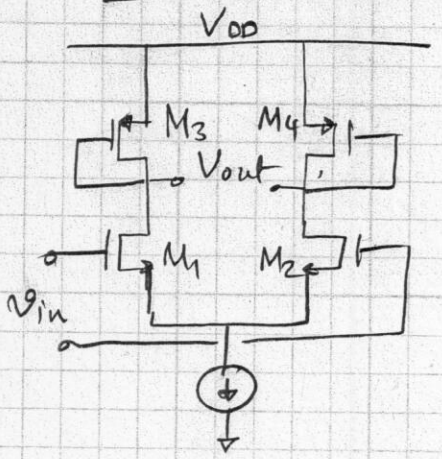
Back to Diff Pair

MOS Load instead of R load.

Diode PMOS load



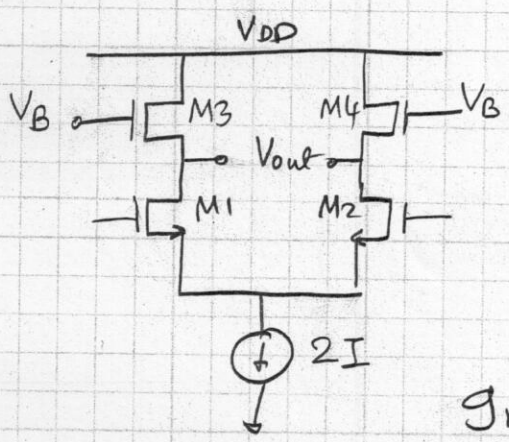
Voltage gain

$$A_v = -\frac{g_{mN}}{g_{mp} + g_{dsN} + g_{dsp}}$$

$$A_v \cong -\frac{g_{mN}}{g_{mp}}$$

$$A_v = -\sqrt{\frac{\mu_n (W/L)_N}{\mu_p (W/L)_P}}$$ (Low value)

Current Source PMOS LOAD



Voltage Gain

$$A_v = \frac{-g_{mN}}{(g_{dsN} + g_{dsp})}$$ High

$$g_{mN} = \frac{2I}{(V_{GS} - V_T)_N}$$

$$g_{dsN} = \lambda_N I$$

$$g_{dsp} = \lambda_P I$$

$$A_v = \frac{2}{(V_{GS} - V_T)_N} \cdot \frac{1}{(\lambda_N + \lambda_P)}$$ ← decided by channel length for NMOS PMOS

$(V_{GS} - V_T)_N$ ↓ 0.15V

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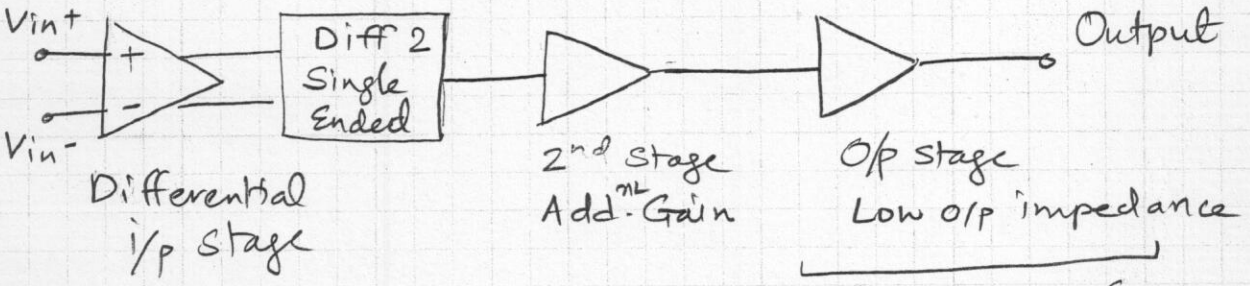
OPERATIONAL AMPLIFIERS

- Basic building block
- High gain differential Amplifier
- A very high V. (Voltage) gain (need not be accurate)
- High input impedance
- Low output impedance

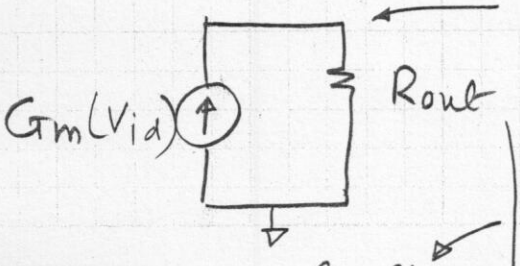
Generic Topology



OPAMP — Low o/p impedance includes final buffer stage

OTA - Operational Transconductance Amplifier
- high o/p impedance
- Current o/p

$V_{out} = [G_m R_{out}]\, V_{id}$



Most Common On-Chip

→ Can be used as voltage amplifier when driving high impedance loads.

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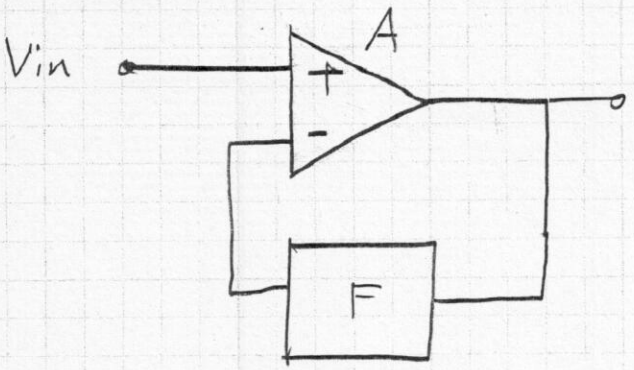
OPAMP/OTA performance Parameters

★ **Voltage Gain** — Determines precision of feedback System.

Example:



$$\frac{V_{out}}{V_{in}} = \frac{A}{1+AF} = \frac{1}{\frac{1}{A}+F} \approx \frac{1}{F}$$

A needs to be Larger than Spec.

↑ driven by desired accuracy

↓ Does not need to be accurate

F can be decided by ratio of R or Cs, — accurate vs. process, temp, voltage variations.

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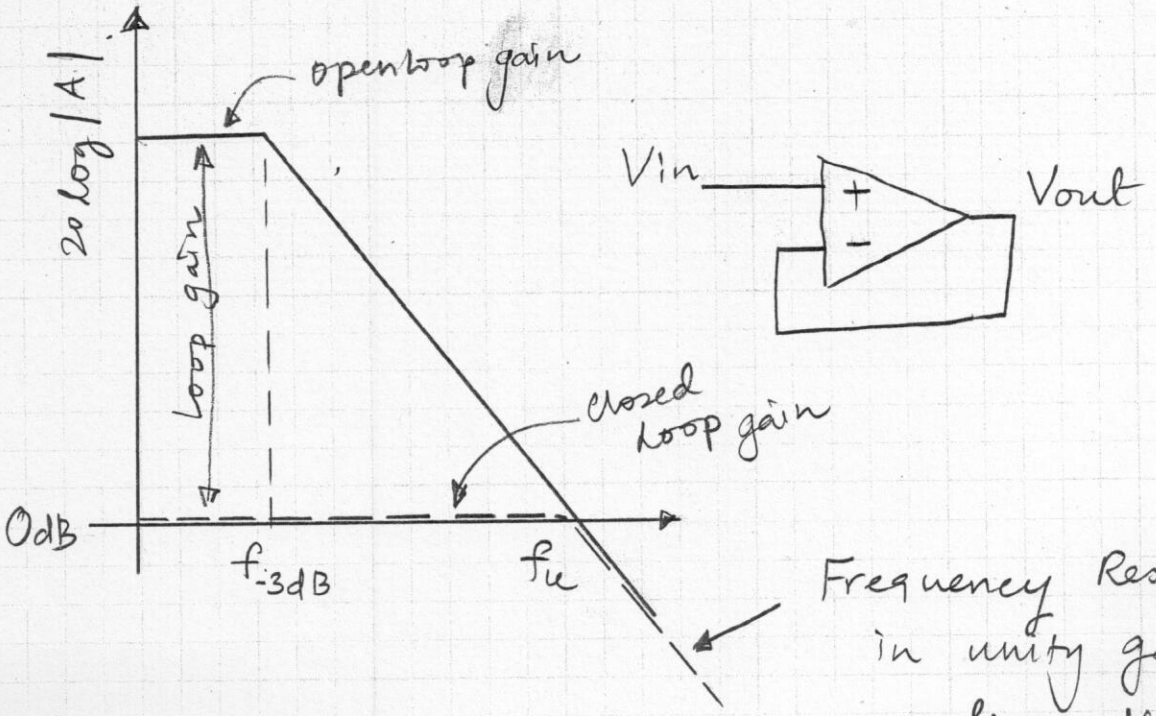
★ Small Signal BW

Open loop frequency response



→ Decides closed loop freq. response after feedback

→ Gain Margin / Phase Margin
(we will be discussing this extensively later)

→ Stability important.

★ Output swing – Large – keeping all transistors in Saturation (maintaing high ac gain)

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★ Input Common-Mode range

- i/p CMR for which all transistors are in saturation.
- NMOS - $(V_{DD} - V_{DSAT}) \leftrightarrow V_T + 2V_{DSAT}$
- PMOS - $[V_{DD} - (V_T + 2V_{DSAT})] \leftrightarrow V_{DSAT}$
- To handle Rail 2 Rail i/p
  - Combo of NMOS & PMOS. Diff i/p pair

★ Input Referred Offset

- Dominated by i/p Diff pair & load
- First Stage high gain
- Avoid systematic mismatches
- Large Device sizes to reduce random mismatches.

★ Noise - Determines minimum signal that can be accurately processed

- Similar treatment like offsets
- We will be studying this extensively.

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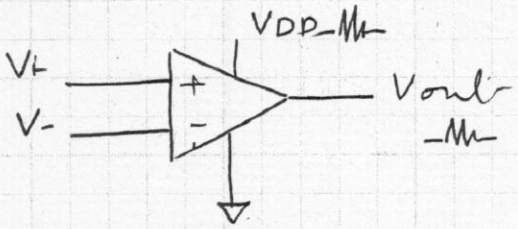
CMRR – Common-mode rejection ratio (already discussed)

PSRR – Power Supply Rejection Ratio

– How much of supply noise shows up @ o/p.

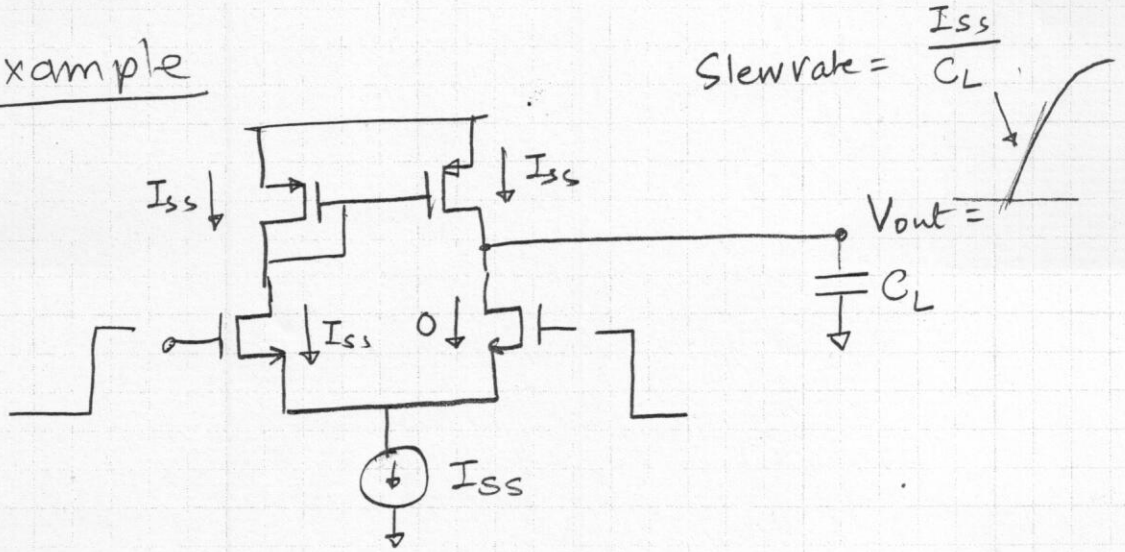


Large Signal Behavior – Slew rate

Slewing – Fastest change in the node voltage. Generally decided by

$$I/C = \frac{dV}{dt}$$

Example



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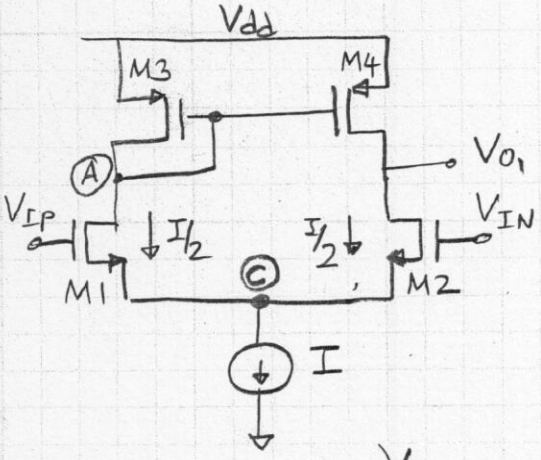
OTA Topologies

(— Allstot)



Single Stage OTA

Common-mode

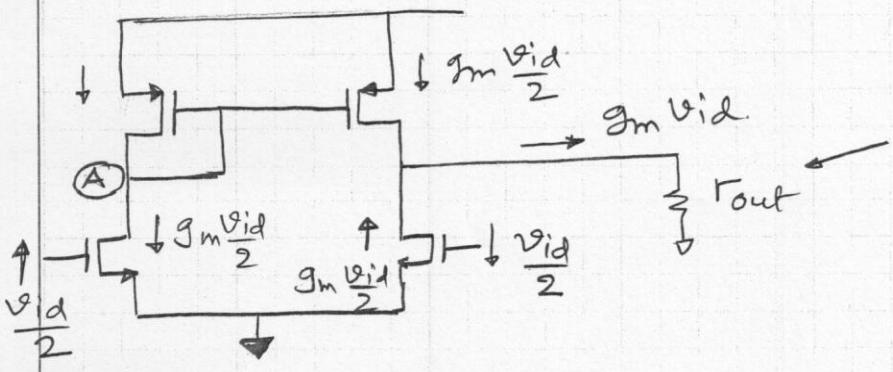
$V_{IP} = V_{IN} = V_{CM}.$ $\left(\frac{V_{dd}}{2}\right)$

Assume Feedback sets $V_{SD_3} = V_{SD_4}$

$$V_{SD_3} = V_{SD_4} = |V_{Tp}| + \sqrt{\frac{2(I/2)}{\mu_p C_{ox}\left(\frac{W}{L}\right)_p}}$$

$$V_{O_1} = V_{dd} - |V_{Tp}| - |V_{DSATp}|$$

Ac analysis — Node © — virtual ground node. for differential signal.



small signal O/P resistance $= \frac{1}{(g_{ds_2} + g_{ds_4})}$

$$V_{O_1} = \frac{g_{m_1} v_{id}}{g_{ds_2} + g_{ds_4}}$$

$$A_V = \frac{g_{m_1}}{g_{ds_2} + g_{ds_4}}$$ 25-100

$$g_{out_A} = g_{m_3} + g_{ds_3} + g_{ds_1} \approx g_{m_3}$$ — low imp. wide Bandwidth node.

Limited gain (one stage only)

D2SE included.

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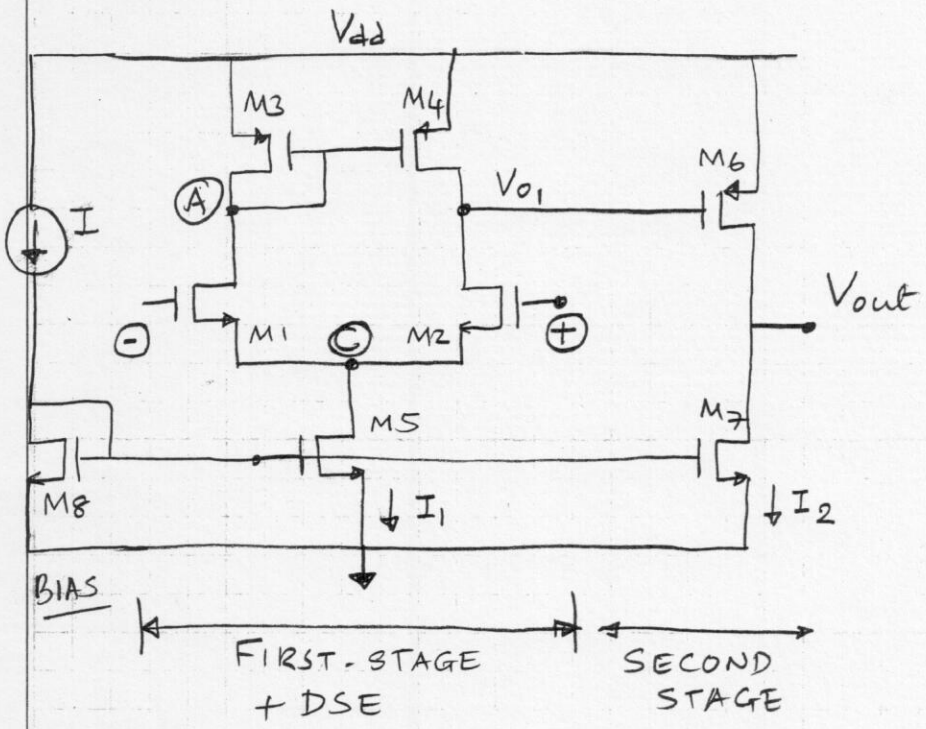
Two Stage OTA



BIASING — To avoid systematic offsets

(DC) $V_A = V_{o_1}$ $\left\{ \begin{array}{l} \text{Else} \\ V_{os} = \dfrac{V_{o_1} - V_A}{A} \end{array} \right.$ ← FIRST STAGE GAIN.

$$V_A = V_{dd} - V_{SG_3} = V_{o_1} = V_{dd} - V_{SG_6}$$

$$V_{SG_3} = V_{SG_6} \Rightarrow \text{Same } V_{dsat}.$$

$$|V_{T_3}| + \sqrt{\frac{2(I_1/2)}{\mu_p C_{ox}\left(\frac{W}{L}\right)_3}} = |V_{T_6}| + \sqrt{\frac{2(I_2)}{\mu_p C_{ox}\left(\frac{W}{L}\right)_6}}$$

Assuming $V_{T_3} = V_{T_6}$ (process matching)

$$\left(\frac{W}{L}\right)_6 = 2\left(\frac{I_2}{I_1}\right)\cdot\left(\frac{W}{L}\right)_3$$

Good design practice

Also use unit cell design – keep W same

M_3, M_4, M_6 – same L

$M_1 - M_2$ same W & L.

M_8, M_5, M_7 – same L.

$$V_{o1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} v_{id} \quad \& \quad V_{out} = \frac{g_{m6} V_{o1}}{g_{ds6} + g_{ds7}}$$

$$\text{Total gain} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} \cdot \frac{g_{m6}}{g_{ds6} + g_{ds7}}$$

↑ ↑

Each high impedance node contributes a low freq pole in frequency response

Each pole → 90° phase shift

Two poles → 180° phase shift → +ve feedback

– Limit Two gain Stages. for Stability.

– <u>Need for frequency compensation</u>

Motivation to Study Feedback & Stability

→ Then comeback & figure out frequency compensation of opamps.

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STAEDTLER Engineer's Computation Pad

Feedback & Stability

1927: Harold Black (Bell labs) — -ve feedback.

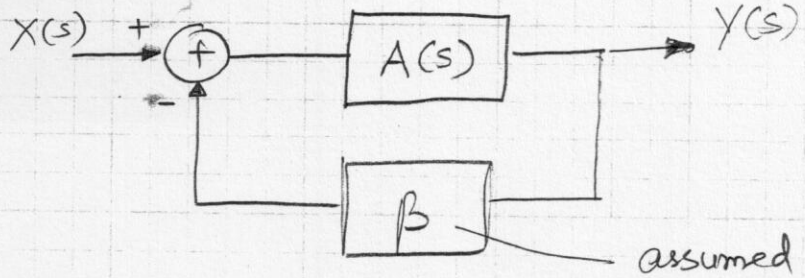
Advantages

1. Gain desensitization
2. Terminal impedance Modification
   - Shunt FB ↓ impedance
   - Series FB ↑ impedance
3. Bandwidth Modification. (increase in BW)
4. Nonlinearity reduction.

Disadvantages

1. Gain Reduction
2. Potential Instability.

Negative feedback example



$$\frac{Y(s)}{X(s)} = \frac{A(s)}{1+\beta A(s)}$$

Closed loop gain.

T = loop gain = $\beta A(s)$.

Closed loop gain goes to ∞ when $\beta A(s) = -1$

$\rightarrow |\beta A(s)| = 1$

$\rightarrow \angle \beta A(s) = -180°$.

Barkhausen's criteria for oscillation.

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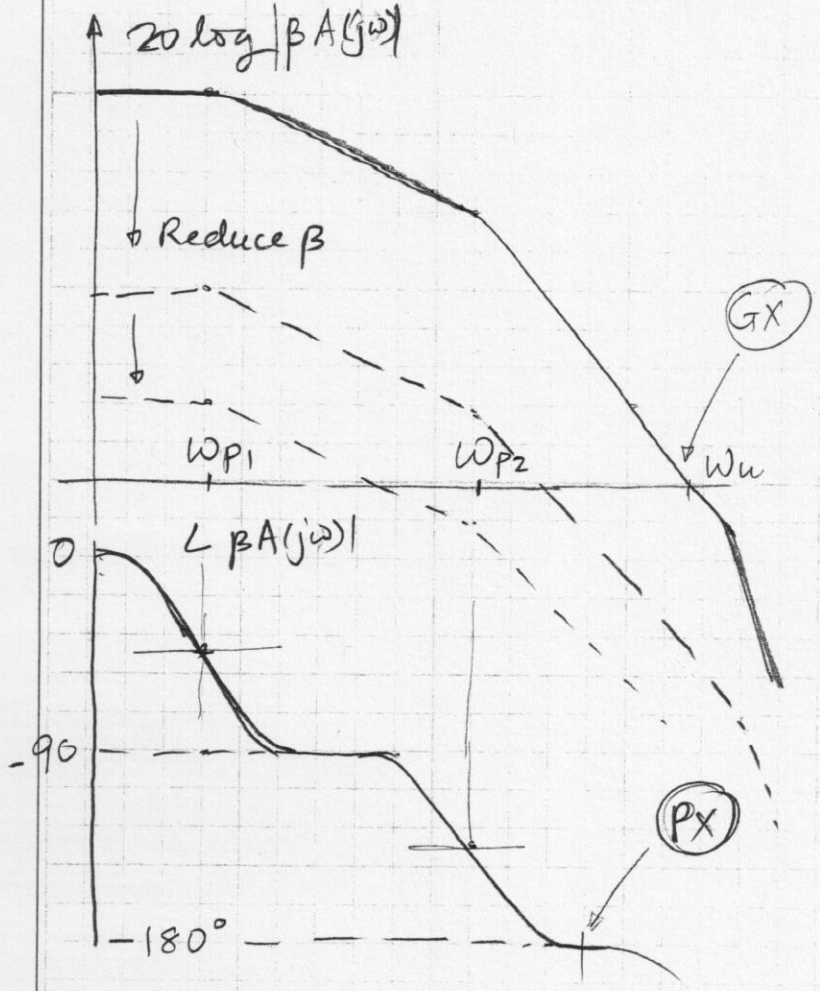
Consider Two-pole frequency response.

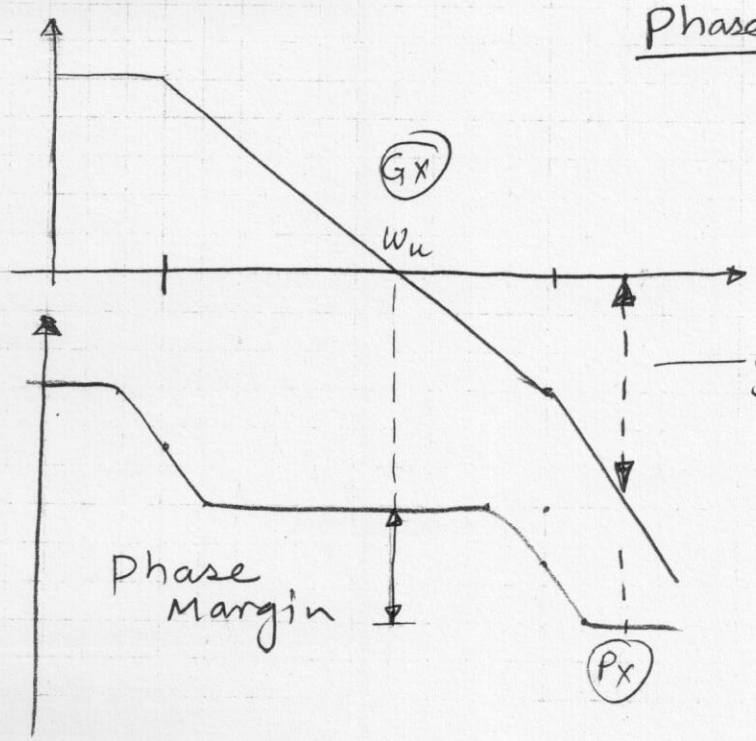


GX
Gain Crossover freq.
- Loop gain unity

PX
Phase Crossover freq.
- Loop phase shift 180°

For Stability
GX must occur before PX

Measure of Stability

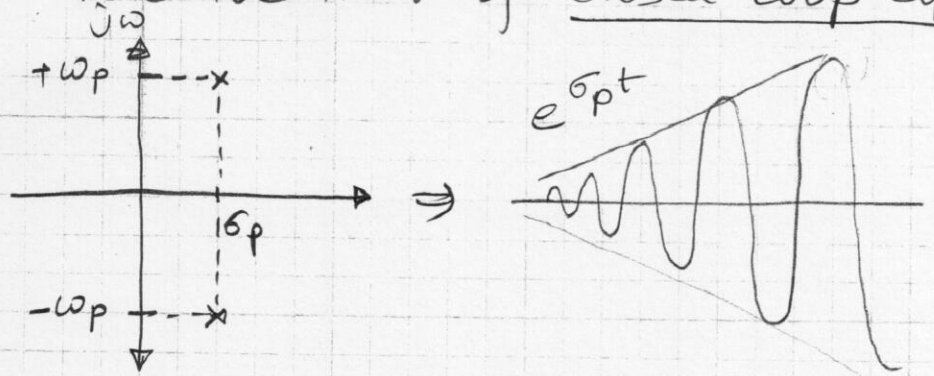


Phase Margin PM
$= 180° - \angle T(\omega_u)$
$= 60°$ (max. flat gain)
$= 70°$ (fast settling)

— Gain Margin GM

$GM = -20 \log |T(\omega_{-180°})|$
$= 12$ dB (typ).

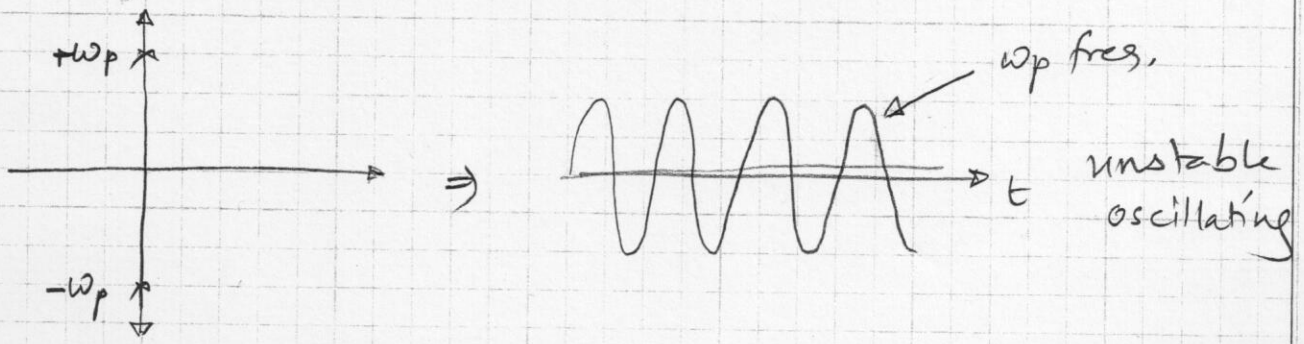
Pole location of Closed Loop System $\frac{Y(s)}{X(s)}$

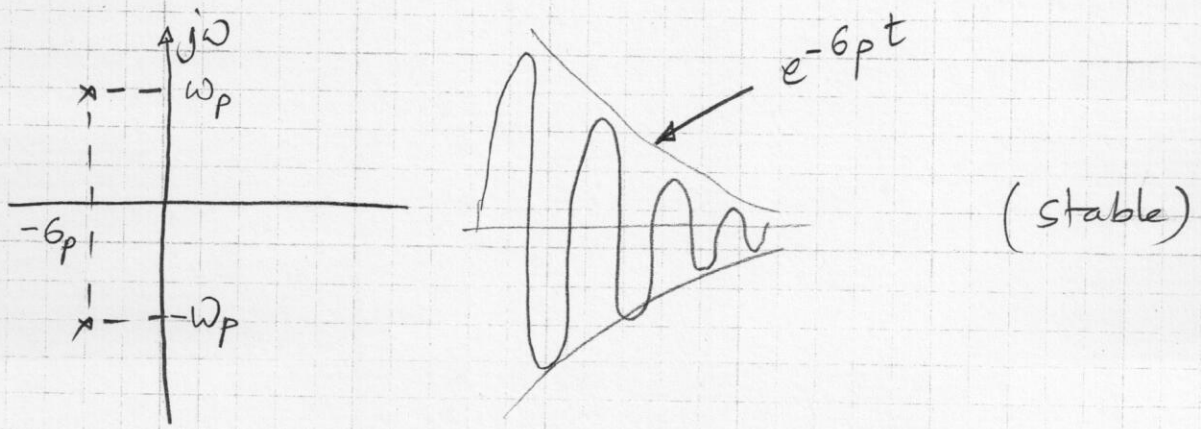


Not T(s) Loop Gain

Freq domain

Time domain





(stable)

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Example One pole amplifier

$$A(s) = \frac{A_0}{\left(1 + \frac{s}{\omega_{p_1}}\right)}$$

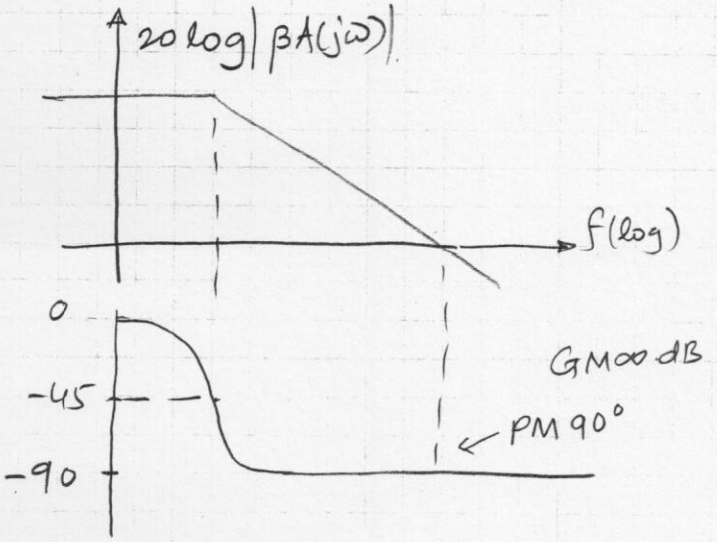
β constant

Loop Gain $T(s) = \dfrac{\beta A_0}{\left(1 + \frac{s}{\omega_{p_1}}\right)}$

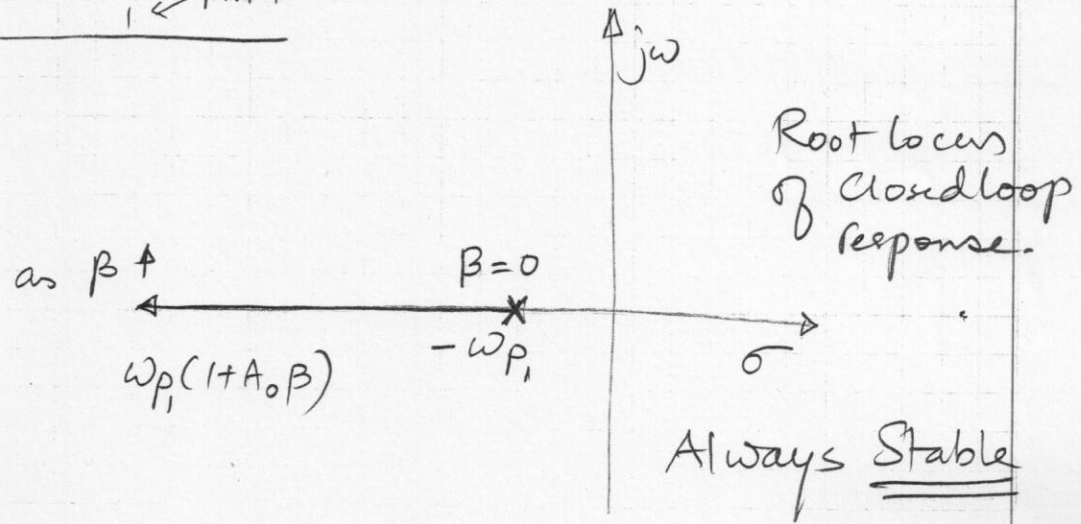
Closed loop gain

$$\frac{Y(s)}{X(s)} = \frac{\frac{A_0}{\left(1 + \frac{s}{\omega_{p_1}}\right)}}{1 + \frac{A_0\beta}{\left(1 + \frac{s}{\omega_{p_1}}\right)}} = \frac{A_0}{\left(1 + \frac{s}{\omega_{p_1}} + A_0\beta\right)}$$

$$\frac{Y(s)}{X(s)} = \frac{A_0/(1 + A_0\beta)}{1 + \frac{s}{\omega_{p_1}(1 + A_0\beta)}}$$ ← used for Root locus.



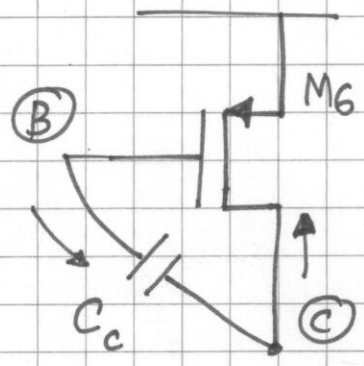
Unconditionally Stable



Root locus of closed loop response.

Always Stable

Cause of RHP Zero



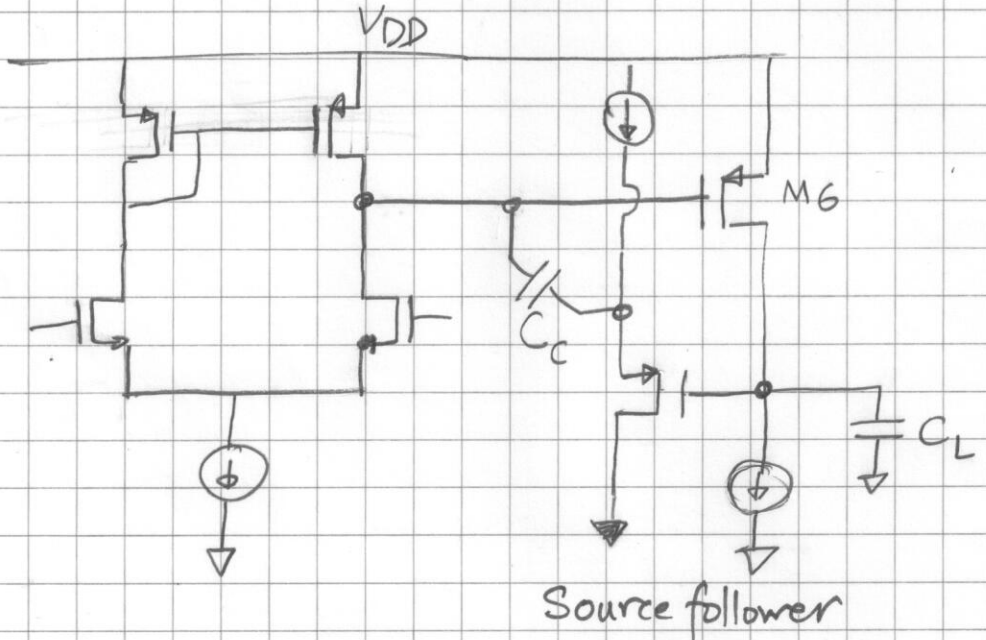
C_c around inverting stage

$\rightarrow \omega_z C_c V_B = g_{m_6} V_B$ @ zero freq.

$s \Rightarrow \omega_z = \frac{g_{m_6}}{C_c}$

→ Due to feedforward path.

Soln Remove feedforward path.

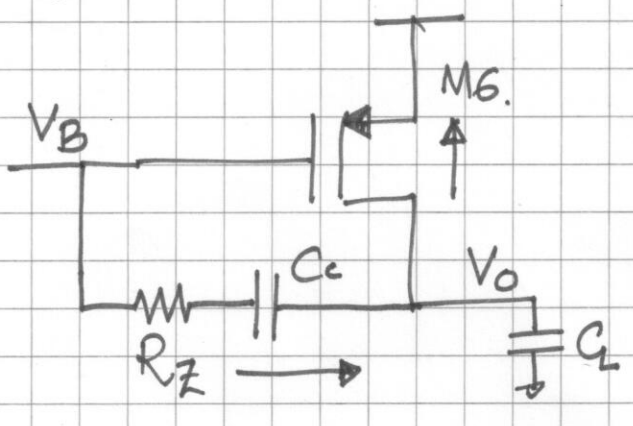


→ P_D & P_{ND} remain same as before.

⊖⊖ Power dissipation of SF.

⊖ SF frequency response. (must make sure that it doesn't deteriorate PM).

Another idea



Location of zero.

At zero freq. ω_z

$$\frac{V_B}{\left(R_z + \frac{1}{\omega_z C_c}\right)} = V_B g_{m6}$$

$$g_{m6}\left(R_z + \frac{1}{\omega_z C_c}\right) = 1$$

$$\frac{g_{m6}}{\omega_z C_c} = (1 - g_{m6} R_z) \Rightarrow \omega_z = \frac{g_{m6}/C_c}{(1 - g_{m6} R_z)}$$

When $g_{m6} R_z = 1 \Rightarrow R_z = \frac{1}{g_{m6}}$

Zero moves to ∞.

Better yet. When $g_m R_z > 1$ $\omega_z \rightarrow$ LHP zero. (-ve)

$\rightarrow$ cancel out Non-dominant pole..

$$\omega_z = \frac{g_{m6}/C_c}{(1 - g_{m6} R_z)} = -\frac{g_{m6}}{C_L}$$

(LHP Pole -ve sign.)

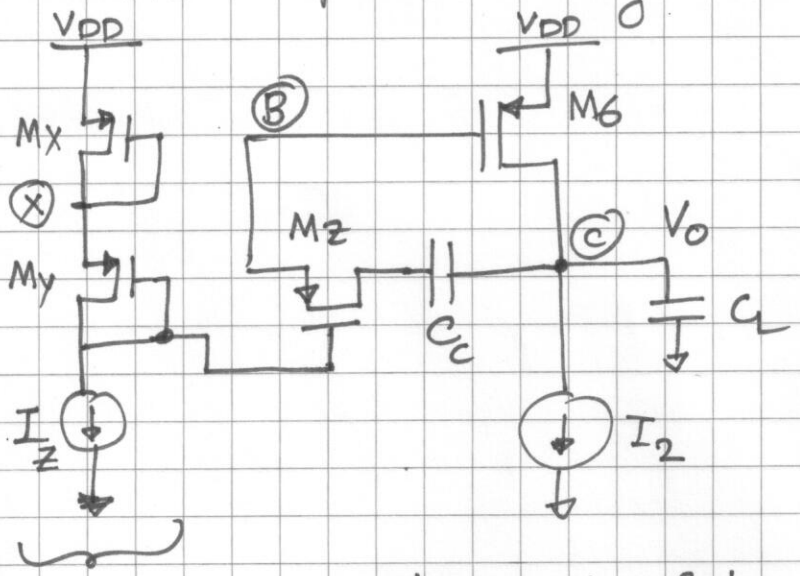
$$\frac{C_L}{C_c} = g_m R_z - 1 \Rightarrow R_z = \frac{1}{g_{m6}}\left(1 + \frac{C_L}{C_c}\right)$$

Really Cool idea!!

How do you achieve this. over PVT ?

R_z - resistor. — to track $\frac{1}{g_m}$.

R_Z → Implement using triode MOSFET.



M_Z – Non Sat.

$$I = \left[(V_{SG}-|V_{Tp}|)V_{SD} - \frac{1}{2}V_{SD}^2\right]\mu_p C_{ox}\left(\frac{W}{L}\right)_Z$$

$$R_Z = \left.\frac{1}{\partial I/\partial V_{SD}}\right|_{V_{SD}=0} = \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_Z (V_{SG}-|V_{Tp}|)_Z}$$

↖ Looks like g_m form.

By design (X) tracks (B) (DC bias)

$\Rightarrow V_{SG_X} = V_{SG_6}$ → choose I_Z & $\left(\frac{W}{L}\right)_X$

$$R_Z = \frac{1}{g_{m_6}}\left(1+\frac{C_L}{C_C}\right) = \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_Z \underbrace{(V_{SG}-|V_{Tp}|)_Z}}$$

↳ $= (V_{SG}-|V_{Tp}|)_Y$

$$\frac{\left(1+\frac{C_L}{C_C}\right)}{\mu_p C_{ox}\left(\frac{W}{L}\right)_6 (V_{SG}-|V_{Tp}|)_6} = \text{"}$$

$$\left(\frac{W}{L}\right)_Z = \left(\frac{W}{L}\right)_6 \cdot \frac{(V_{SG}-|V_{Tp}|)_6}{(V_{SG}-|V_{Tp}|)_Y} \cdot \left(\frac{C_C}{C_C+C_L}\right)$$

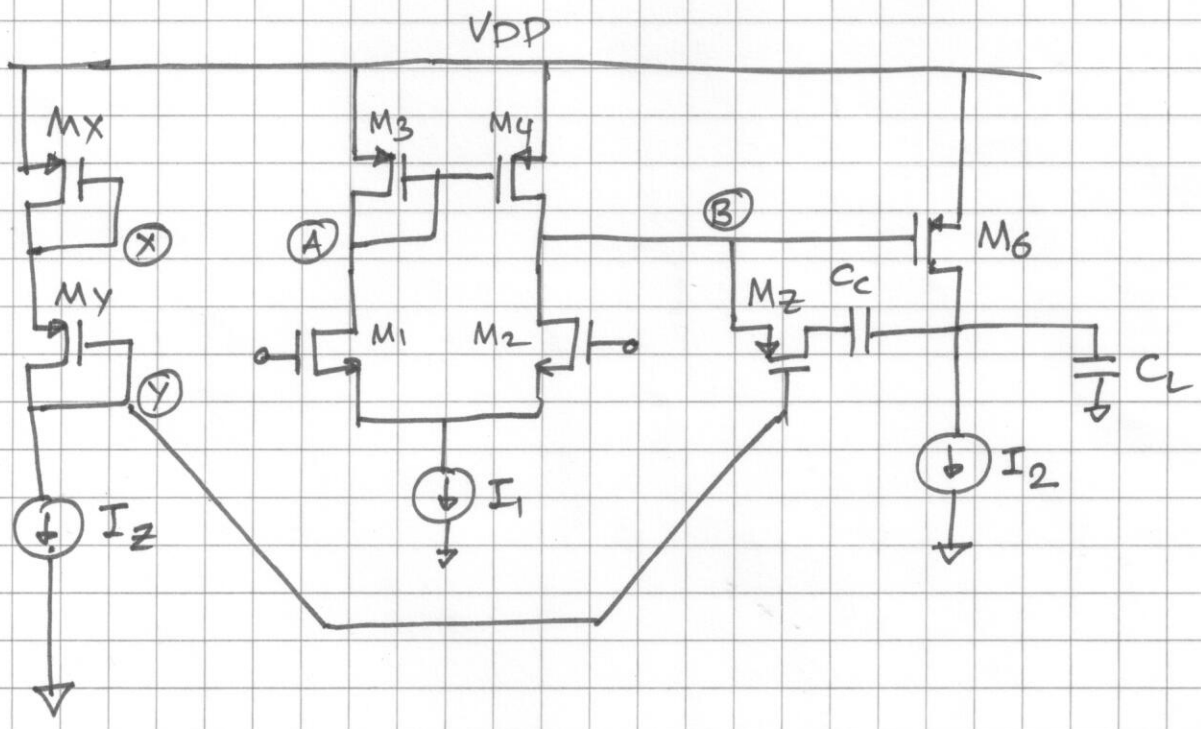
$$\left(\frac{W}{L}\right)_Z = \left(\frac{W}{L}\right)_6 \sqrt{\frac{2I_{6Q}}{\left(W/L\right)_6 \cdot \mu_p C_{ox}}} \times \sqrt{\frac{\left(\frac{W}{L}\right)_y \mu_p C_{ox}}{2I_Z}} \cdot \left(\frac{C_c}{C_c + C_L}\right)$$

$$= \sqrt{\frac{I_{6Q}}{I_Z}} \cdot \sqrt{\left(\frac{W}{L}\right)_6 \cdot \left(\frac{W}{L}\right)_y} \cdot \left(\frac{C_c}{C_c + C_L}\right)$$

→ All dependent on ratios – Not abs values

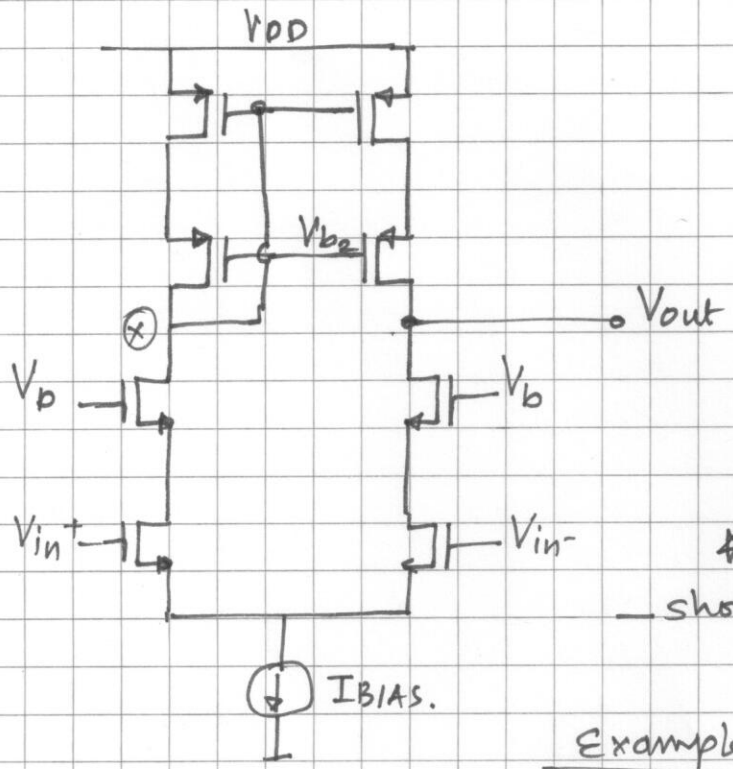
→ Tracking compensation.

* Black, Allstot, Reed. – JSSC Dec 83



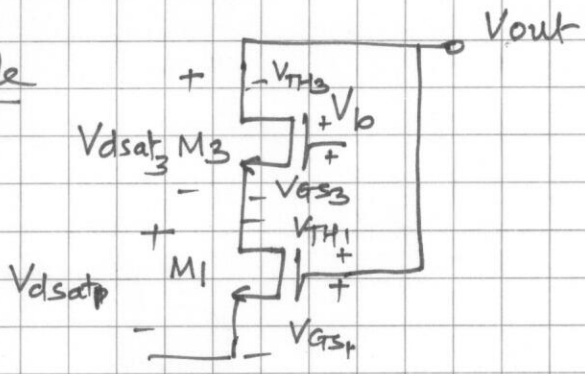
OPAMP ARCHITECTURES

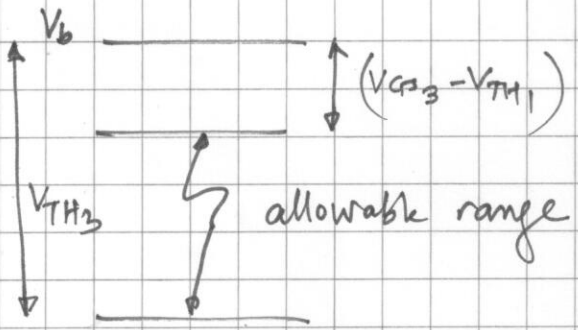
Telescopic Cascode Opamp.



* Single Stage.
  Low power - current reuse
* Limited output swing.
  $(V_{DD} - 2V_{dsat_n} - 2|V_{dsat_p}| - V_{IBIAS})$
* unity gain buffer difficult
  - shorting -ve i/p to o/p.

Example

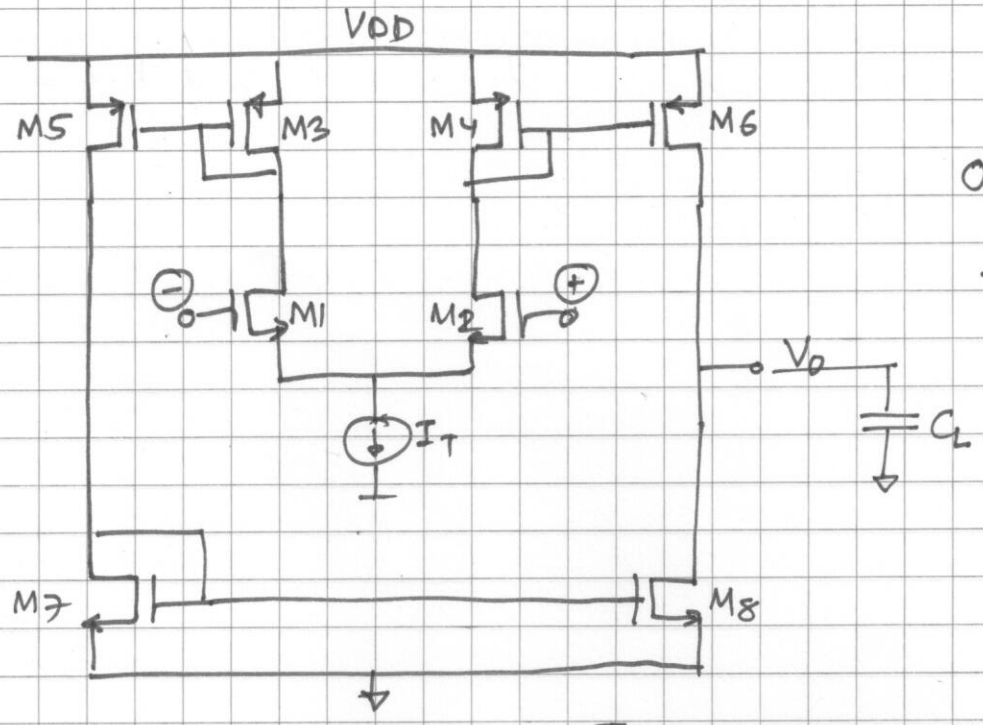




$$\text{Gain} = g_{m_N}\left[g_{m_N} r_{o_N}^2 \,\|\, g_{m_P} r_{o_P}^2\right]$$

* Mirror pole @ x

OPAMP using current mirrors



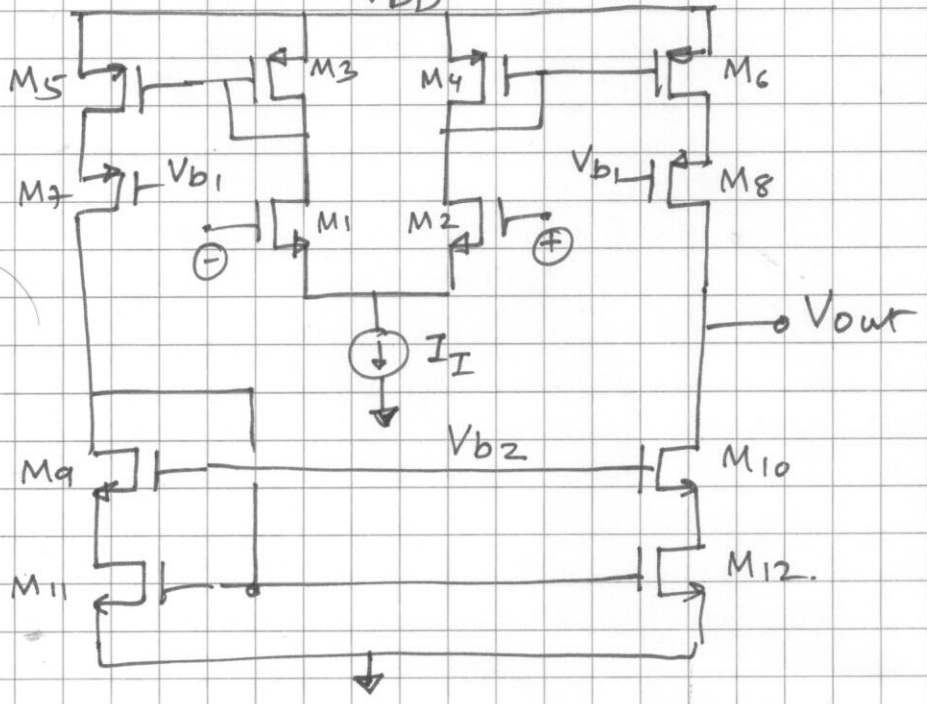
Output pole dominant - unloaded may become unstable.

Slew rate $= \frac{I_T}{C_L}$ (if all mirrors are unity gain)

$= M \frac{I_T}{C_L}$ (Mirror gain = M)

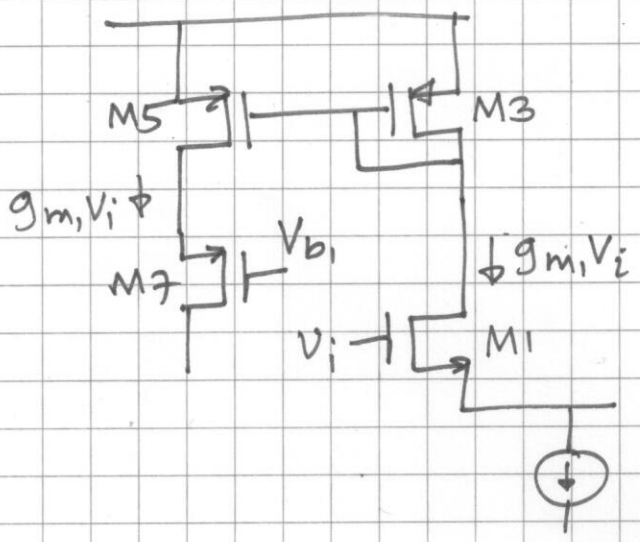
Low gain $\frac{g_m r_o}{2}$

Gain Improvement using cascodes.



Gain $\frac{(g_m r_o)^2}{2}$.

Consider PMOS mirror



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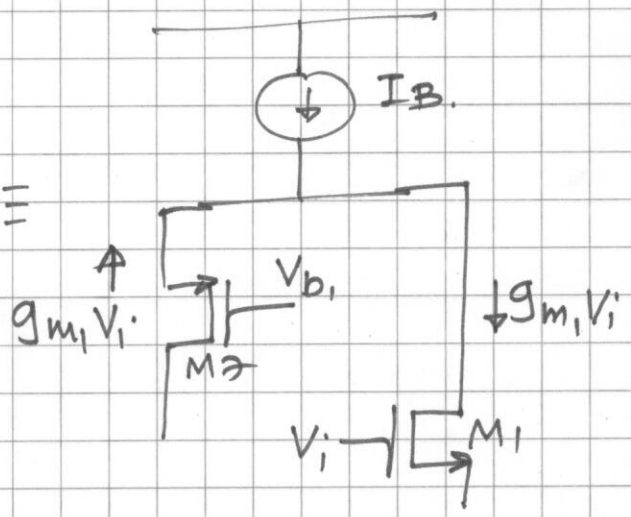
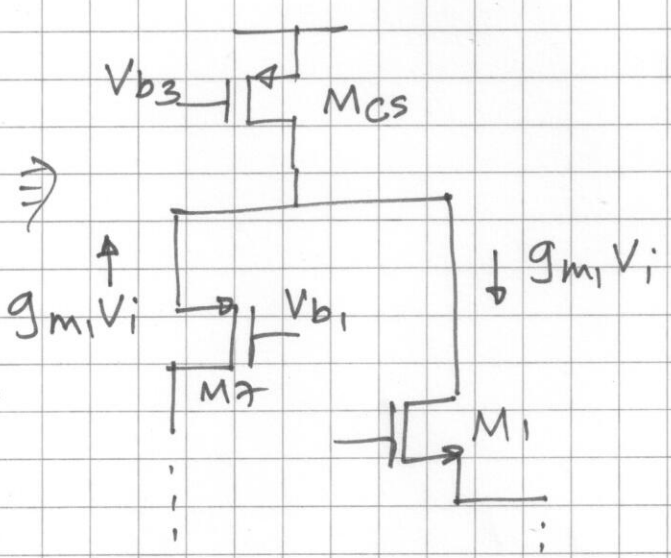


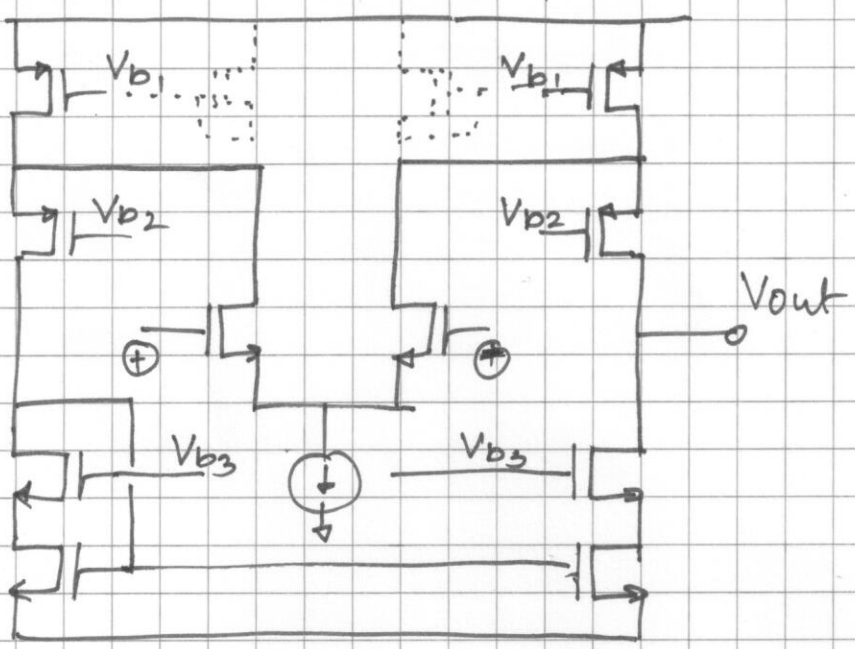


Signal Current flows to o/p. only sign change

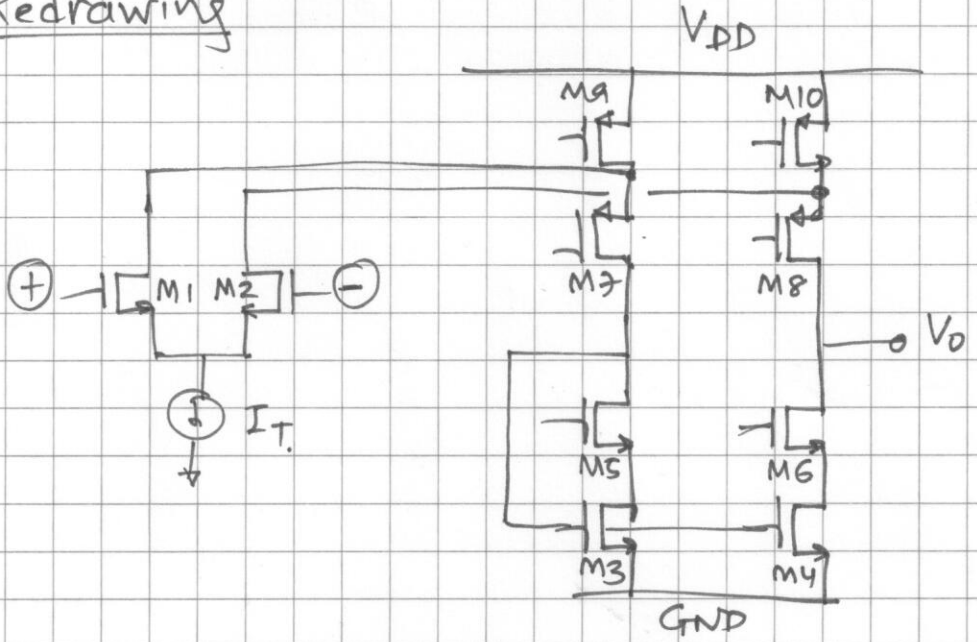
Key Concept of folded Cascode opamp

Avoid Mirror pole. M3/M5 & M4/M6

Folded Cascode OPAMP



Redrawing



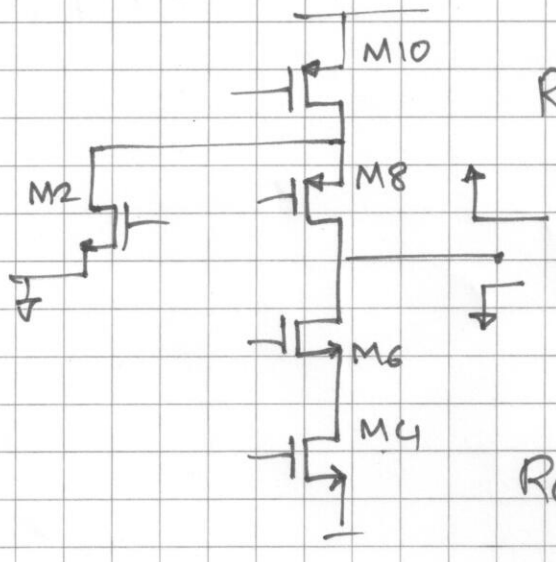
Advantage – No stacking of cascode on top of i/p. devices.

Large o/p swing ($V_{DD} - 4V_{dsat}$)

Calculate gain How?

Short o/p to DC ⇒ $G_m = g_m$,

Output impedance $\underline{R_{out}}$.



$$R_{out\uparrow} = g_{m8} r_{o8} \left[r_{o10} \parallel r_{o2} \right]$$

$$R_{out\downarrow} = (g_{m6} \cdot r_{o6}) r_{o4}$$

$$R_{out} = R_{out\uparrow} \parallel R_{out\downarrow}$$

$\parallel$ impedances Lets use g.

$$g_{out\uparrow} = \frac{(g_{ds2} + g_{ds10})}{g_{m8} \cdot r_{o8}}$$

$$g_{out\downarrow} = \frac{g_{ds4}}{g_{m6} \cdot r_{o6}}$$

diff pair

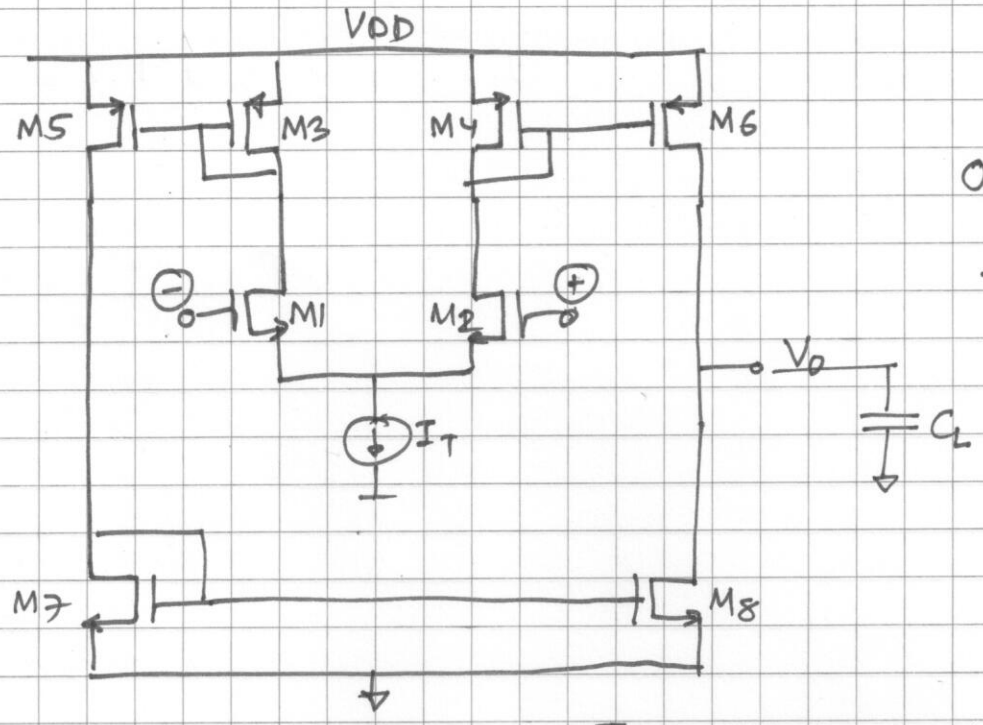
$$Gain = \frac{G_m}{g_{out}} = \frac{g_{m1} \cdot}{\frac{(g_{ds2} + g_{ds10})}{g_{m8} r_{o8}} + \frac{g_{ds4}}{g_{m6} \cdot r_{o6}}}$$

Extreme Simplification all g_ms equal. all g_{ds} equal.

$$Gain = \frac{g_m}{\frac{2g_{ds}}{g_m r_o} + \frac{g_{ds}}{g_m r_o}} = \frac{g_m}{3g_{ds}} \cdot g_m r_o$$

$$= \frac{1}{3} (g_m r_o)^2.$$

OPAMP using current mirrors



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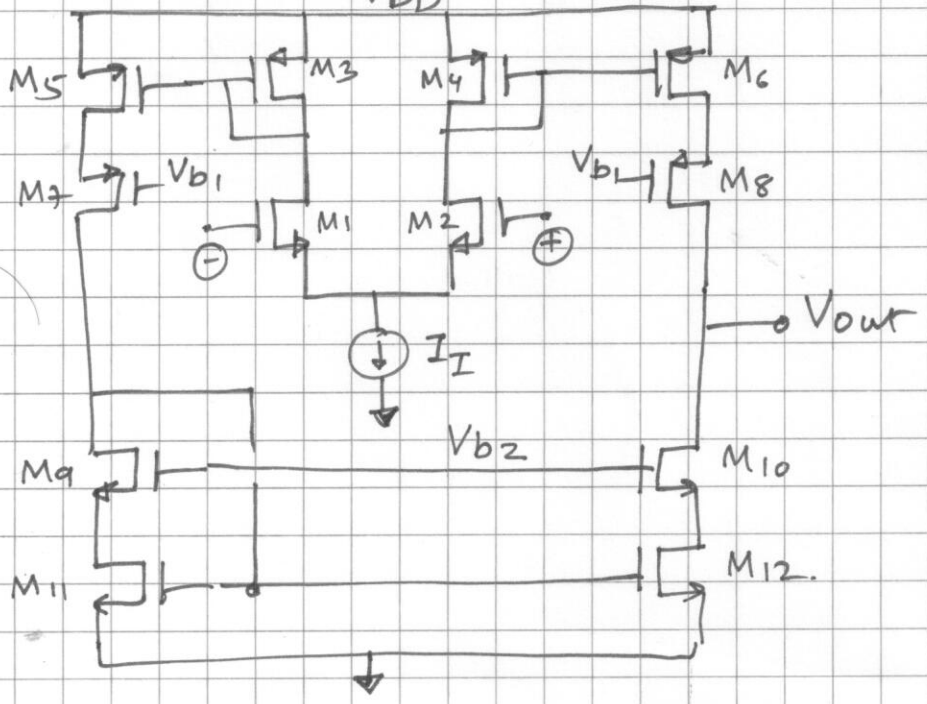
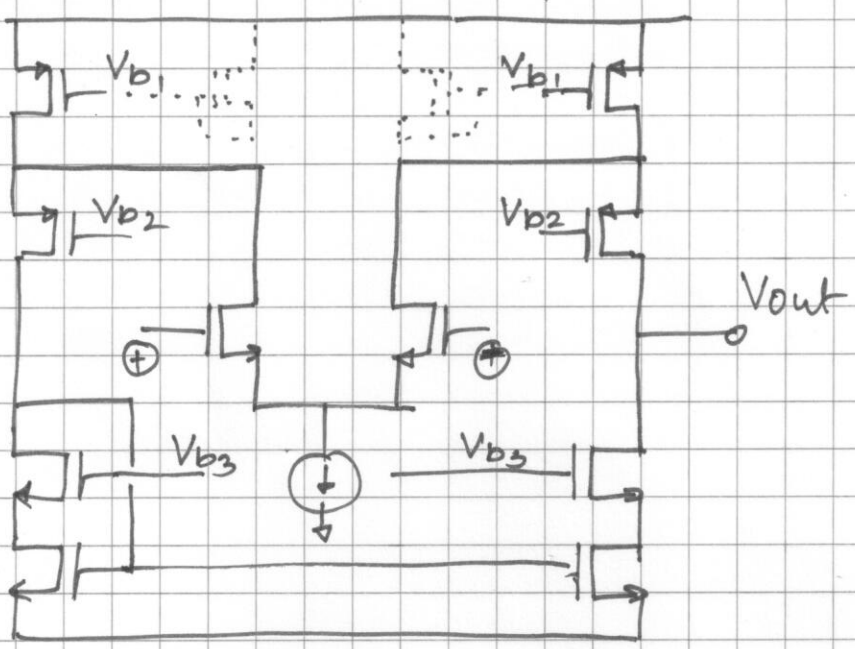
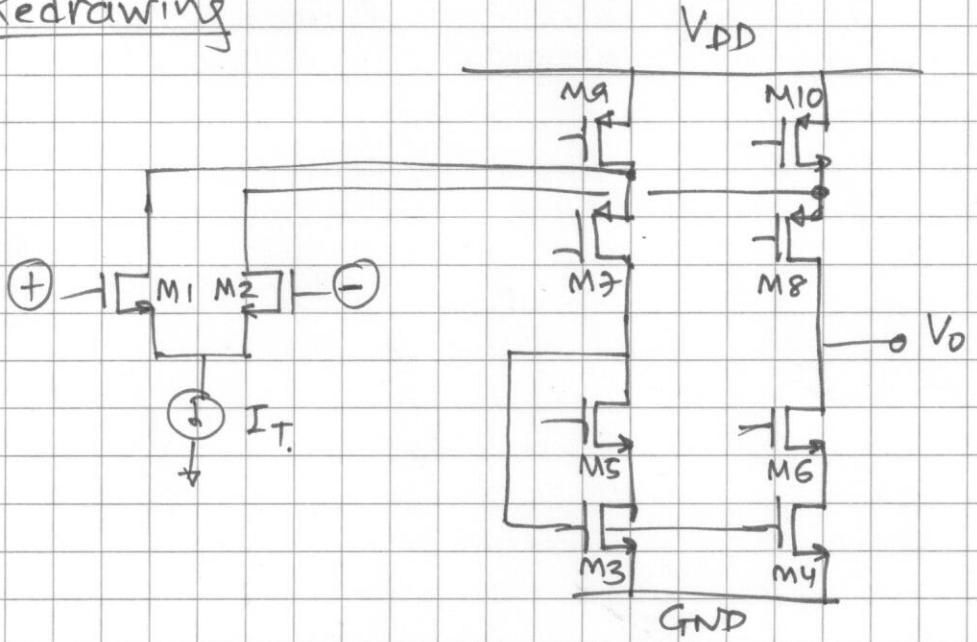


Gain $\frac{(g_m r_o)^2}{2}$.

Folded Cascode OPAMP



Redrawing



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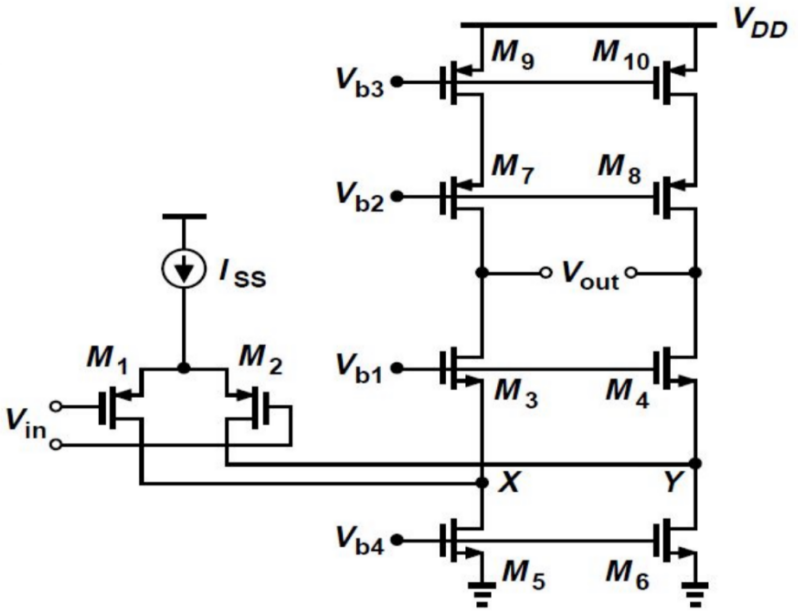
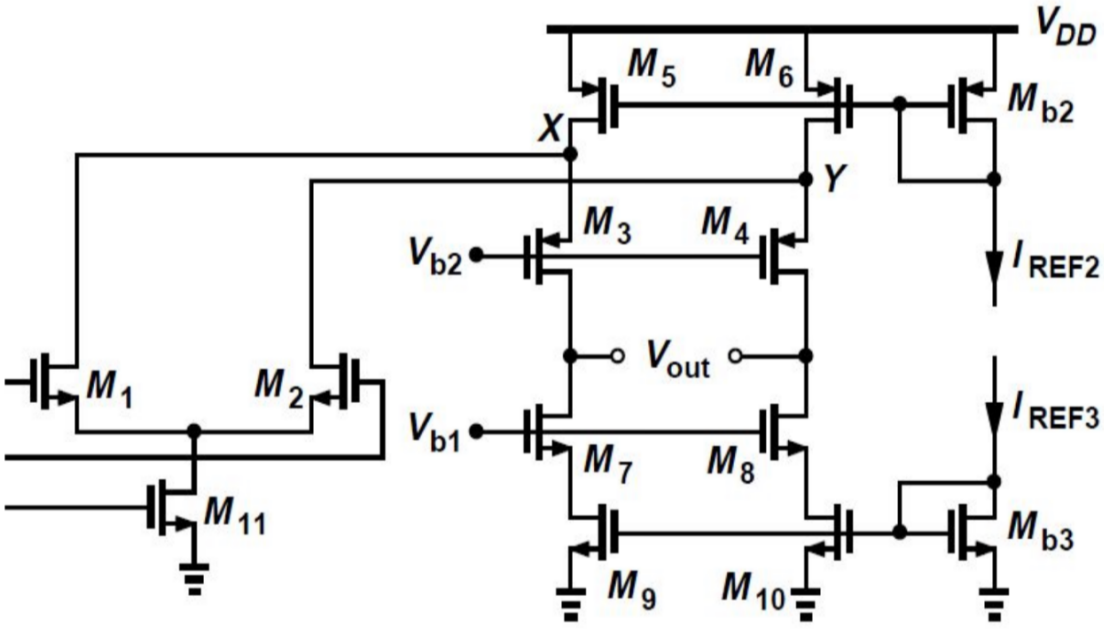
Folded cascode op amp with cascode PMOS load:



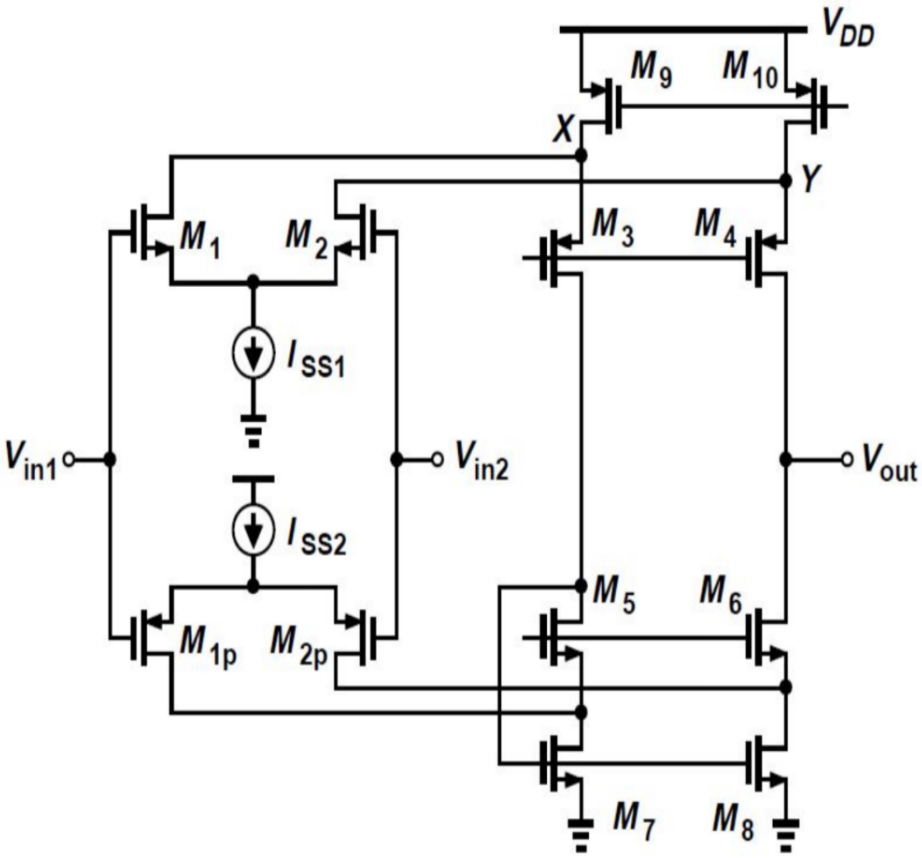
$V_{in,cm\ -\ range} => V_{DD}-(V_{Tp}+2V_{dsatp})$ to $V_{dsatn\ (previous\ stage)}$

Folded cascode op amp with cascode NMOS load:

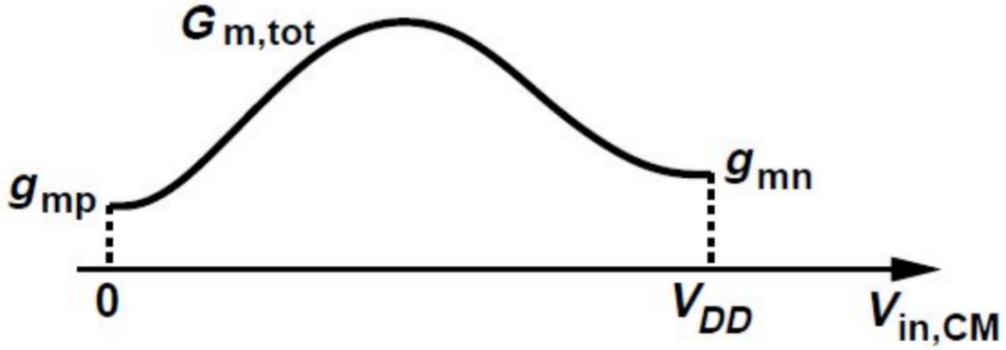


$V_{in,cm\ -\ range} => (V_{DD}- V_{dsatp\ (previous\ stage)})$ to $(V_{Tn}+2V_{dsatn})$

Extension of input common mode range:

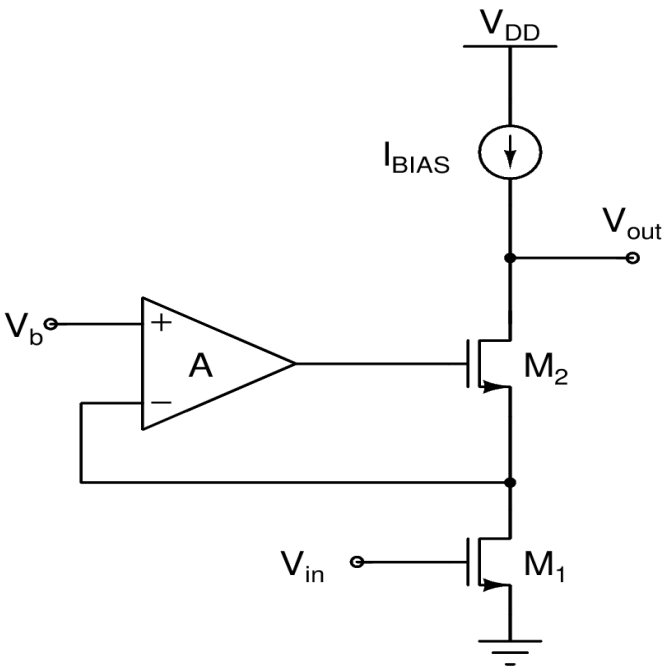


$$V_{\text{in, cm range}} = \sim V_{DD}$$



Reference: Design of Analog CMOS Integrated Circuits- B. Razavi. Chapter 9

Gain Boosting



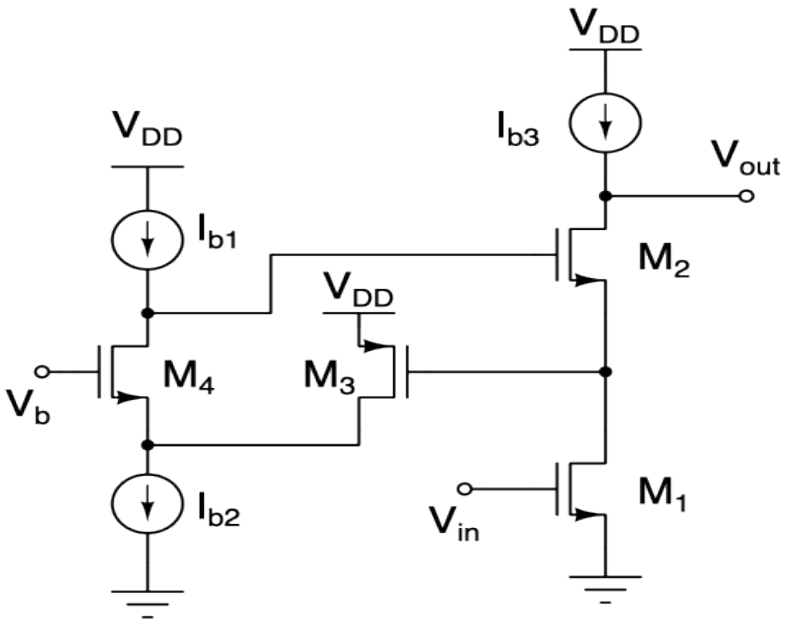
$$G_m = g_{m1}$$

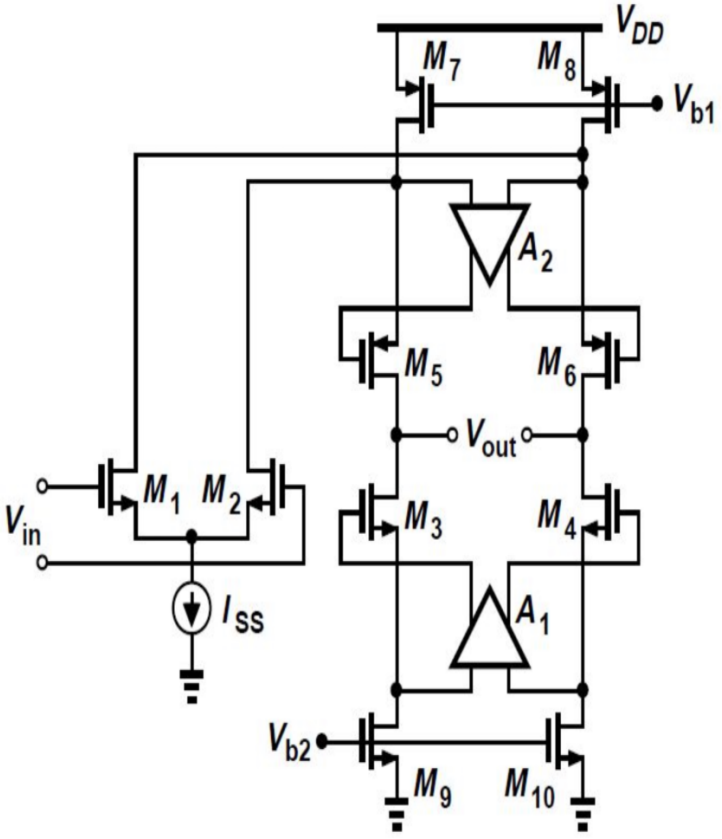
$$R_{out} = r_{o1} g_{m2} r_{o2} .(A+1)$$

$$\text{Gain} = g_{m1} r_{o1} g_{m2} r_{o2} .(A+1)$$

Reference: Klaas Bult JSSC – Dec 1990 pp. 1379 : Gain Boosting with Fast Settling

Implementation:





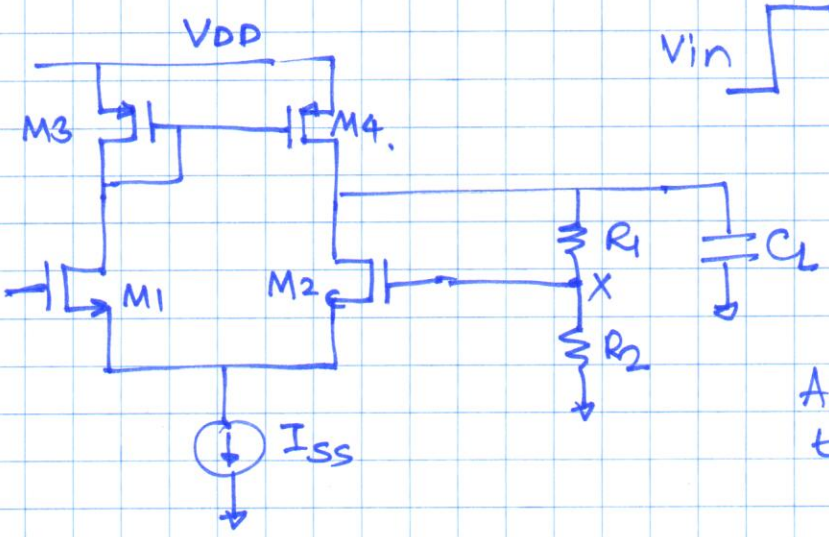
$$A = g_{m3} r_{o3} \frac{g_{m4} r_{o4}}{3}$$

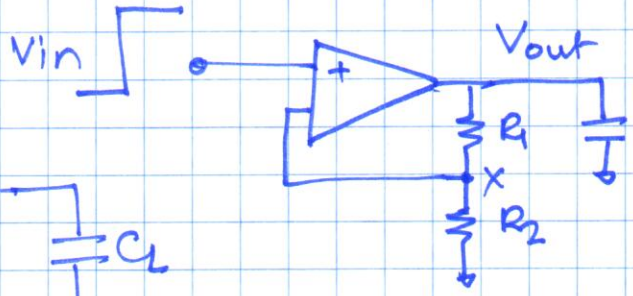
Slew Rate – Revisited

— large signal behavior Non-Linear

— fastest change in the node voltage.
decided by $\frac{I}{C} = \frac{dV}{dt}$

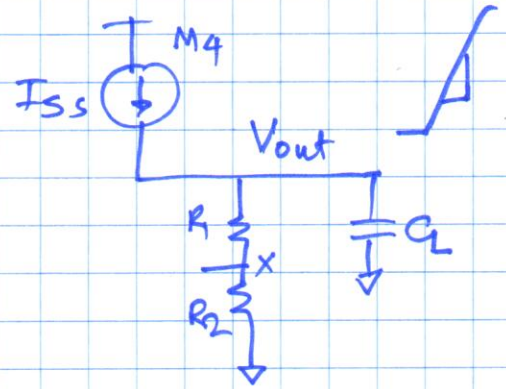
Consider single stage OTA





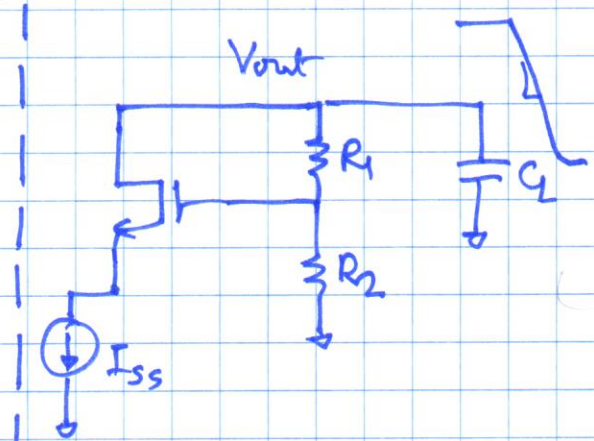
Assume $R_1 + R_2$ large to neglect current through

When ⌐ Vin step is applied,



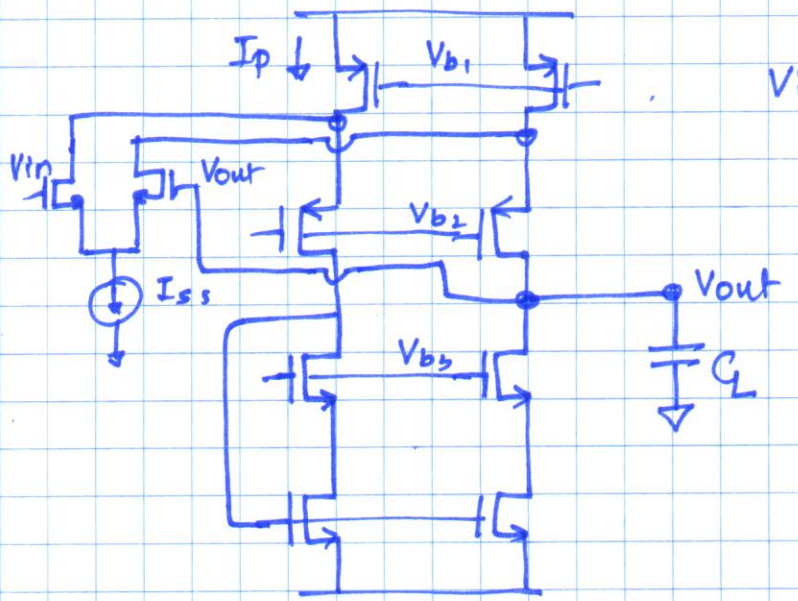
+ve slew rate = $\frac{I_{ss}}{C_L}$

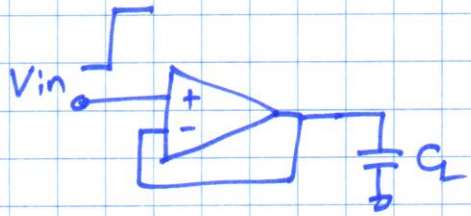
When ⌐ vin applied,



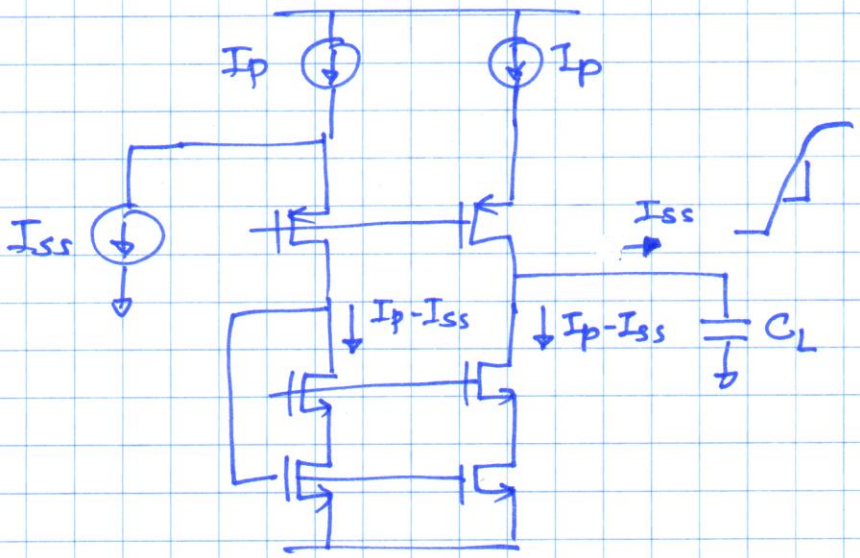
-ve slew rate = $\frac{I_{ss}}{C_L}$

Folded Cascode Opamp



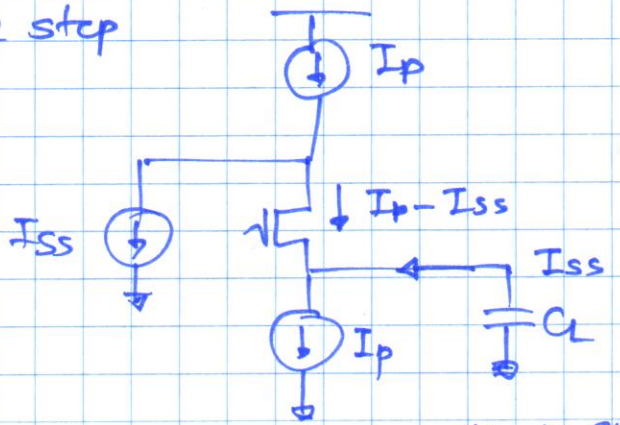


+ve step



+ve slew rate $= \frac{I_{ss}}{C_L}$

-ve step

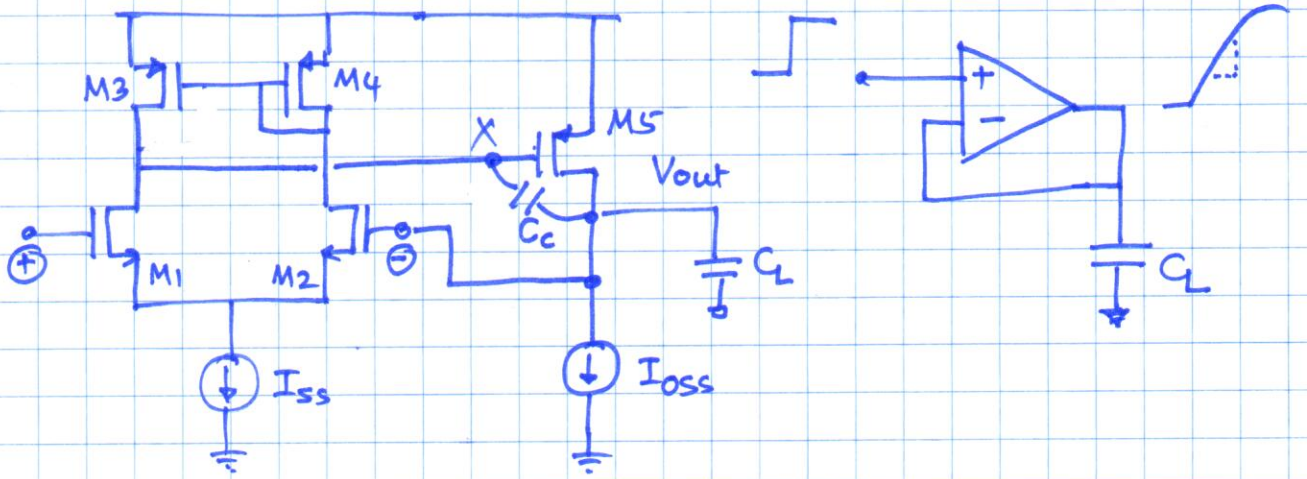


-ve slew rate $= \frac{I_{ss}}{C_L}$

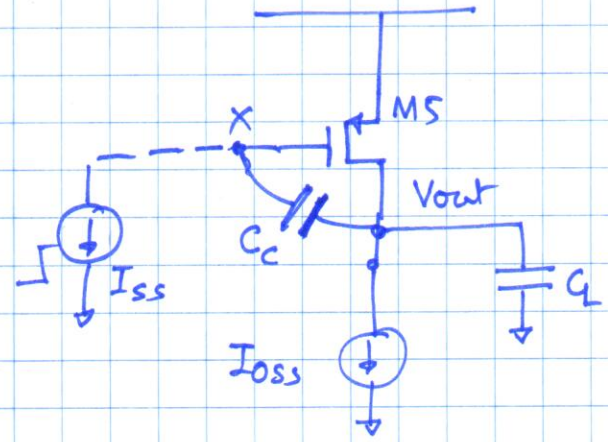
Keep $I_p = I_{ss}$ atleast

Else Slew rate limited to I_p/C_L I

Two stage op-amps slew rate.



+ve i/p step



Node x virtual gnd due to gain of M5.

$$\frac{dV_{out}}{dt} = \frac{I_{ss}}{C_c}$$

Current thru. $C_L = C_L \cdot \frac{dV_{out}}{dt}$

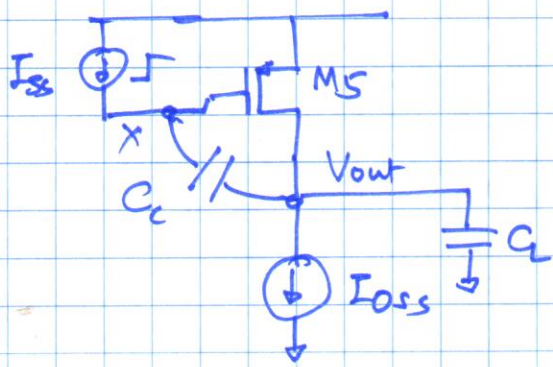
$$= \frac{C_L}{C_c} \cdot I_{ss}$$

M5 must support & stay in sat.

$$\left(I_{ss} + \frac{C_L}{C_c} I_{ss} + I_{oss}\right)$$

Slew rate = $\frac{I_{ss}}{C_c}$

-ve i/p step



$$\frac{dV_{out}}{dt} = \frac{I_{ss}}{C_c} \quad \text{(slew rate)}$$

if. $I_{oss} \geq I_{ss} + \frac{C_L}{C_c} I_{ss}$

Slew rate if $I_{oss} < I_{ss}\left(1 + \frac{C_L}{C_c}\right)$

$$= \frac{(I_{oss} - I_{ss})}{C_L}$$ | M5 off

How to increase slew rate?

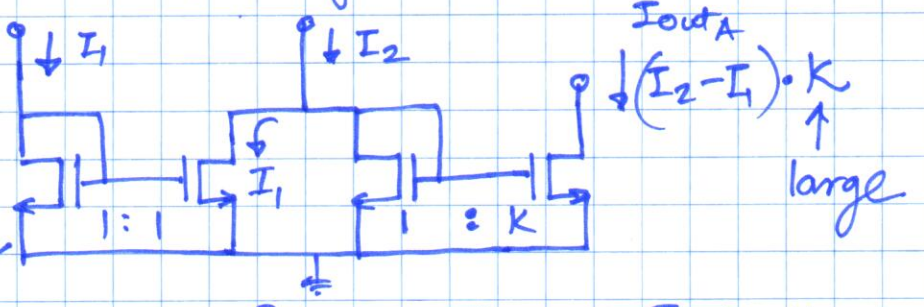
→ ↑ I_T → Increase in Quiescent Power

→ increase I_T only when large i/p voltage step applied.

→ Adaptively Biased opAMP. JSSC - JUNE 82

REFERENCE : ADAPTIVE BIASING CMOS AMP - DEGRAUWE

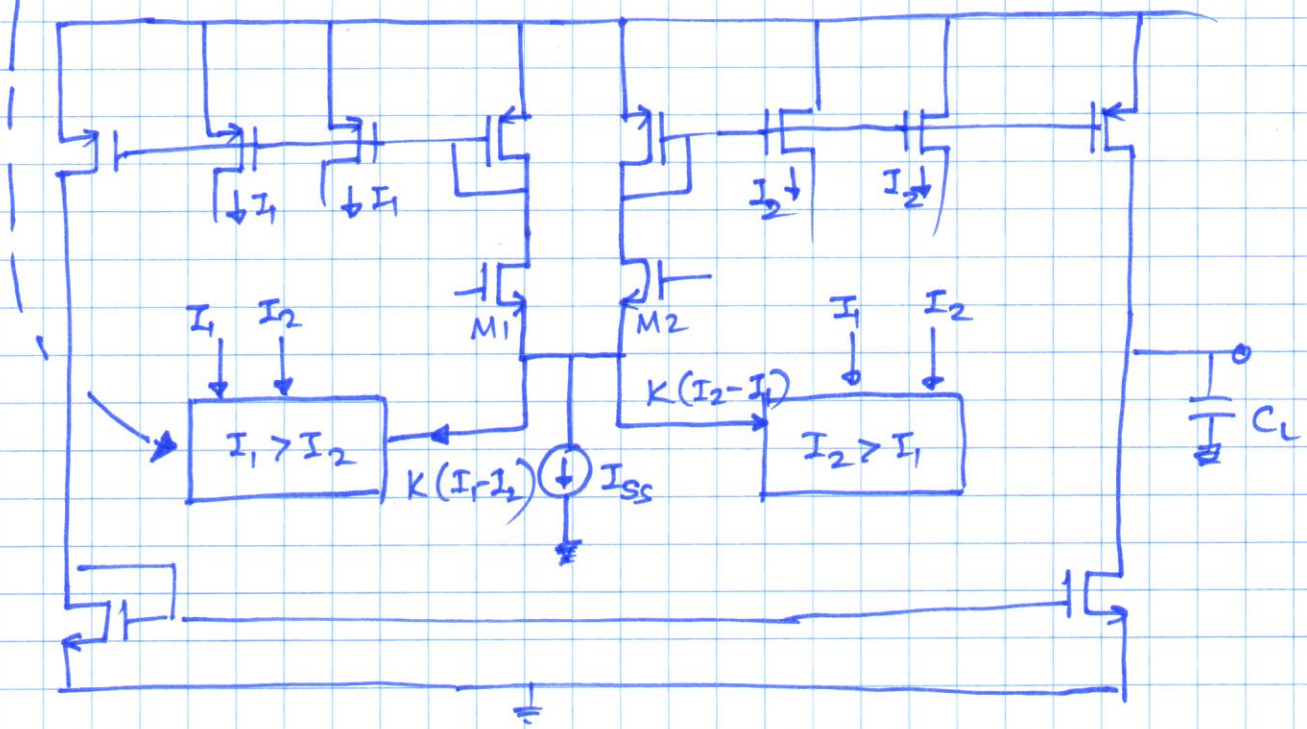
Consider following current mirror based circuit

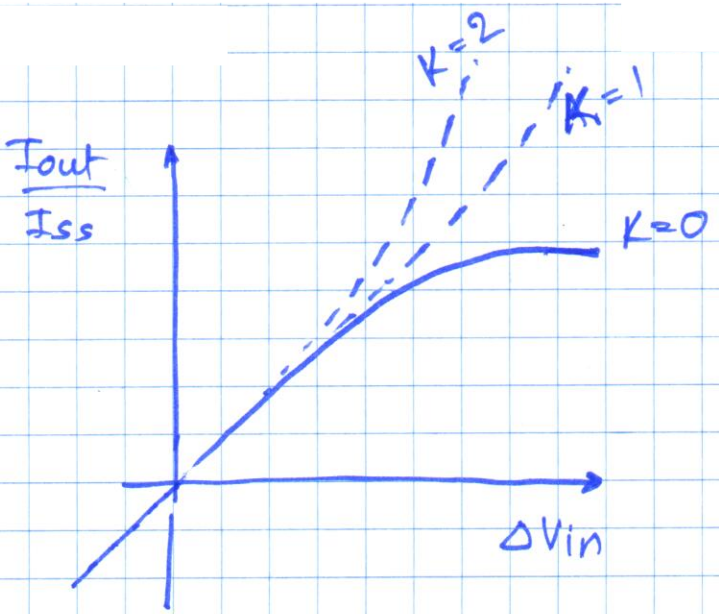


⇒ when $I_1 = I_2$ → $I_{out_A} \cong 0$

when $I_2 \gg I_1$ → $I_{out_A} = \underbrace{K(I_2 - I_1)}_{\text{large current}}$

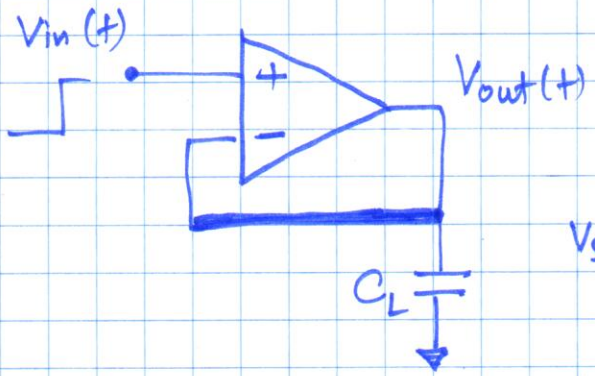
$I_2 < I_1$ → off. $I_{out_A} = 0$

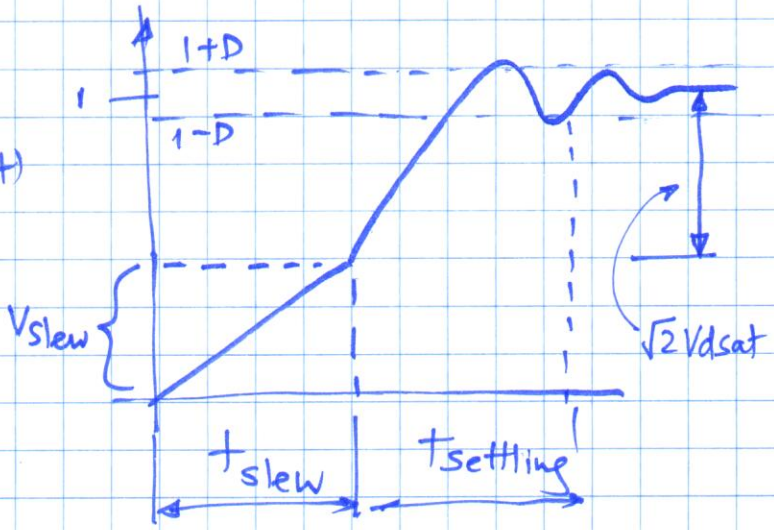




✡ Settling Time — Small-signal

Consider





Excellent Reference

Considerations for fast Settling Amplifiers

Howard Yang, Allstot —

IEEE Tran. CAS March 90

(from Allstot Notes)

Consider Opamp with single pole response. $a(s) = \frac{a_0}{\left(1+\frac{s}{p_1}\right)}$

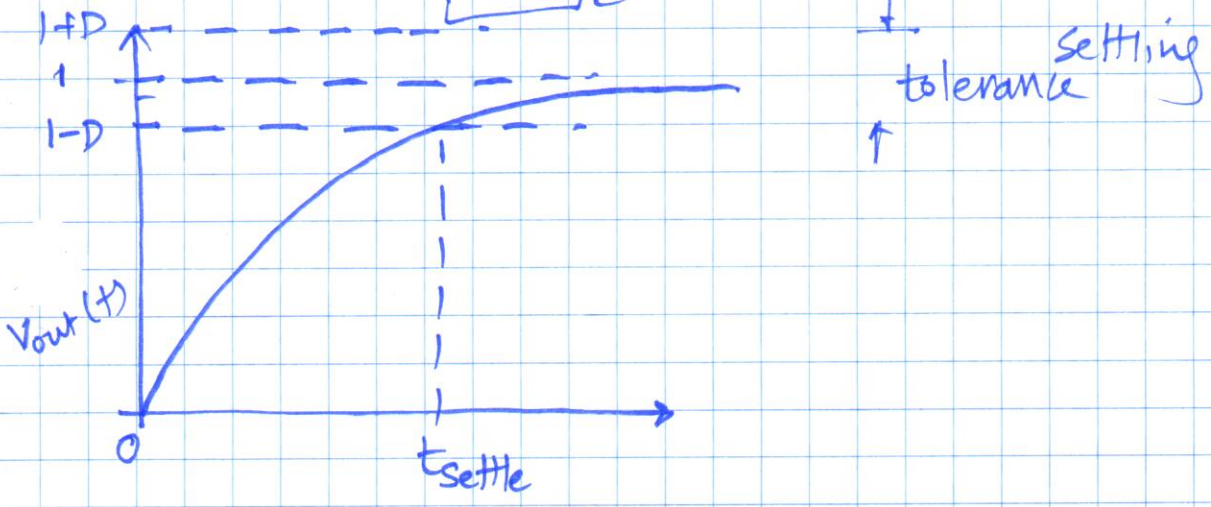
$$A(s) = \frac{a(s)}{1+a(s)} = \frac{a_0 p_1}{s + p_1(a_0+1)}$$

For unit step $V_{in}(s) = \frac{1}{s}$

$$V_{out}(s) = A(s) V_{in}(s) = \frac{a_0}{a_0+1}\left[\frac{1}{s} - \frac{1}{s+p_1(a_0+1)}\right]$$

Time domain ($\frac{a_0}{a_0+1} \to \sim 1$)

$$V_{out}(t) = \left[\frac{a_0}{a_0+1}\right]\left[u(t) - e^{-p_1(a_0+1)t}\right]$$



τ = small-signal settling time constant

$$= \frac{1}{p_1(a_0+1)} \simeq \frac{1}{p_1 a_0} \simeq \frac{1}{\omega_u} \leftarrow \underline{\text{GBW}}$$

D (%)	$t_s = -\tau \ln D$	f_u
1 (6.64 bits)	4.61τ	73.4 MHz
0.01 (13.3 bits)	9.21τ	147 MHz
0.001 (16.6 bits)	11.51τ	183 MHz
0.0001 (20 bits)	13.82τ	220 MHz

for 100 MHz operation.

Example $D = 0.01\%$ $\quad 20\log(0.01/100)^{-1}$

$= 80\,dB$ SNR

$\Rightarrow \frac{80}{6} \Rightarrow$ 13.33 bits resolution

$t_s = -\tau \ln D = -\tau \ln(0.0001)$

$= 9.21\tau.$

we wish to settle in $\frac{1}{100MHz}$ time $= 10nS.$

$t_{settle} = 10ns = 9.21\tau.$

$\Rightarrow \tau = 1.0857\,nS.$

$f_u = \frac{1}{2\pi\tau} = 146.6\,MHz$

Yang paper describes Minimum Settling Time as a function of Phase margin. for two pole system

Note Phase Margin depends on relative positions of two poles.

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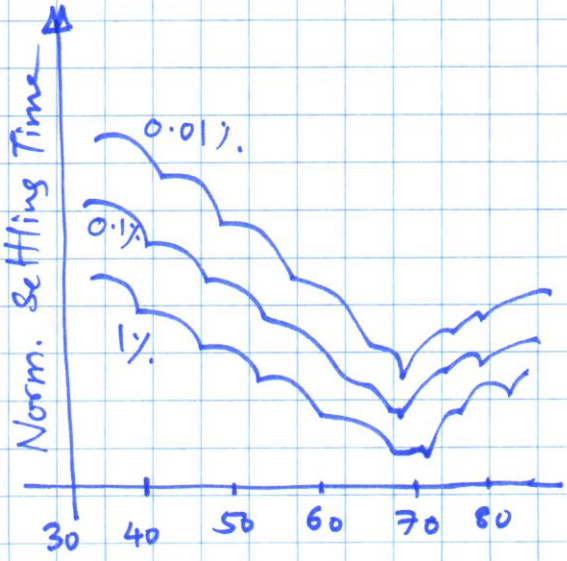

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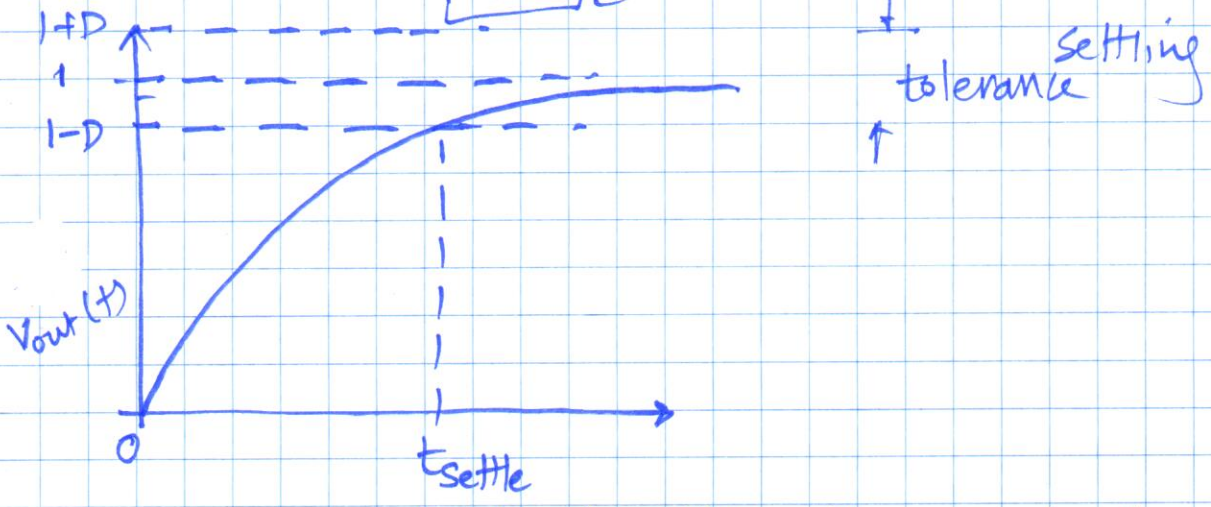

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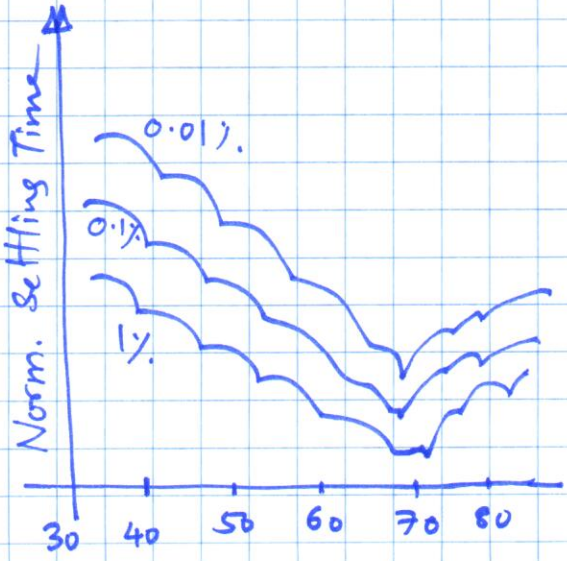
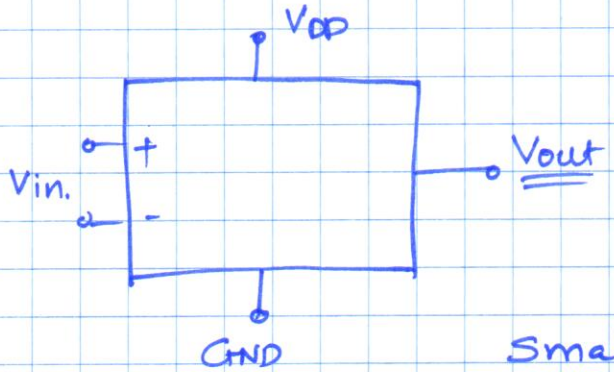


24 September 2019

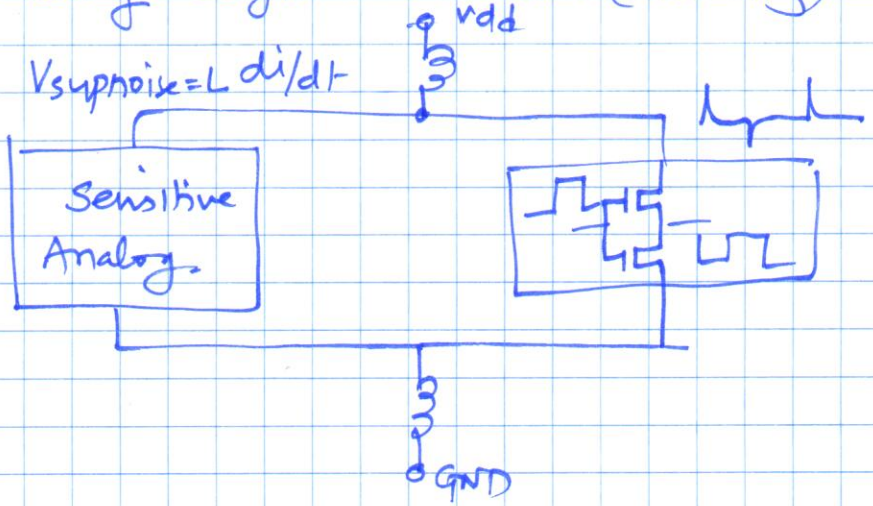
Power Supply Rejection Ratio PSRR



Supply noise either on Vdd or GND can leach into Vout - limiting smallest signal we can detect.

Source of Supply noise

* Off-chip noise electrically coupled through pins
* Noise of V_{DD} (regulators - switching power supplies)
* Noise coupled through V_{DD} / GND bondwires sharing digital circuits. (switching)

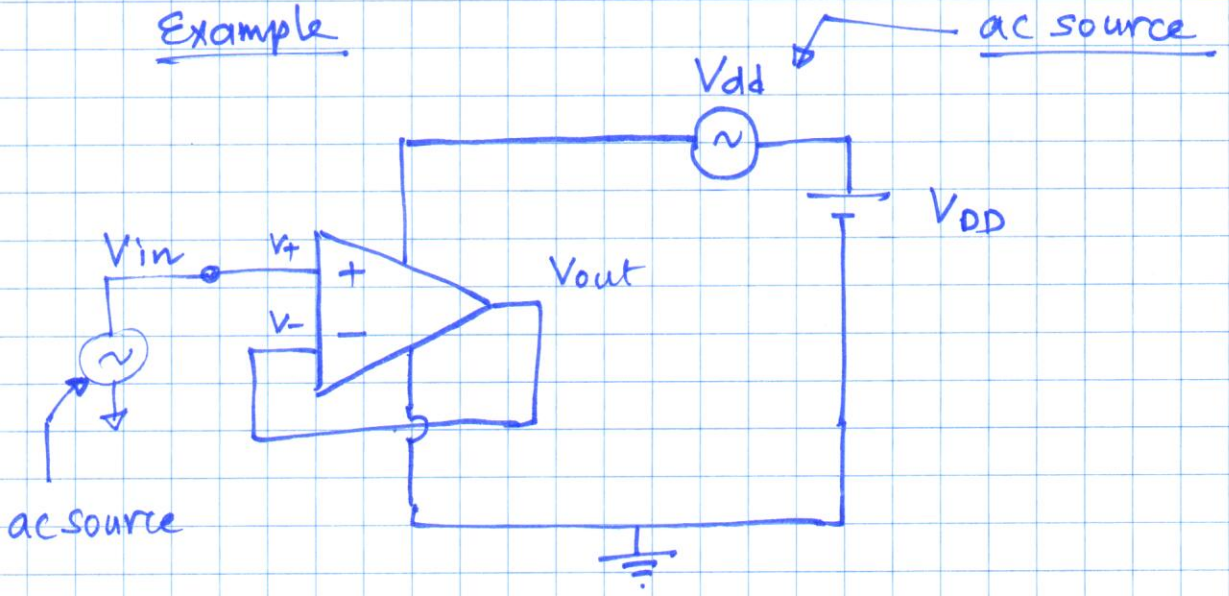


$$PSRR\ (definition) = \frac{A_{dm}\ (\sim V_{dd}\ or\ \sim GND = 0)}{A_{ps}\ (V_{in} = 0)}$$

A_{ps} = AC gain from Vdd or Gnd to Vout when $V_{in} = 0$.

Measuring PSRR

Example



To calculate gain from Vdd to Vout Vin = 0

$$V_{out} = A_{Ps\,Vdd} V_{dd} + A_{dm}(V_+ - V_-)$$

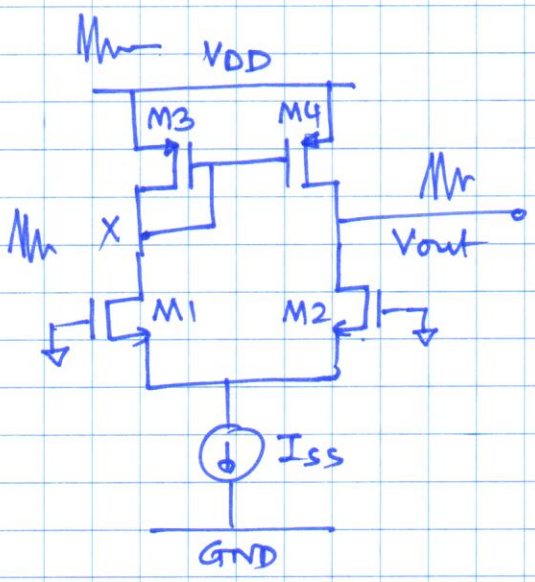
$$V_{out} = A_{Ps\,Vdd} V_{dd} + A_{dm}(0 - V_{out})$$

$$V_{out}(1 + A_{dm}) = A_{Ps\,Vdd} V_{dd}$$

$$\frac{V_{out}}{V_{dd}} = \frac{A_{Ps\,Vdd}}{(1 + A_{dm})} \cong \frac{A_{Ps\,Vdd}}{A_{dm}} = \frac{1}{PSRR}$$

Caution: During PSRR measurements, make sure all biasing circuits are included.

Insights on PSRR

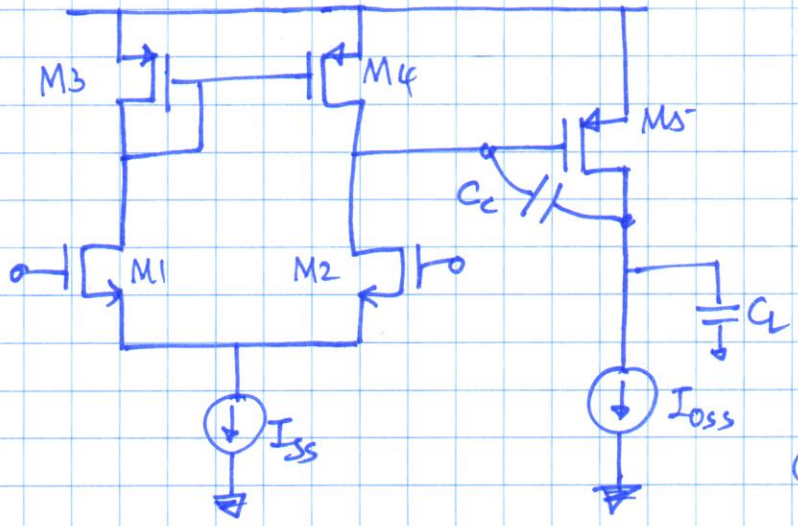


unity gain from V_{DD} to V_{out}

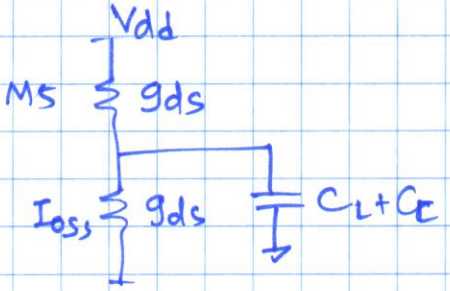
$$A_{PS_{VDD}} = 1$$

$$\therefore \text{PSRR} = \frac{g_{m_N} r_{out}}{1}$$

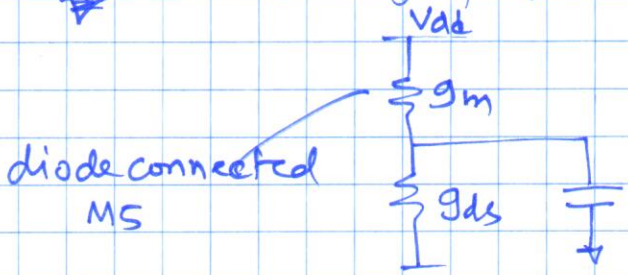
Two Stage OTA



@ Low frequency



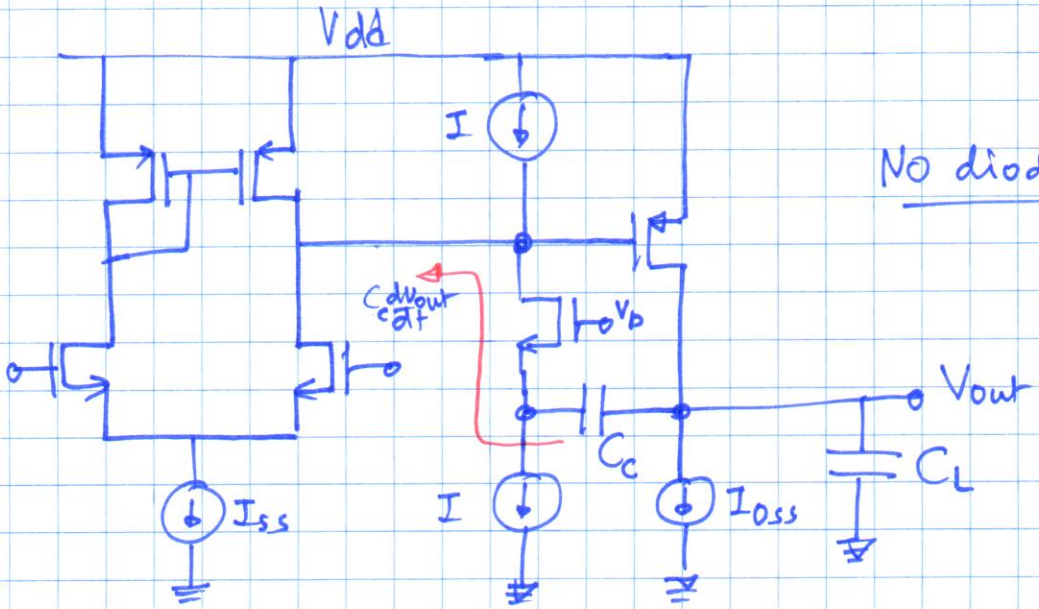
@ High frequencies



Poor PSRR @ High frequencies.

To improve High freq. PSRR — C_c decoupling from V_{dd}.

How?



No diode @ HF

ZELE EE618

LECTURE 14

24 September 2019

NOISE

Lecture Notes adapted from Chapter 7

B. Razavi (Design of Analog CMOS ICs)

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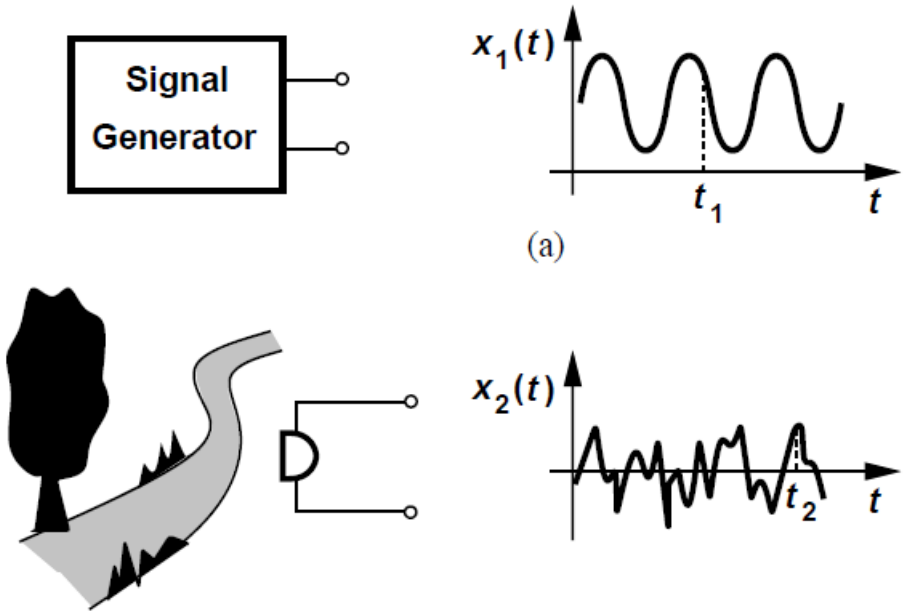
Statistical Characteristics of Noise



- **Noise - random process**
- **Noise is everywhere**
- ***$x_1(t_1)$ & $x_2(t_2)$* - Difference between deterministic and random**
- **Noise(t) unpredictable**
- **Noise can't be calibrated out**

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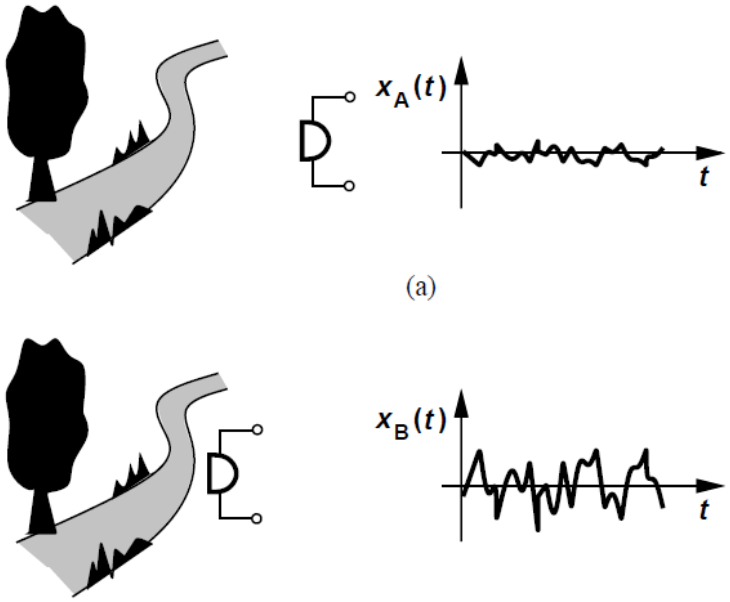
Statistical Characteristics of Noise



- **Average power of noise is predictable**
- **Average power delivered by a periodic voltage *v(t)* with period *T* to a load resistance R_L is defined as**

$$P_{av} = \frac{1}{T}\int_{-T/2}^{+T/2} \frac{v^2(t)}{R_L} dt$$

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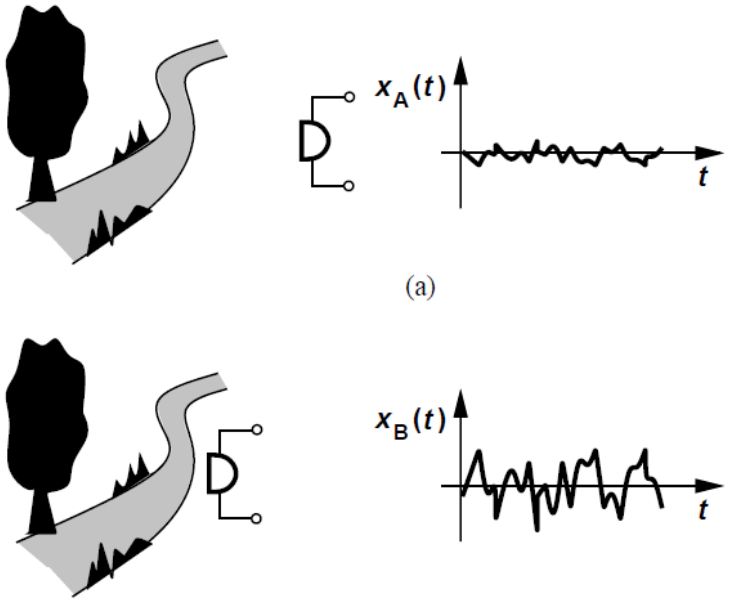
Statistical Characteristics of Noise



- **Random signal (aperiodic): measurement over a long time**

$$P_{av} = \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{+T/2} \frac{x^2(t)}{R_L} dt$$

- ***$x_B(t)$* delivers more power than *$x_A(t)$***

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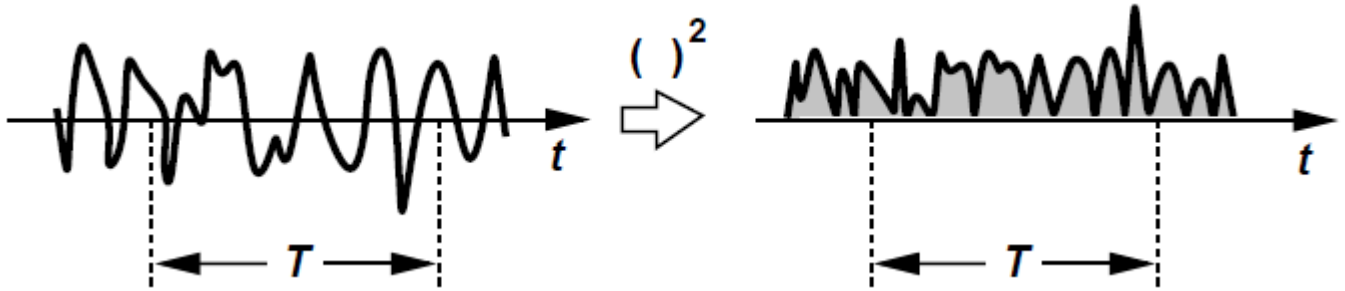
Statistical Characteristics of Noise

- To calculate average power of (noise) signal *x(t)*



- P_{av} is defined as

$$P_{av} = \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{+T/2} x^2(t)dt$$

- P_{av} is expressed in V^2 rather than *W*
- RMS voltage for noise can be defined as $\sqrt{P_{av}}$

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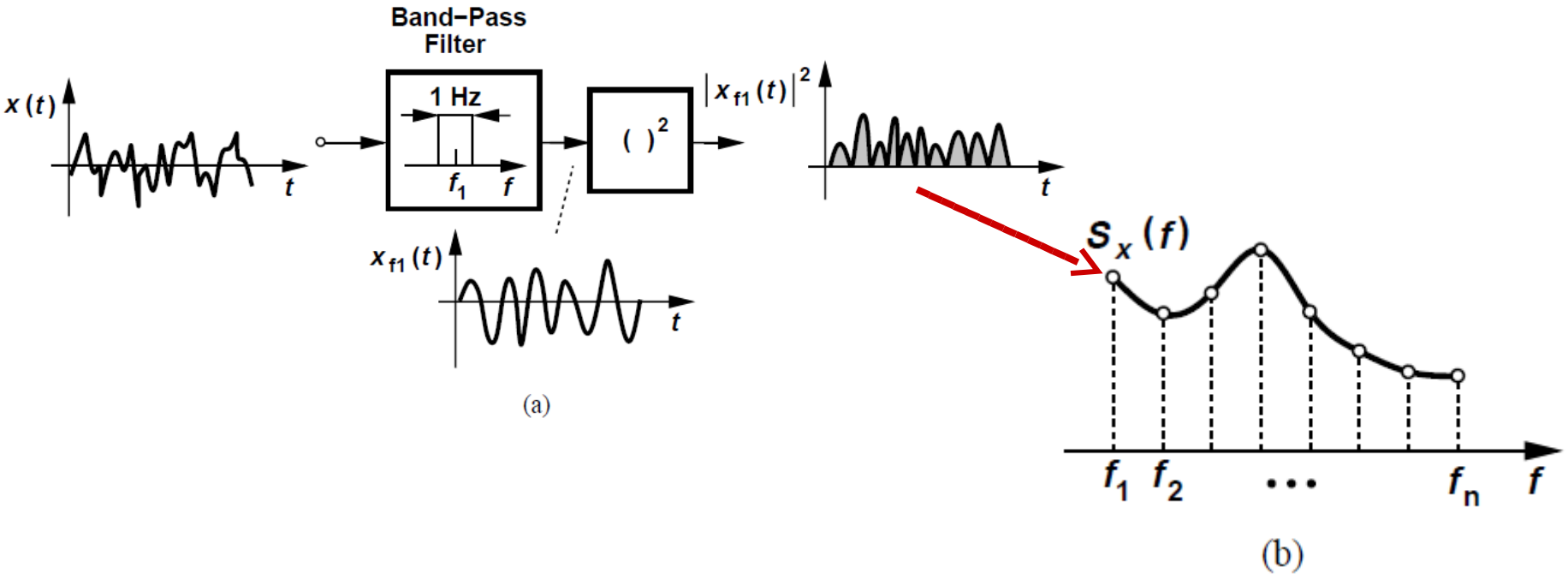
Noise Spectrum

- **Power Spectral Density (PSD) $S_x(f)$**
  - **signal power at each frequency**
- **$S_x(f)$ defined as the average power carried by $x(t)$ in a 1-Hz bandwidth around f**



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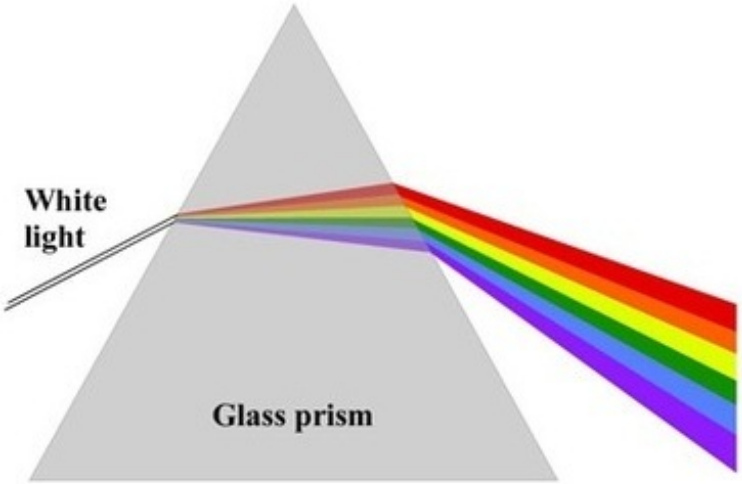
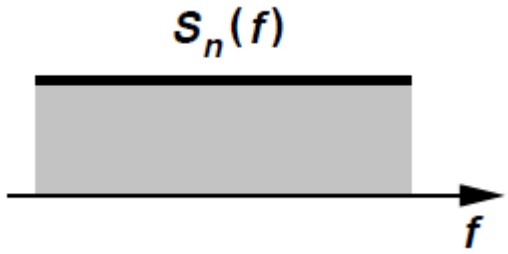
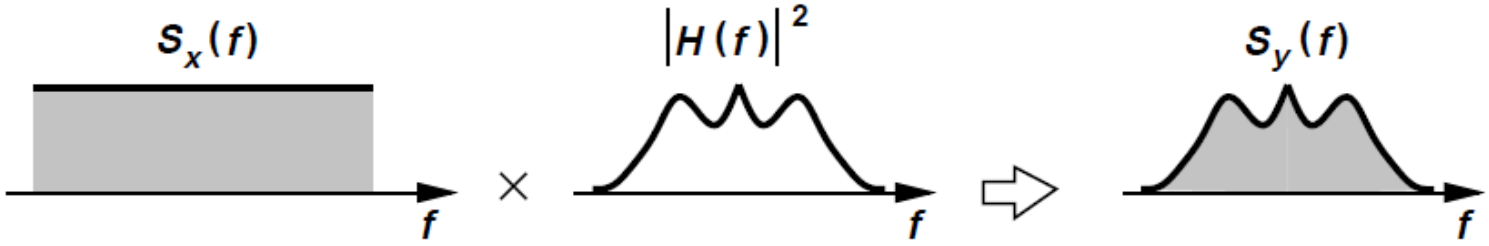
Noise Spectrum

- $S_x(f)$ -- V^2/Hz or $V/\sqrt{Hz}$
- **white noise PSD -- Noise spectrum that is flat *in the band of interest* is usually called white**



Color	λ (nm)	Freq (Hz)
Red	760-647	4.3×10^{14}
Orange	647-585	4.3×10^{14}
Yellow	585-575	5.2×10^{14}
Green	575-491	5.6×10^{14}
Blue	491-424	6.6×10^{14}
Violet	424-380	7.3×10^{14}





$$S_Y(f) = S_x(f)|H(f)|^2$$

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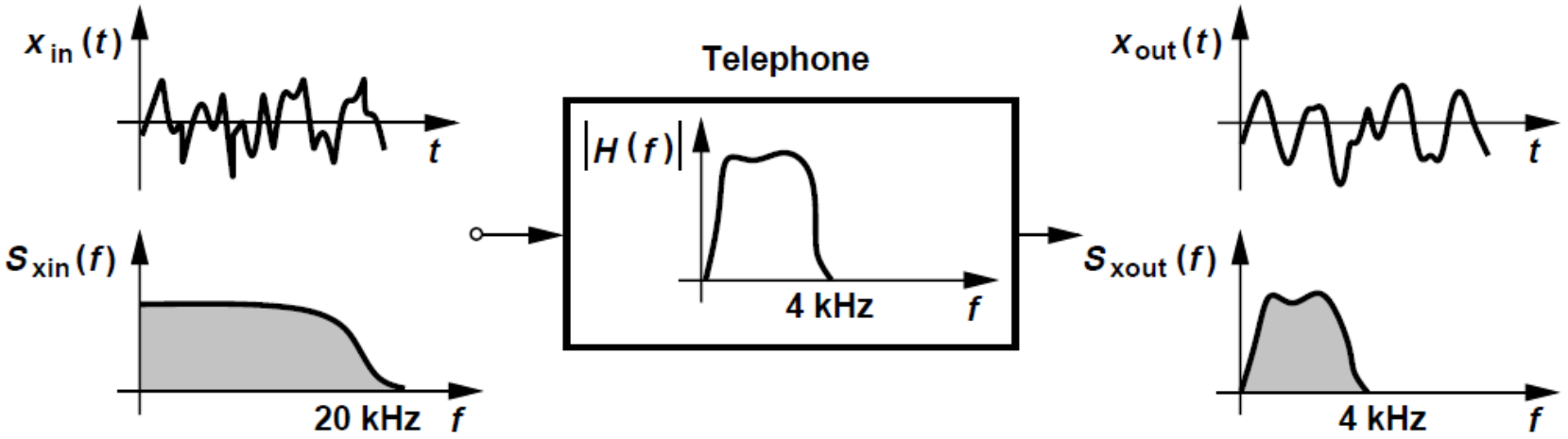
Telephone Example



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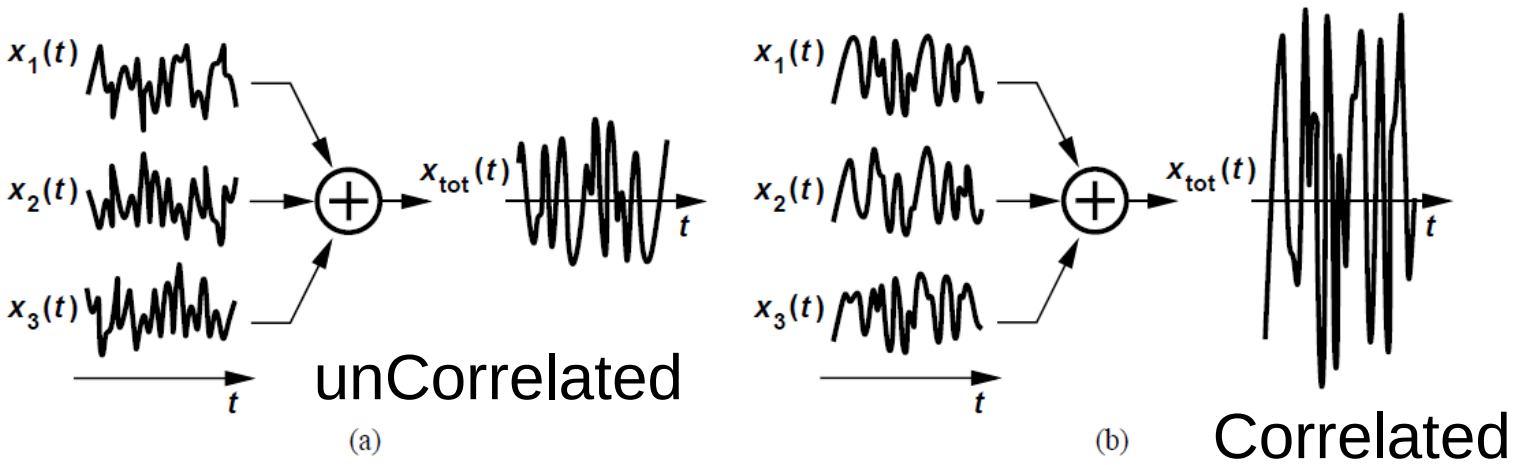
Correlated vs Uncorrelated Sources

- **Superposition Principle not suitable for random noise signals**
- **Average noise power**

$$
\begin{aligned}
P_{av} &= \lim_{T\to\infty}\frac{1}{T}\int_{-T/2}^{+T/2}[x_1(t)+x_2(t)]^2dt \\
&= \lim_{T\to\infty}\frac{1}{T}\int_{-T/2}^{+T/2}x_1^2(t)dt + \lim_{T\to\infty}\frac{1}{T}\int_{-T/2}^{+T/2}x_2^2(t)dt \\
&\quad + \lim_{T\to\infty}\frac{1}{T}\int_{-T/2}^{+T/2}2x_1(t)x_2(t)dt \\
&= P_{av1} + P_{av2} + \lim_{T\to\infty}\frac{1}{T}\int_{-T/2}^{+T/2}2x_1(t)x_2(t)dt,
\end{aligned}
$$

correlation

Stadium Noise



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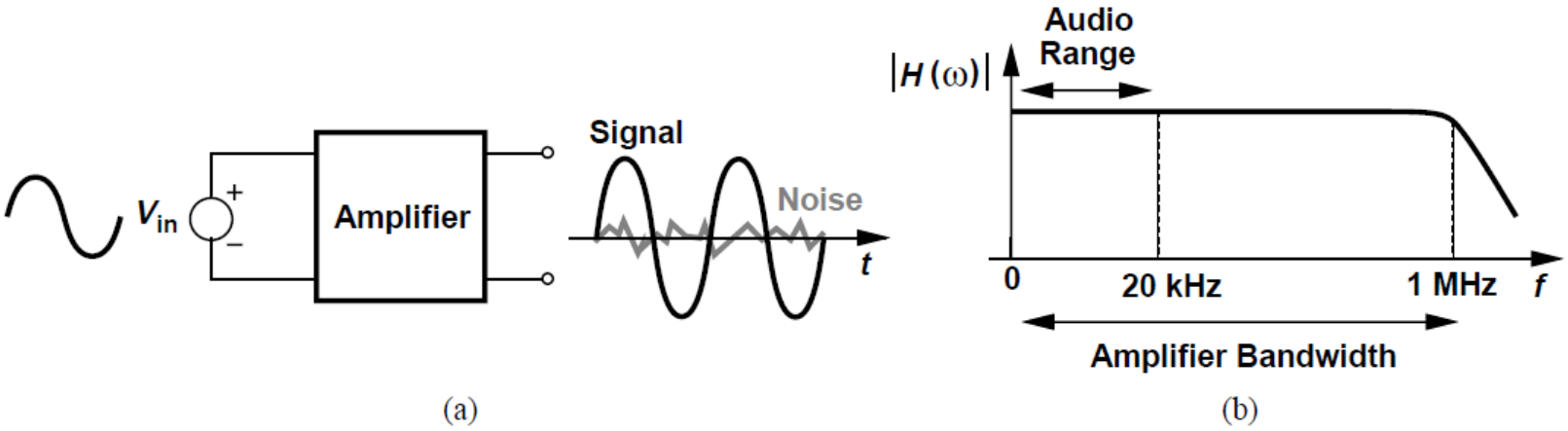
Signal-to-Noise Ratio (SNR)

- **SNR – intelligibility of the signal**

$$\text{SNR} = \frac{P_{sig}}{P_{noise}}$$

- **For a sinusoid with peak amplitude *A*, $P_{sig} = A^2/2$**
- **Noise Power**

$$P_{noise} = \int_{-\infty}^{+\infty} S_{noise}(f)\,df.$$



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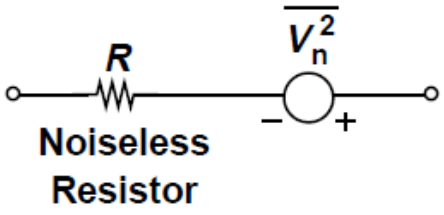
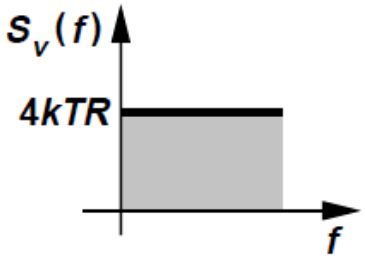
Resistor Thermal Noise

- **Random motion of electrons in a conductor induces fluctuations in the voltage measured across it even though the average current is zero**





$$S_v(f) = 4kTR, \quad f \geq 0$$

$$\overline{V_n^2} = 4kTR$$

- ***k*** **= 1.38 X 10^{-23} J/K is the Boltzmann constant**
- **1000 Ω (300 K) → 16 X 10^{-18} *V^2/Hz*, or 4 nV/√Hz**

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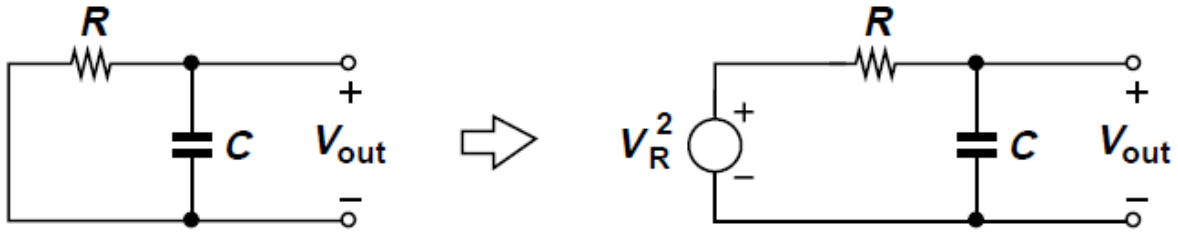
Resistor Thermal Noise: Example



Noise spectrum and total noise power in V_{out}

$$\frac{V_{out}}{V_R}(s) = \frac{1}{RCs+1}$$

$$P_{n,out} = \int_0^\infty \frac{4kTR}{4\pi^2R^2C^2f^2+1}df$$

$$S_{out}(f) = S_v(f)\left|\frac{V_{out}}{V_R}(j\omega)\right|^2$$

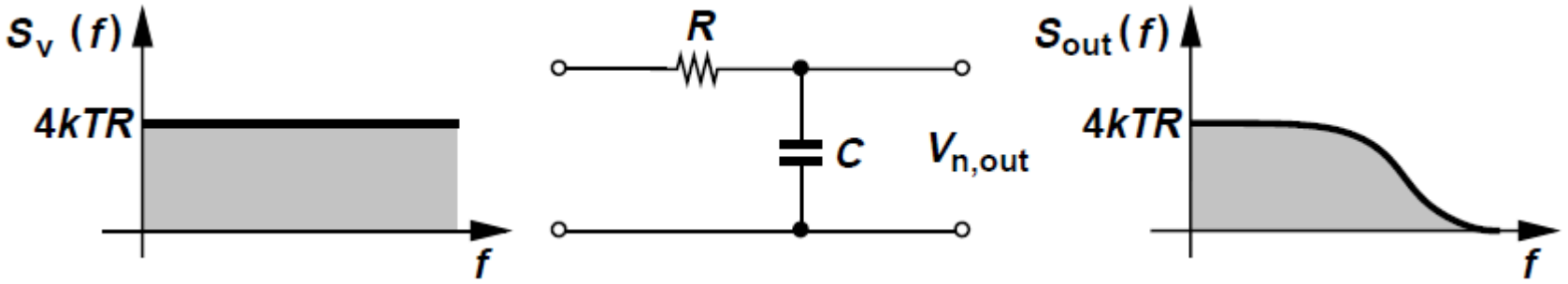
$$= 4kTR\frac{1}{4\pi^2R^2C^2f^2+1}$$

$$Put\ 2\pi RCf = u$$

$$P_{n,out} = \frac{2kT}{\pi C}\int_0^\infty \frac{du}{u^2+1}$$

$$P_{n,out} = \frac{2kT}{\pi C}\tan^{-1}u\Big|_{u=0}^{u=\infty}$$

$$= \frac{kT}{C}.$$



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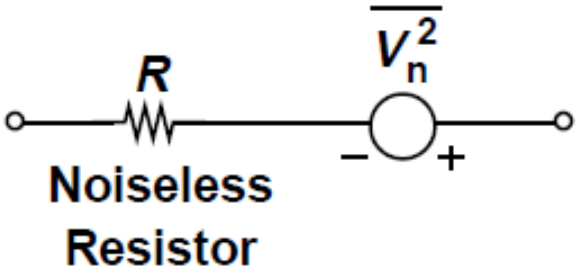
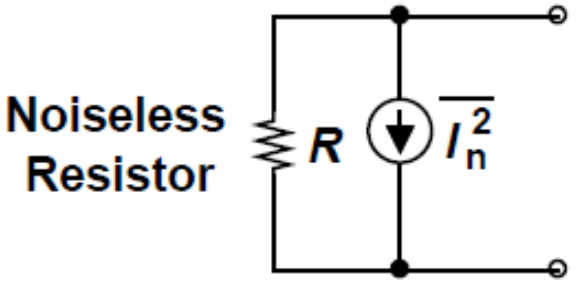
Resistor Thermal Noise



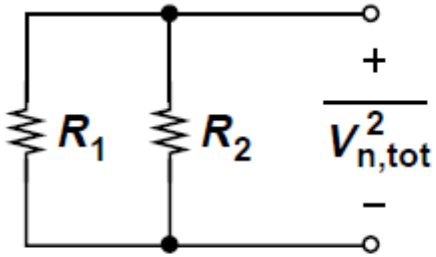
$$\overline{V_n^2} = 4kTR$$

V^2/Hz

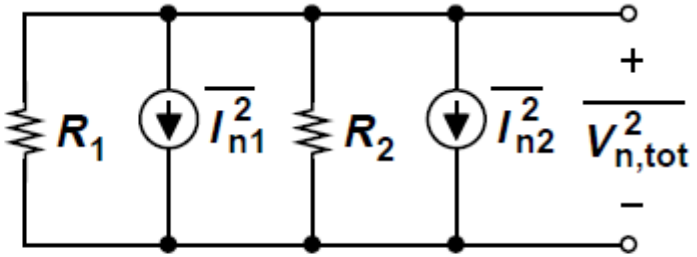


$$\overline{I_n^2} = 4kT/R$$

A^2/Hz



$$\overline{I_{n,tot}^2} = \overline{I_{n1}^2} + \overline{I_{n2}^2} = 4kT\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$$



$$\overline{V_{n,tot}^2} = \overline{I_{n,tot}^2}(R_1 \| R_2)^2 = 4kT(R_1 \| R_2),$$

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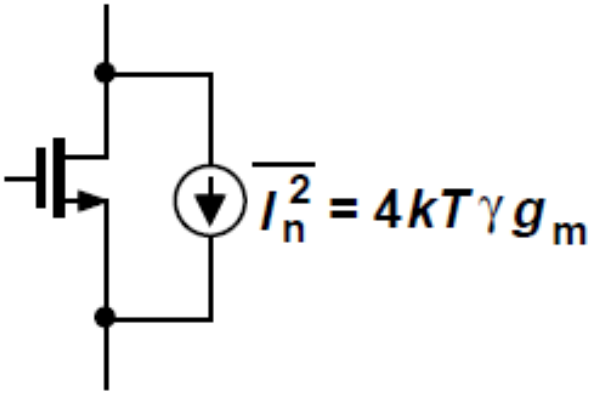
MOSFET Thermal Noise

- **The Thermal noise generated in the channel**
- **For long-channel MOS devices operating in saturation,**



γ *(Excess Noise Coefficient)* = 2/3 for long-ch transistors
2-3 for short-ch transistors

Short channel device – Ecritical – Velocity saturation – extra work done by Efield – dissipation → Noise ^

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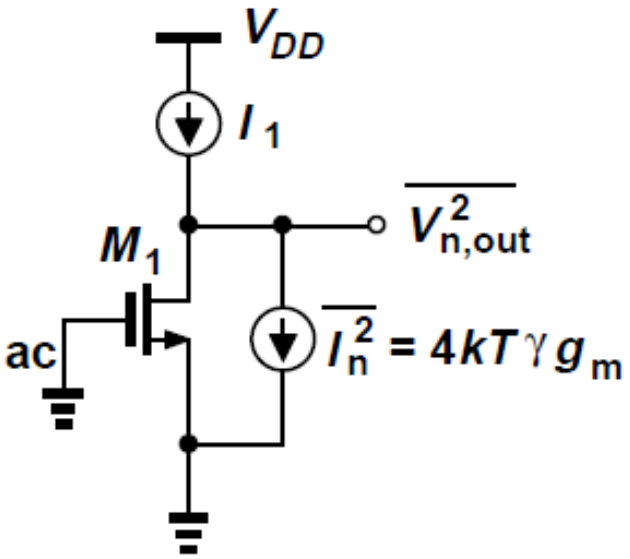
MOSFET Thermal Noise: Example



$$S_{out}(f) = S_{in}(f)|H(f)|^2$$

$$\overline{V_n^2} = \overline{I_n^2} r_O^2$$

$$= (4kT\gamma g_m) r_O^2$$

- **Input is set to zero for noise calculation**
- **The output resistance r_o does not produce noise because it is not a physical resistor**

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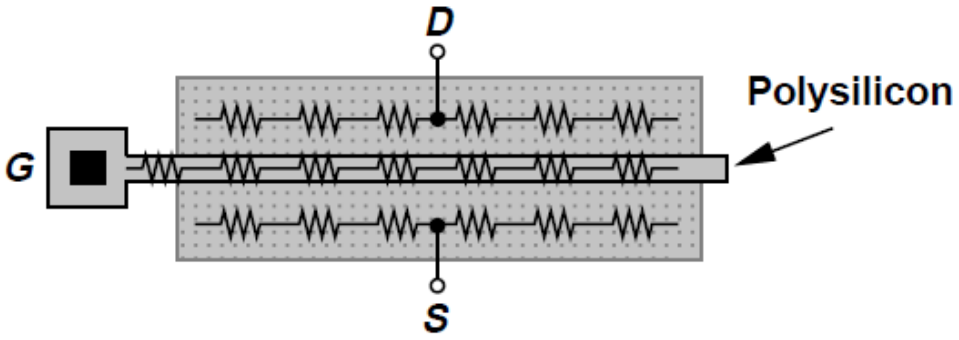
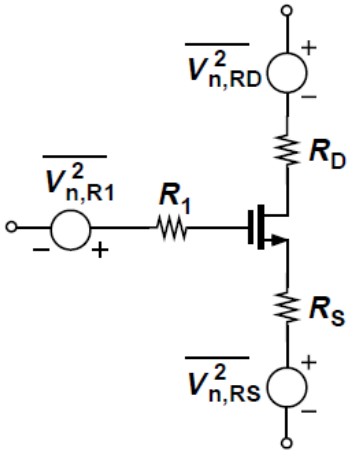
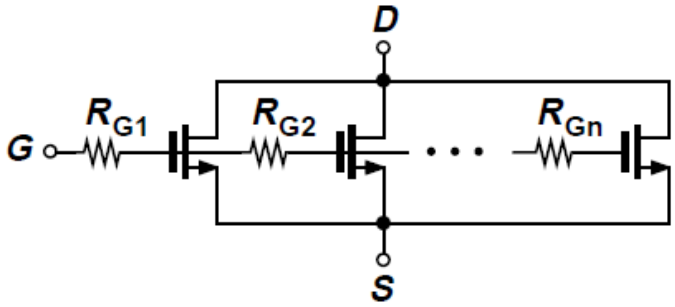
MOSFET Thermal Noise



(a)



(b)



$$R_{G1} + R_{G2} + \cdots + R_{Gn} = R_G$$

(c)

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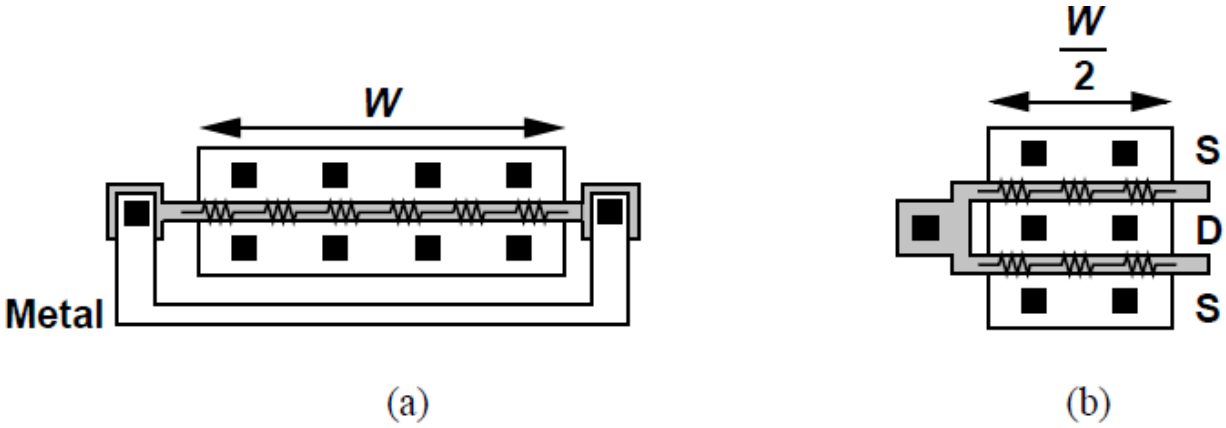
MOSFET Thermal Noise



- Effect of R_G can be reduced by proper layout
- For total gate resistance of R_G, equivalent noise resistance is $R_G/3$ (Distributed effects).

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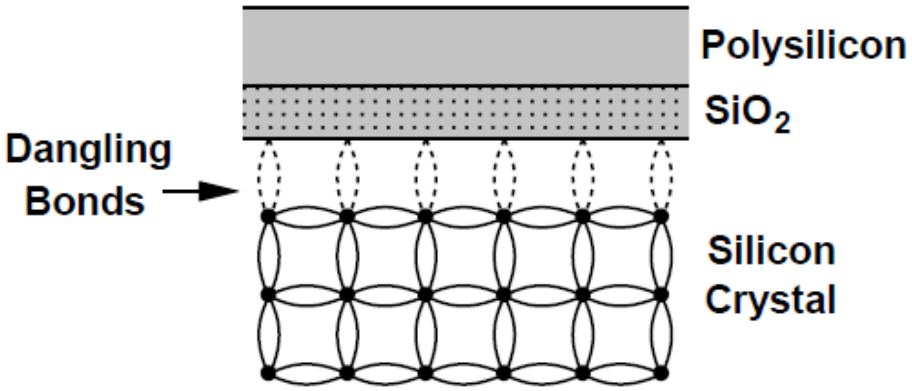
Flicker Noise



- "dangling" bonds giving rise to extra energy states
- Charge carriers moving at the interface are randomly trapped and later released by such energy states, introducing "flicker" noise in the drain current
- Depnds on cleanness of oxide-silicon interface and CMOS technology

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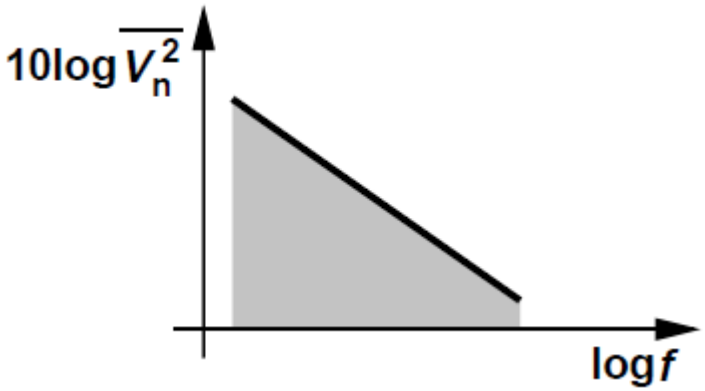
Flicker Noise

- **Modeled as a voltage source in series with the gate and in the saturation region, is roughly given by**

$$\overline{V_n^2} = \frac{K}{C_{ox} W L} \cdot \frac{1}{f}$$

- ***K* is a process-dependent constant on the order of 10^{-25} V^2F**
- ***Larger Area – Averaging effect – Less Flicker***



- **PMOS devices better *1/f* noise**

→ **Holes are carried in a "buried" channel, below oxide-silicon interface**

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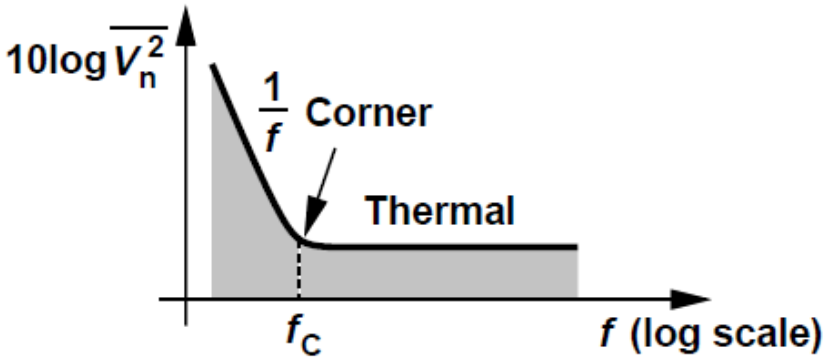
Flicker Noise Corner Frequency

- **At low frequencies, the flicker noise power approaches infinity**
- **Intersection point of thermal noise and flicker noise spectral densities is called "corner frequency" f_c**

At f=f_c ,
Thermal noise = Flicker noise. i.e.,

$$4kT\gamma g_m = \frac{K}{C_{ox}WL}\cdot\frac{1}{f_c}\cdot g_m^2$$



that is,

$$f_c = \frac{K}{\gamma C_{ox}WL}\cdot g_m\frac{1}{4kT}$$

$$f_c \approx \frac{K}{\gamma}.\omega_t.\frac{1}{4kT} \quad \text{and} \quad \omega_t \propto \frac{1}{L^2}$$

Hence, the f_c increases with technology scaling.

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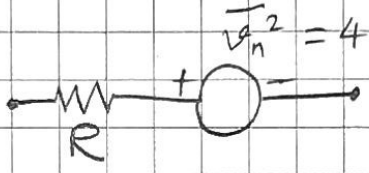
NOISE

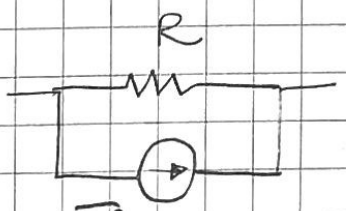
Repeat
Motivation: Why we are studying Noise?

Recap

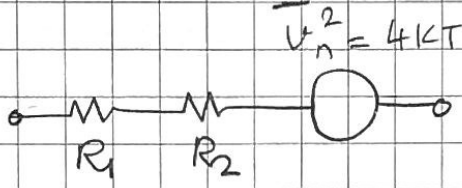


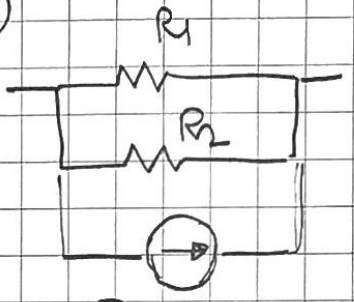
Noiseless

NOISELESS



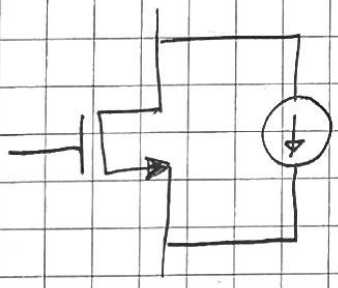
$\overline{i_n^2} = \frac{4KT}{R}$





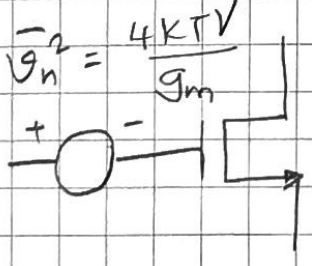
$\overline{i_n^2} = \frac{4KT}{(R_1 \| R_2)}$

MOSFET Thermal Noise



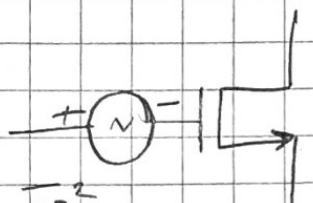
$\overline{i_n^2} = 4KT\gamma g_m$

Excess Noise Coeff. = 2/3 long ch
= 2-3 sh. ch.



r_o – Not physical resistor
– does not produce Noise

MOS FLICKER NOISE



$$\overline{V_{n,1/f}^2} = \frac{K_{1/f}}{C_{ox} W L} \cdot \frac{1}{f}$$

MOS in saturation region.

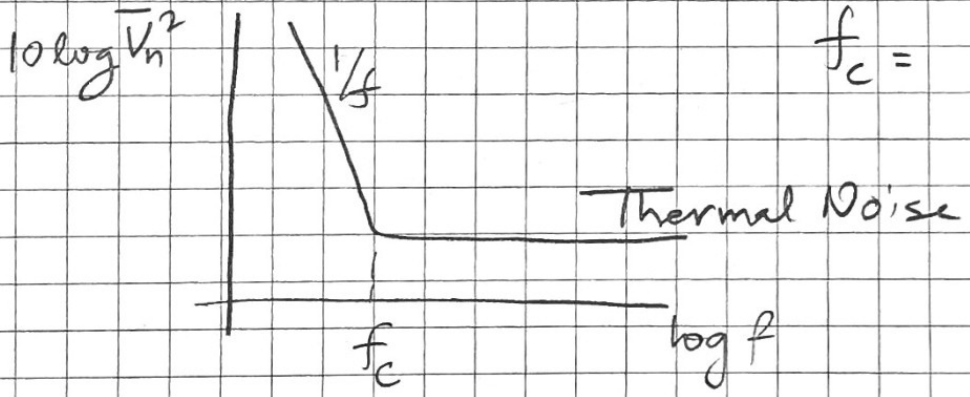
$K_{1/f}$ — process dependent $10^{-25}\ V^2F$

WL — Area ↑ — flicker ↓

Pmos — better 1/f

└ hole transport in buried channel

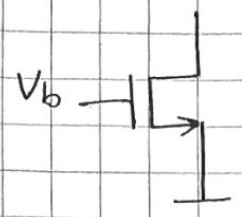
1/f corner



$$f_c = \frac{K_{1/f}}{4KT\gamma} \cdot \frac{g_m}{WLC_{ox}}$$

ω_T

Example: Calculate Thermal & flicker noise for nmos current source. (BW – 1KHz – 10MHz)



Assume $g_m = 1mS$

$C_{gs} = 50\,fF$

$K_{1/f} = 10^{-25}\,V^2F$

(integrated) $\overline{i_{n,thermal}^2} = 4KT\gamma g_m (10^7 - 10^3)$

$= 4 \times 1.38 \times 10^{-23} \times 300 \times \frac{2}{3} \times 1 \times 10^{-3} \times 10^7$

$\doteq 1.1 \times 10^{-16}\ A^2$

$\overline{i_{n\,rms}} = 10.48\ nA_{rms}$. (integrated)

FLICKER NOISE $\overline{i_{n\,1/f}^2} = \frac{K_{1/f}}{C_{ox} W \cdot L} \cdot \frac{1}{f} \cdot g_m^2$

$= \frac{10^{-25}\,V^2F}{50\,fF} \times \frac{(1mS)^2}{f} = \frac{2 \times 10^{-18}}{f}\ (A^2/Hz)$

Total 1/f noise (integrated)

$= \int_{1K}^{10M} \frac{2 \times 10^{-18}}{f}\, df = 2 \times 10^{-18} \ln\left(\frac{10M}{1K}\right)$

$= 18.42 \times 10^{-18}\ A^2$

$\overline{i_{n\,1/f\,rms}} = 4.29\ nA_{rms}$.

$$\overline{i_{n\,1/f}^2} = K' \ln\left(\frac{f_H}{f_L}\right)$$

(total integrated noise)

$f_L \to 0 \rightarrow$ Extremely slow noise components.

$0.01\,Hz \rightarrow 10\,s$; $10^{-6}\,Hz \rightarrow 1$ day

@ Slow rate - noise indistinguishable from thermal drift & aging.

* Voice Band (20 Hz - 20 KHz)

1/f below 20 Hz - insignificant corruption of signal.

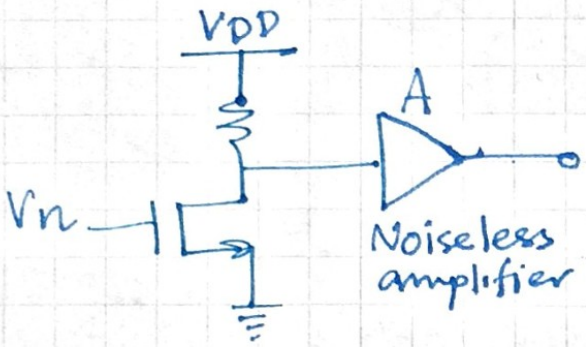
* Total integrated 1/f noise $= K' \ln\left(\frac{f_H}{f_L}\right)$

$K' \ln(10000) = 9.21\,K'$

$K' \ln(1 \times 10^6) = 13.8\,K'$

Taking f_L lower doesn't ~~ing~~ increase integrated noise as fast. - due to "ln" function.

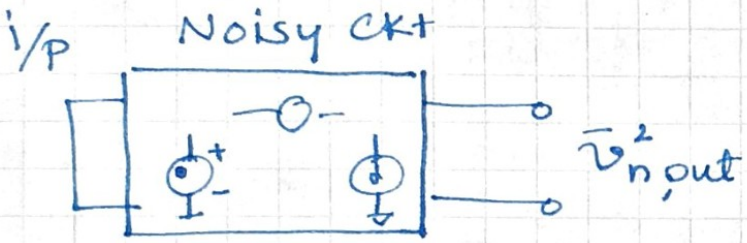
Concept of input referred noise.

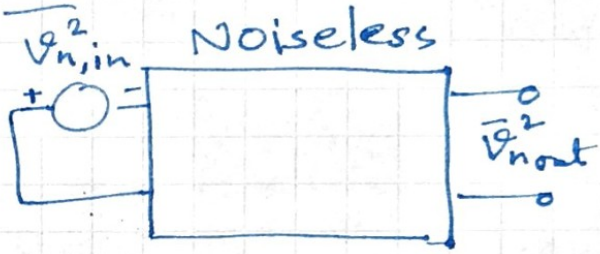


As A ↑ o/p noise ↑.

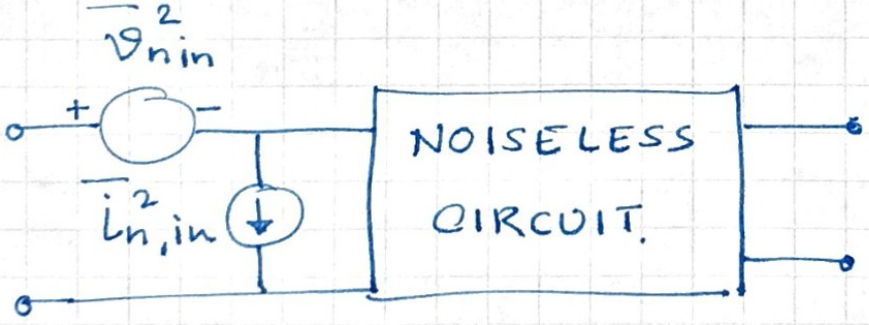
→ A ↑ Signal ↑.

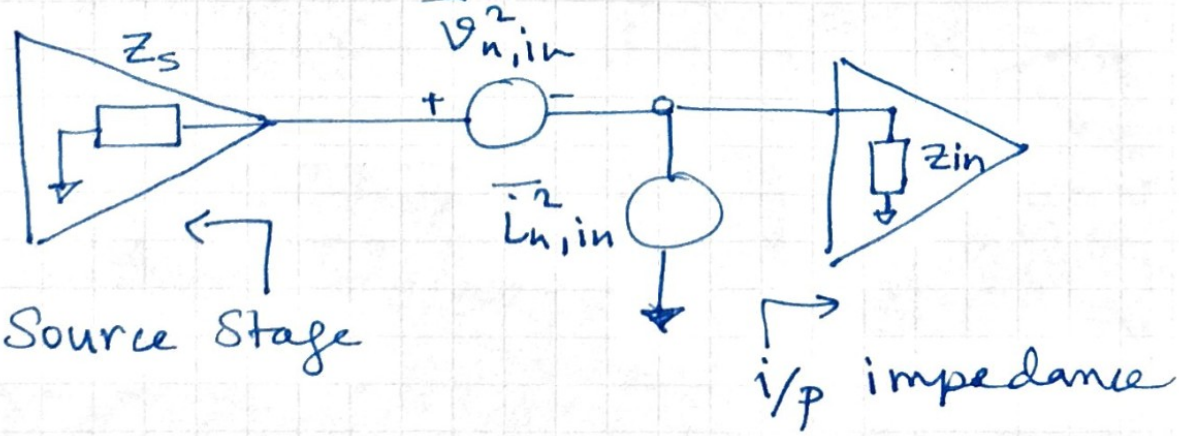
SNR – i/p referred noise.



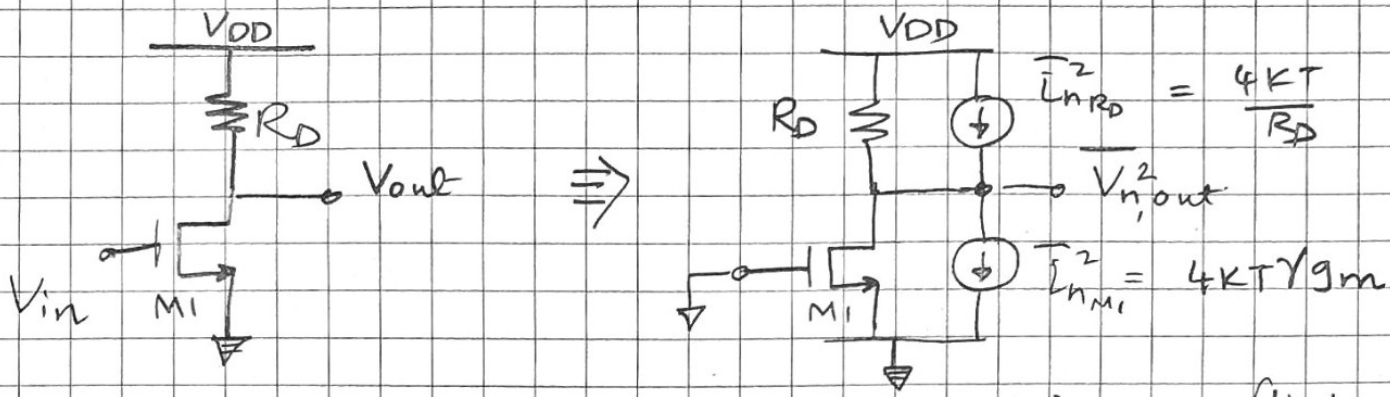


✡ To account for input ~~source~~ impedance of the circuit & source impedance.



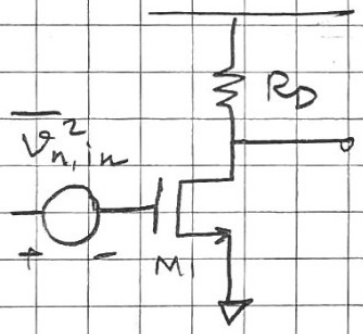


Noise Analysis Examples



(ignoring flicker)

$$\overline{V_{n,out}^2} = \left(\frac{4KT}{R_D} + 4KT\gamma g_m\right) R_D^2 \qquad (R_D \ll r_o)$$



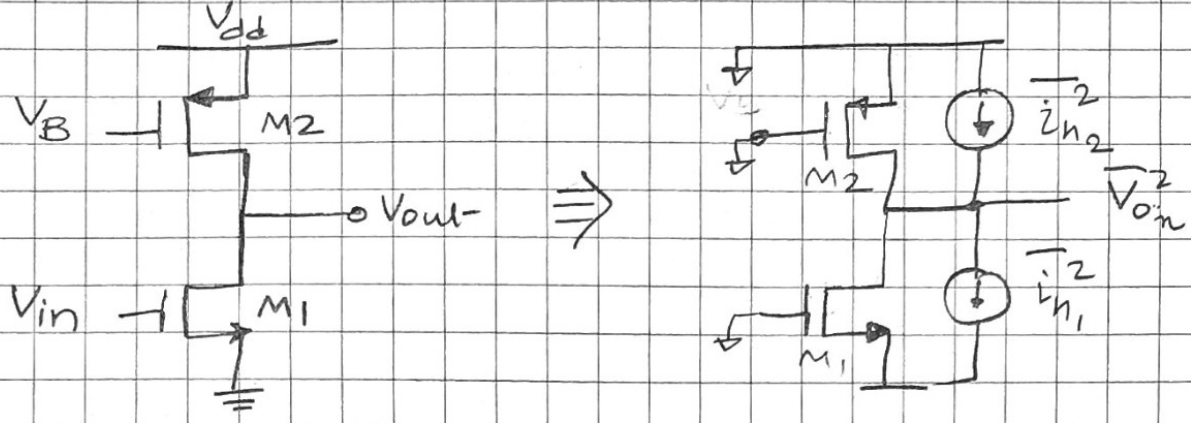
$$\overline{V_{n,in}^2} = \frac{\overline{V_{n,out}^2}}{A_V^2} = \frac{\overline{V_{n,out}^2}}{(g_m R_D)^2}$$

$$= \left(\frac{4KT}{R_D} + 4KT\gamma g_m\right) \frac{R_D^2}{(g_m \cdot R_D)^2}$$

$$= \frac{4KT}{g_m}\left(\frac{1}{g_m R_D} + \gamma\right)$$

(ONLY THERMAL NOISE CONSIDERED)

Example 2. CS AMP



$$\overline{v_{o_n}^2} = \left(4KT\gamma_n g_{m_1} + 4K\gamma_p g_{m_2}\right) r_{out}^2$$

$$\text{Gain} = A_0 = g_{m_1} r_{out}$$

$$\overline{v_{o,in}^2} = \left(4KT\gamma_n g_{m_1} + 4KT\gamma_p g_{m_2}\right) \frac{r_{out}^2}{g_{m_1}^2 r_{out}^2}$$

$$= \frac{4KT\gamma_n}{g_{m_1}} + \frac{4KT\gamma_p}{g_{m_2}} \left(\frac{g_{m_2}}{g_{m_1}}\right)^2$$

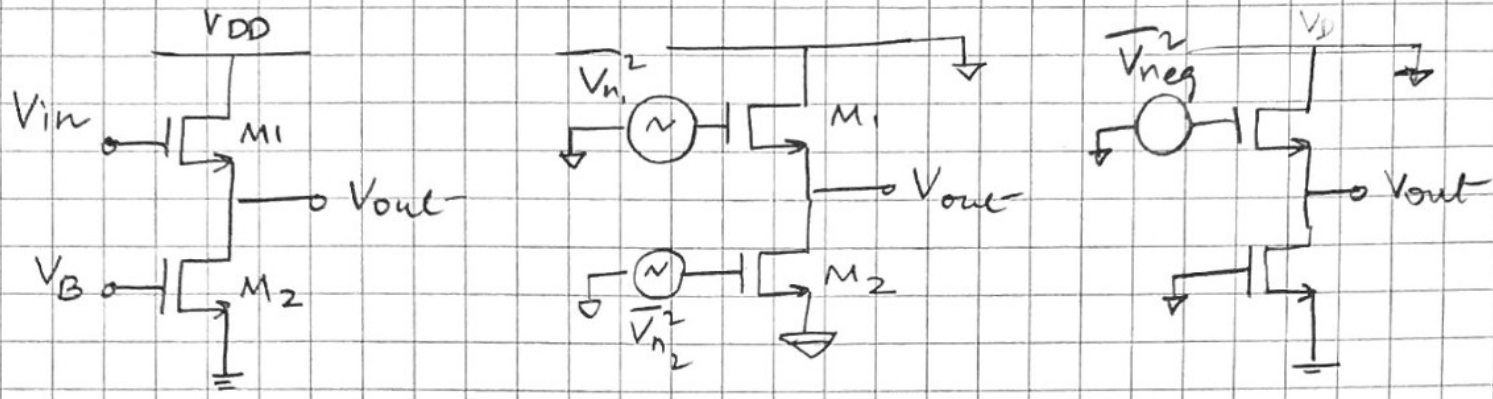
↑ i/p refered due to M_1 only.

→ Keeping g_{m_1} high. Reduces contributions of current source.

$$= \overline{v_{n_1}^2} + \overline{v_{n_2}^2} \left(\frac{g_{m_2}}{g_{m_1}}\right)^2$$

Gate Refered Noise of Each transistor.

Example 3 SOURCE FOLLOWER



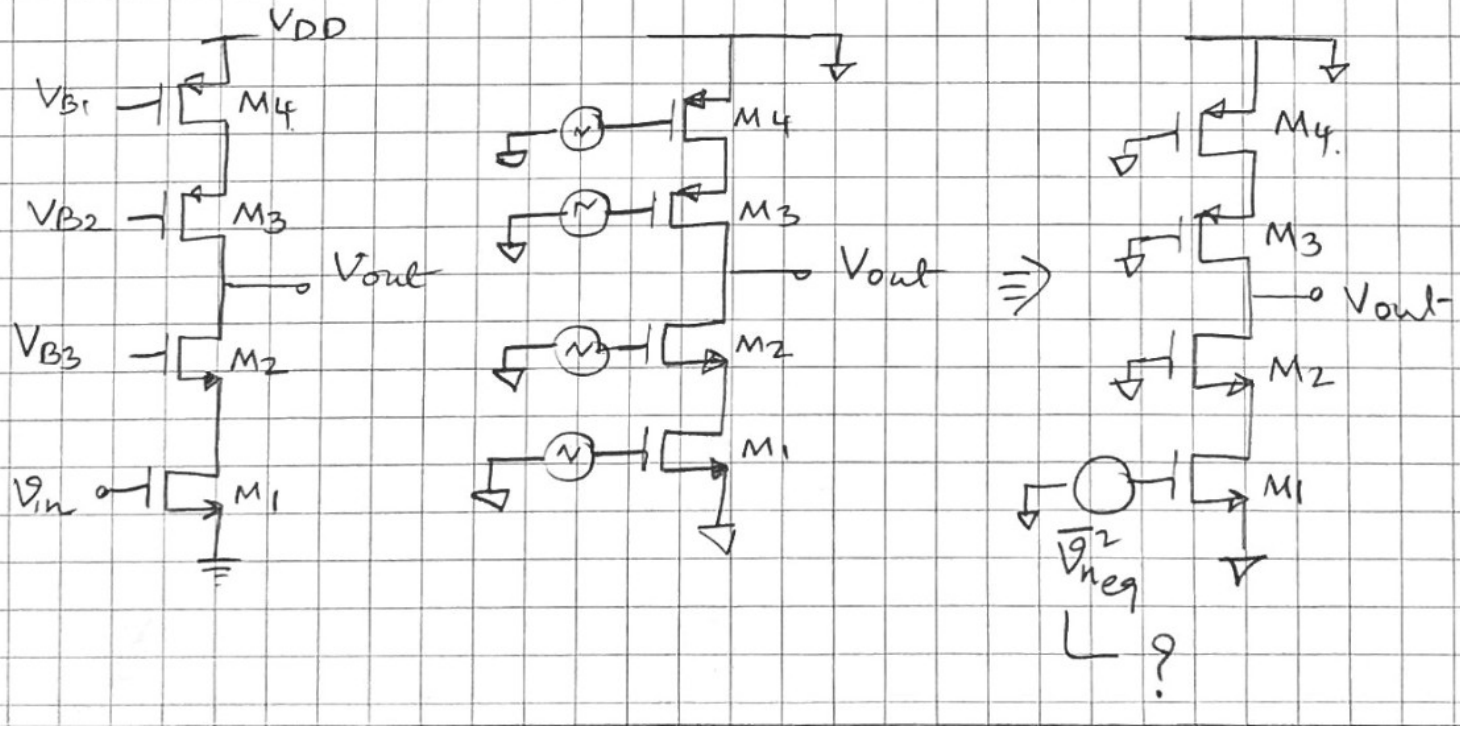
Using superposition

$$\overline{V_{out}^2} = \overline{V_{n_1}^2} + \overline{V_{n_2}^2}\left(\frac{g_{m_2}}{g_{m_1}}\right)^2 = \overline{V_{neq}^2}$$

(Since $A_V = 1$ unity gain)

$$\overline{V_{neq}^2} = \left(\overline{V_{n_1}^2} + \overline{V_{n_2}^2}\left(\frac{g_{m_2}}{g_{m_1}}\right)^2\right)$$

Example 4 CASCODE CS AMP.

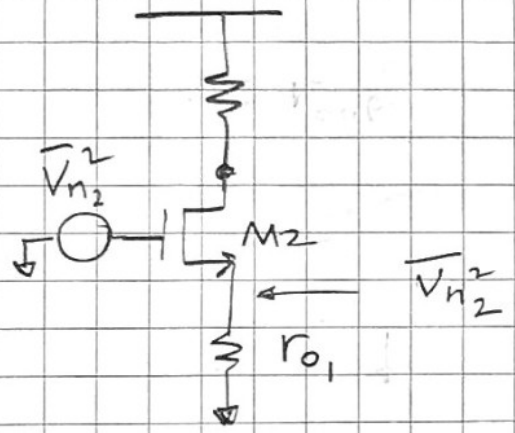


Consider M_1 & M_4 only.

$$\overline{V_{neq}^2} = \overline{v_{n_1}^2} + \overline{v_{n_4}^2}\left(\frac{g_{m_4}}{g_{m_1}}\right)^2$$

(Based on previous example)

Imp point Cascode $\leftrightarrow$ Noise ?

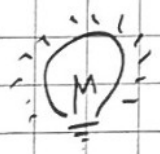


$$\overline{v_{nout}^2} = \frac{\overline{v_{n_2}^2}}{r_{o_1}^2} \times r_{out}^2$$

i/p referred to gate of M_1

$$\overline{V_{neq}^2} = \frac{\overline{V_{n_2}^2}}{r_{o_1}^2} \times \frac{r_{out}^2}{g_{m_1}^2 r_{out}^2}$$

$$= \frac{\overline{V_{n_2}^2}}{(g_{m_1} r_{o_1})^2}$$



Insight Cascode Noise contributions divided by $(g_m r_o)$

Large #

Same applicable to M3.

By superposition

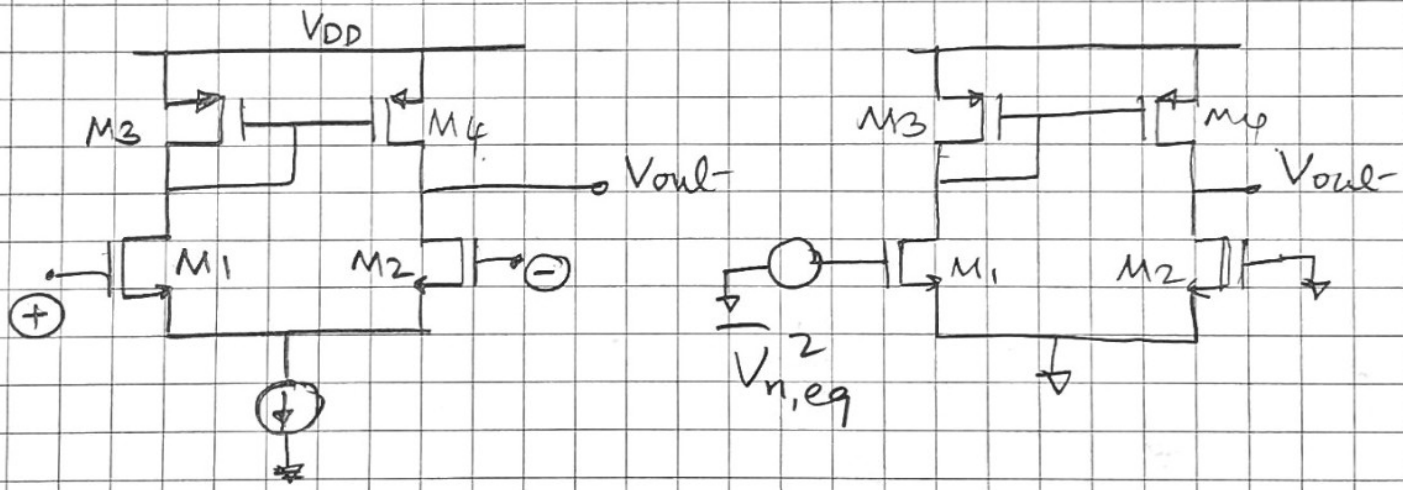
$$\overline{V_{neq}^2} = \overline{v_{n1}^2} + \overline{v_{n4}^2}\left(\frac{g_{m4}}{g_{m1}}\right)^2 + \frac{\overline{v_{n2}^2}}{(g_{m1}r_{o1})^2} + \frac{\overline{v_{n3}^2}}{(g_{m1}r_{o4})^2}$$

Cascode contribution

Cascode generally does not degrade noise performance.

Example: 5

CMOS DIFF AMP



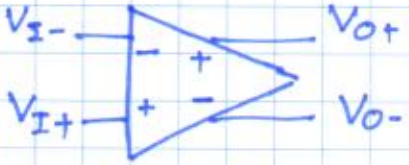
$$\overline{V_{n,eq}^2} = 2\left[\overline{v_1^2} + \overline{v_3^2}\left(\frac{g_{m3}}{g_{m1}}\right)^2\right]$$

(PROVE URSELF)

Standard Differential Amplifier (Lecture 7)

- → Differential i/p
- → Common-mode (i/p) is rejected by diff pair with current source
- → Single-Ended Output (DE to SE conversion) using mirror.

Std. Diff. Amplifier



Fully Differential Amplifier

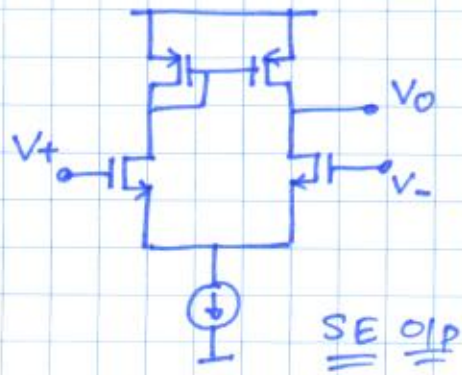
Fully. Differential Amplifier

- → Differential i/p, Differential O/p.
- → i/p common-mode is rejected by i/p diff pair
- → O/p common-mode set independently

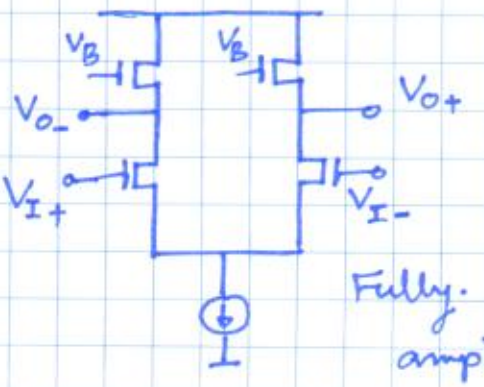
Why?

- ✡ Increased (double) O/p swing.
- ✡ Excellent Power Supply rejection
- ✡ Immune to noise coupling from any external sources.
- ✡ Improved freq. response ← NO DE2SE conversion

Simplest Example

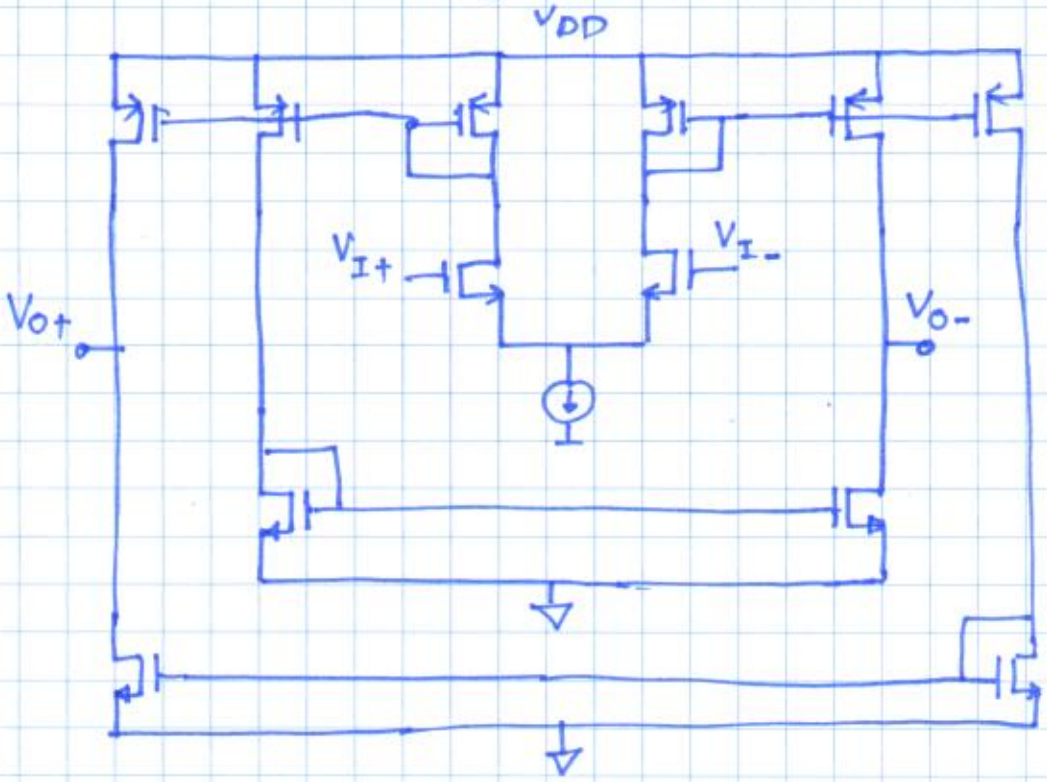


SE O/P

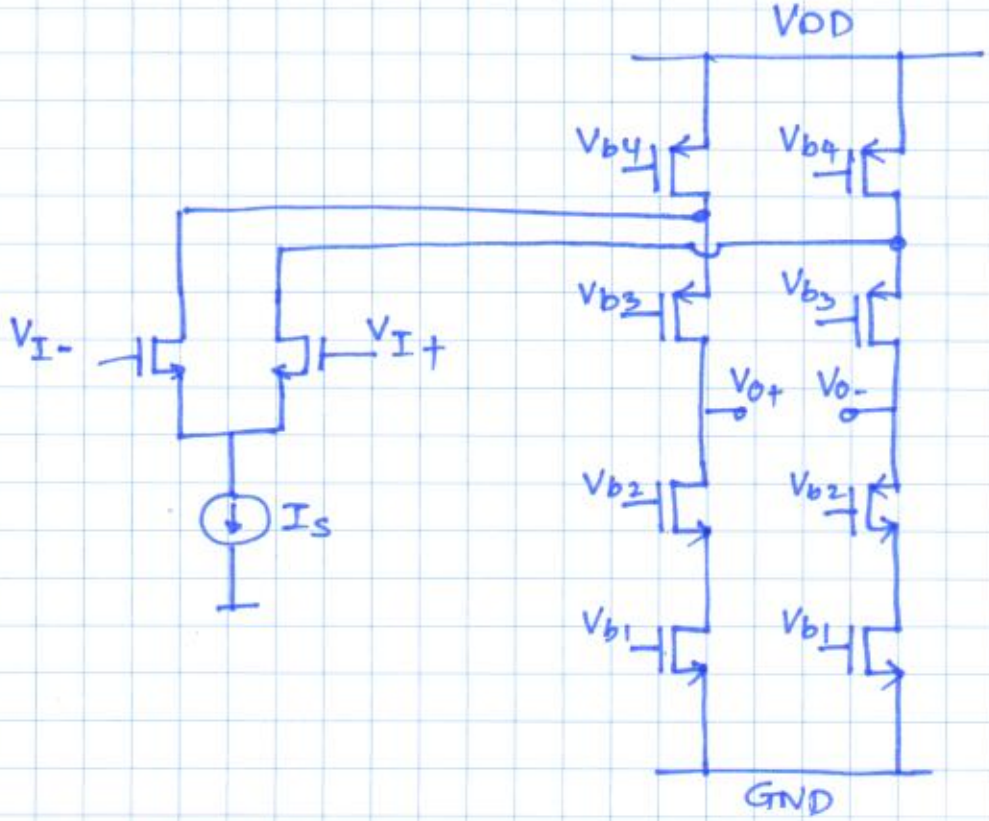


Fully. Diff. amplifier

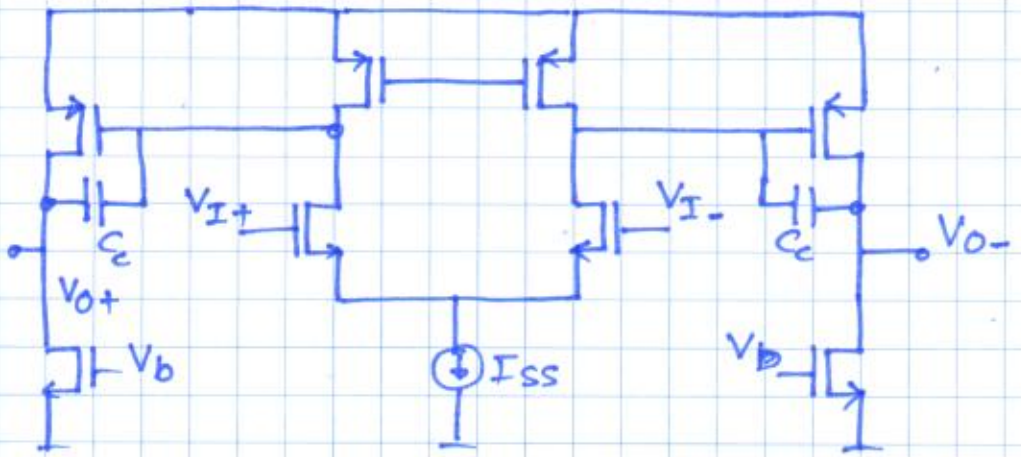
Examples of fully. differential Amplifiers



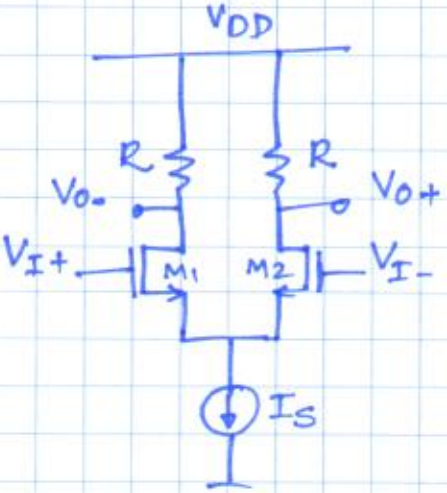
Fully Diff Folded Cascode Opamp



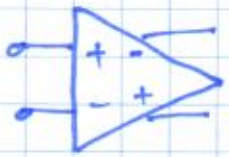
Fully-Differential Two Stage Opamp



Consider Simple diff pair with Rload. (fully diff)



$\Rightarrow$

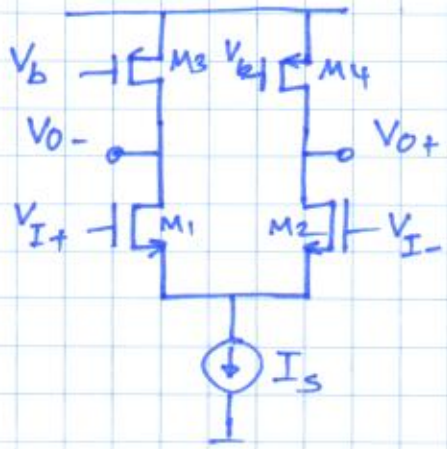


Assume: $V_{I+} = V_{I-} = V_{ICM}$.

M_1, M_2 sat.

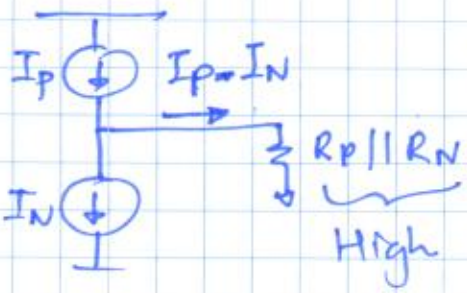
$V_{OCM} = V_{DD} - \frac{I_S}{2} R$ ← very well defined.

Current Source loading — High Gain



For common mode i/p V_{ICM}.

Assume all Transistor in Sat.



V_{OCM} undefined

I_P ; I_N are defined by process, temp, voltage
→ will change.
∴ → Even mismatches will impact V_{OCM}.

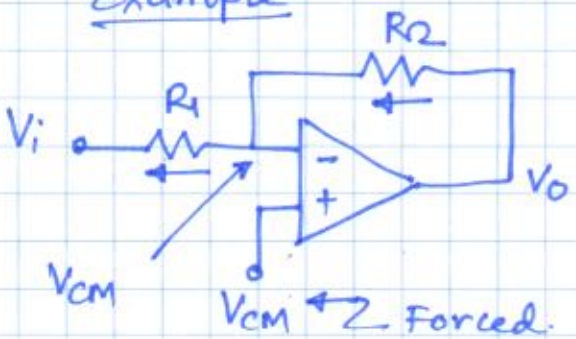
→ Tweeking I_P, I_N to get $V_{OCM} = V_{DD}/2$

→ DOESNOT work – V_{OCM} will keep changing with PVT & mismatches.

→ Need Feedback at o/p to stabilize output common-mode voltage.

→ Note: Differential feedback does not correct common-mode.

Example

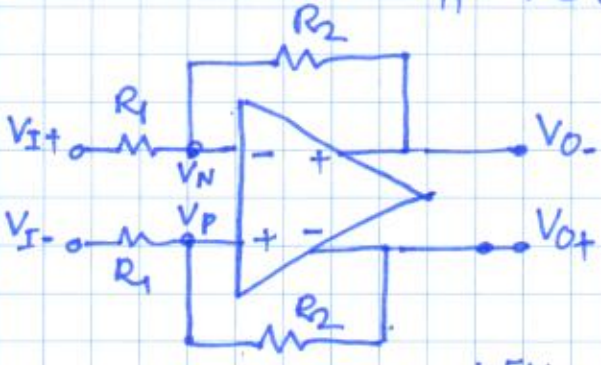


$$\frac{V_o - V_{CM}}{R_2} = \frac{V_{CM} - V_i}{R_1}$$

$$V_o = \frac{R_2}{R_1}(V_{CM} - V_i) + V_{CM}$$

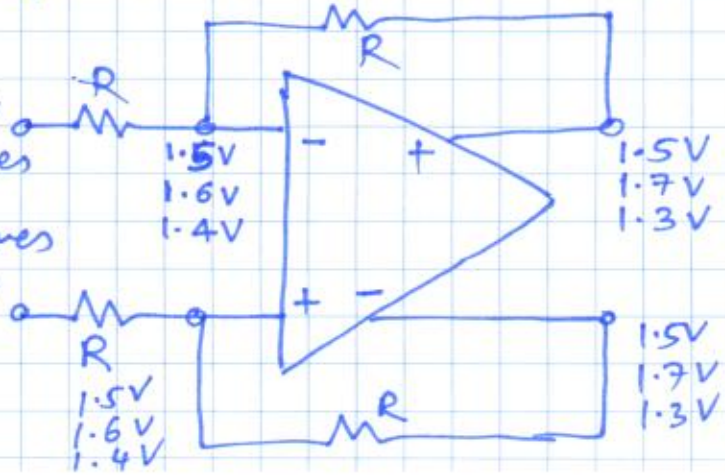
$$= -\frac{R_2}{R_1} V_i + \left(1 + \frac{R_2}{R_1}\right) V_{CM}$$

o/p DC (common Mode) very well defined.



Lets assume $(V_{I+}, V_{I-})_{CM} = V_{icm}$.
$= 1.5V$

$R_1 = R_2 = R$



V_P, V_N can take any values

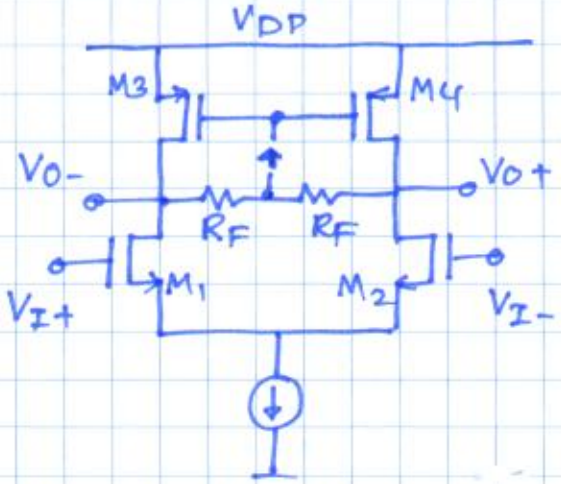
V_{op}, V_{o-} can take any values

o/p CM poorly defined

Need CMFB Common-Mode Feedback circuit

→ Required for high gain fully differential ckt.

Simple Example



Diff gain $g_{m_1}(r_{o_1} \| r_{o_3} \| R_F)$

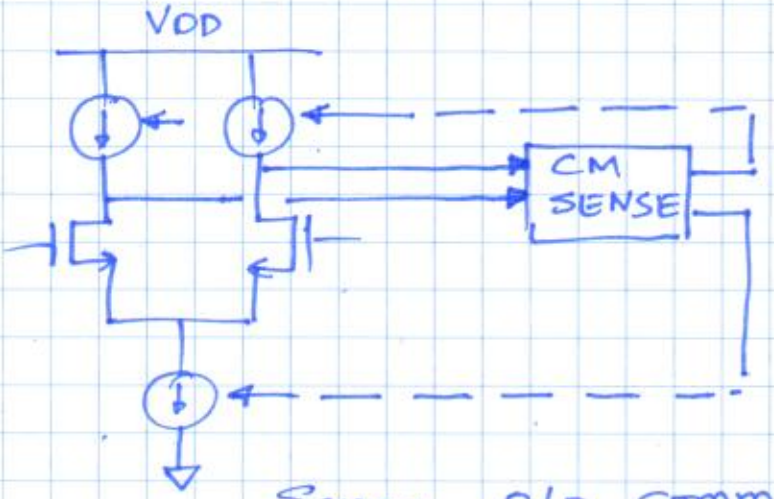
R_F → large.

O/p Common-mode

$$V_{OCM} = V_{DD} - |V_{GS_3}|$$

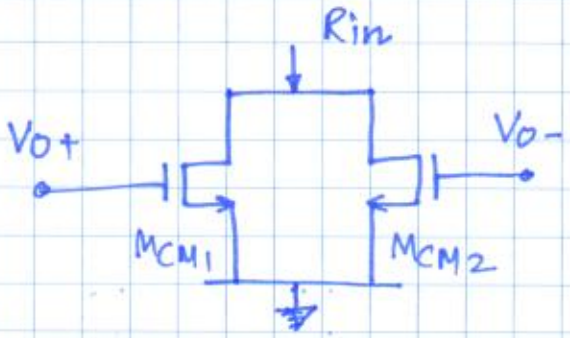
$$V_{DD\,min} = 2V_{dsat} + |V_{GS_3}| = 3V_{dsat} + |V_{T_P}|$$

Generic CMFB Strategy



Sense O/p common-mode voltage & adjust one of current sources.

CMFB using MOSFETs in triode region.



$$R_{in} = R_{CM1} \parallel R_{CM2}$$

↑ ↑

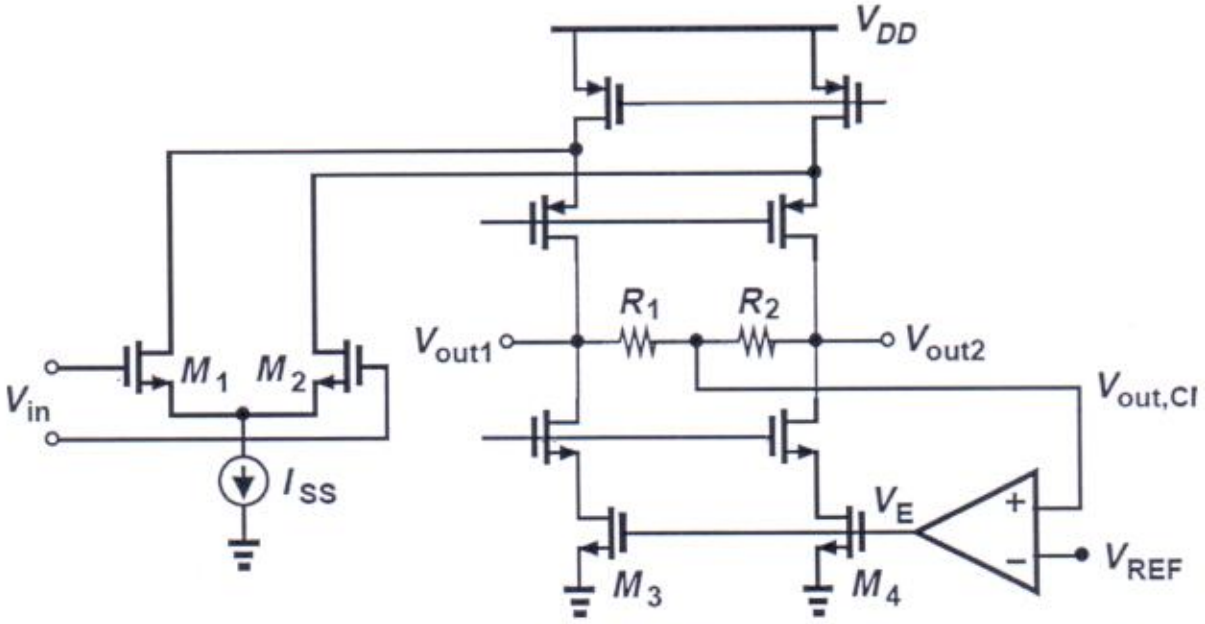
Triode region Resistance

$$R_{in} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{O+} - V_{TH})} \parallel \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{O-} - V_{TH})}$$

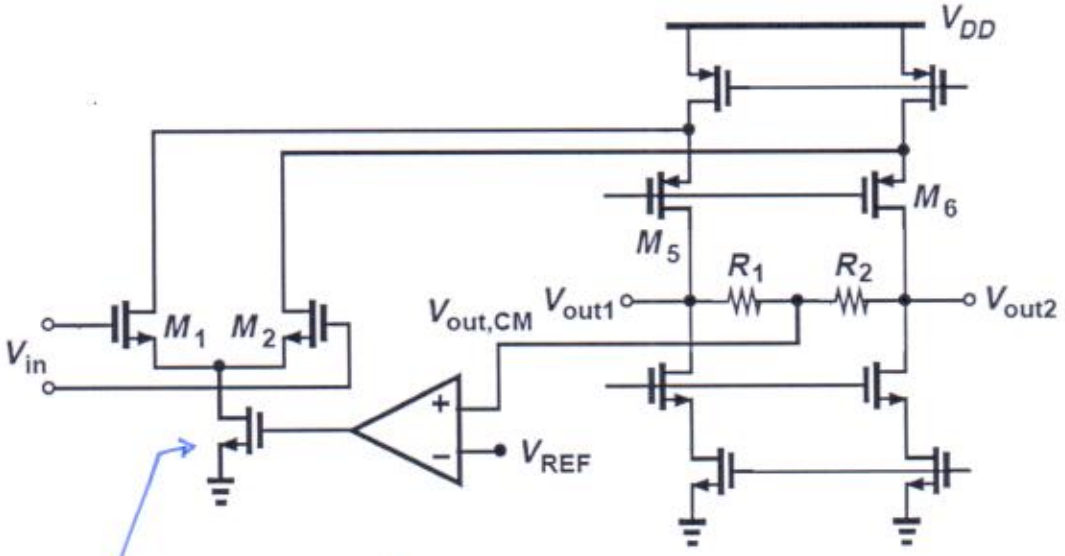
$$= \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{O+} + V_{O-} - 2V_{TH})}$$

$V_{O+} + V_{O-} \propto \frac{1}{V_{CM}}$ ← Independent of $(V_{O+} - V_{O-})$ (diff o/p voltage)

CMFB implementations (Folded-Cascode opamps)



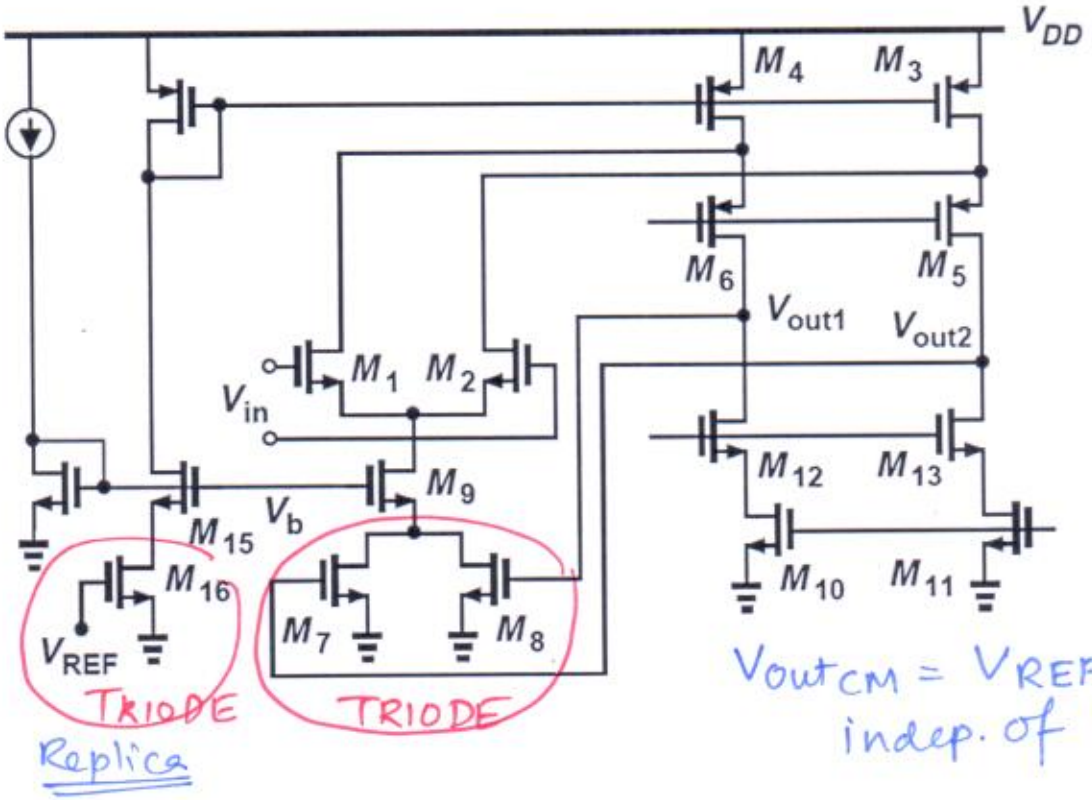
o/p current source control.



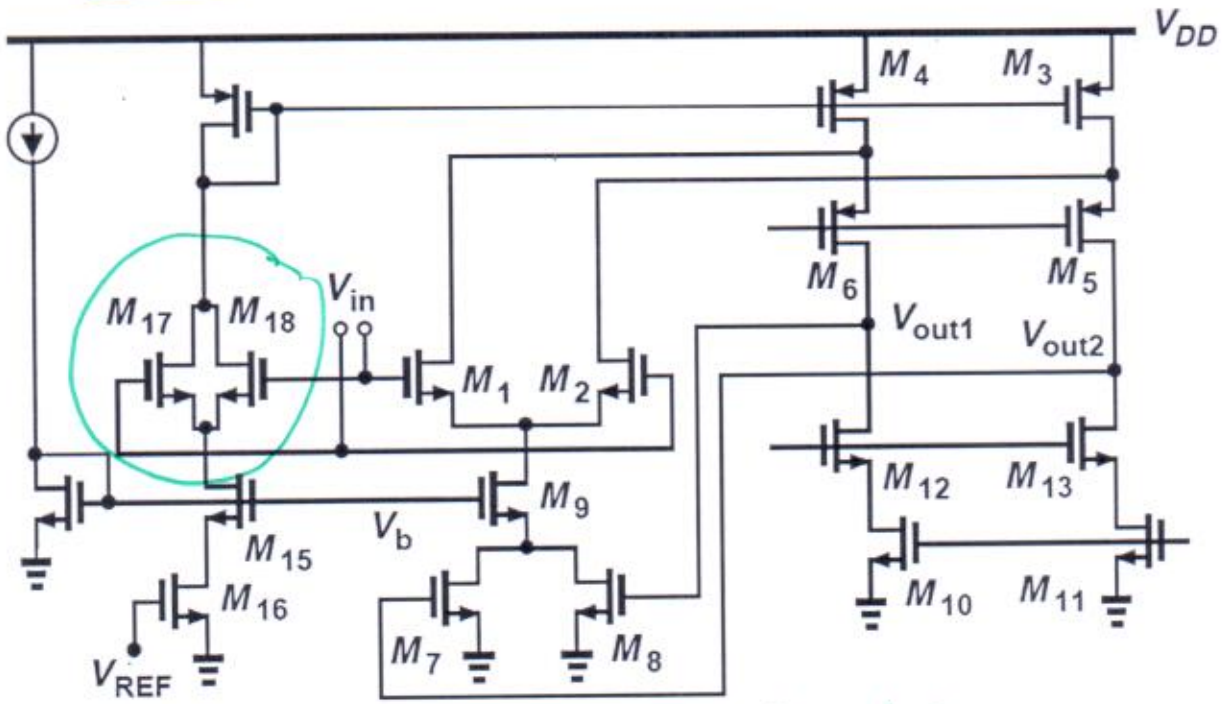
Diff pair tail current source control

Illustrations from Razavi Textbook

CMFB using triode region transistors



$V_{out_{CM}} = V_{REF}$ indep. of V_b.



M_{17} & M_{18} – Replica of diff pair

→ Make sure $V_{DS_{15}} = V_{DS_9}$

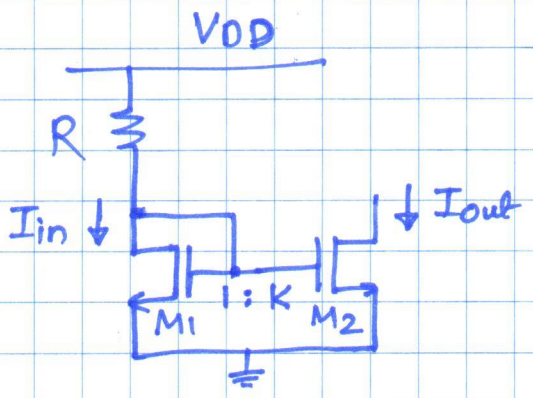
Indep. of Ch. length Mod?

REFERENCE CIRCUIT DESIGN.

* Voltage or Current Reference
* Process, Temperature or Supply independent
* Or. well-defined (predictable) dependence on Temp.

⇒ Goal - Overall Chip performance predictable / consistent over PVT. Yield. - Meet specs over PVT.

1. Supply Independent Current-source



$I_{in} = \frac{V_{DD} - V_{GS}}{R}$

$\Delta I_{in} = \frac{\Delta V_{DD} - \Delta V}{R}$

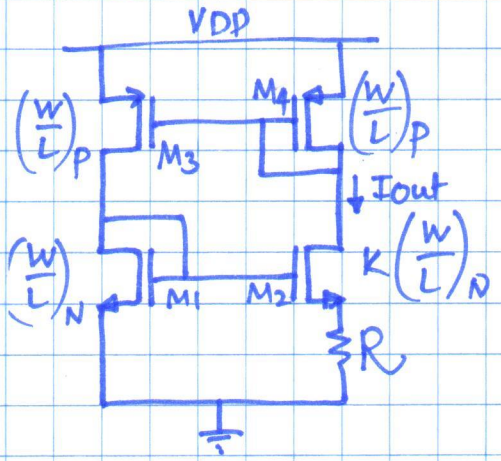
$\Delta V_{GS_1} = \frac{\Delta I_{in}}{g_{m_1}}$

$\Delta I_{in} = \frac{\Delta V_{DD}}{R + \frac{1}{g_{m_1}}}$

$\Delta I_{out} = K \frac{\Delta V_{DD}}{R + 1/g_{m_1}}$ ← fn of I & hence V_{DD}

No good. ☹

Consider



$V_{GS_1} = V_{GS_2} + I_{out} R$

$K_n = \mu_n C_{ox}$

$V_T + \sqrt{\frac{2 I_{out}}{K_n (W/L)_N}} = V_T + \sqrt{\frac{2 I_{out}}{K_n K (W/L)_N}} + I_{out} R$

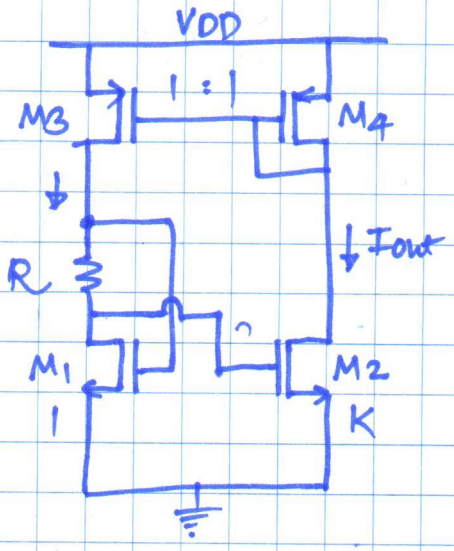
$\sqrt{I_{out}} = \frac{1}{R} \left[\sqrt{\frac{2}{K_N (W/L)_N}} \left(1 - \frac{1}{\sqrt{K}} \right) \right]$

$I_{out} = \frac{1}{R^2} \cdot \frac{2}{K_N (\frac{W}{L})_N} \left(1 - \frac{1}{\sqrt{K}} \right)^2$

→ indep of V_{DD} – dependson process & T & R value.

⊖ Body effect of M_2.

Improved circuit



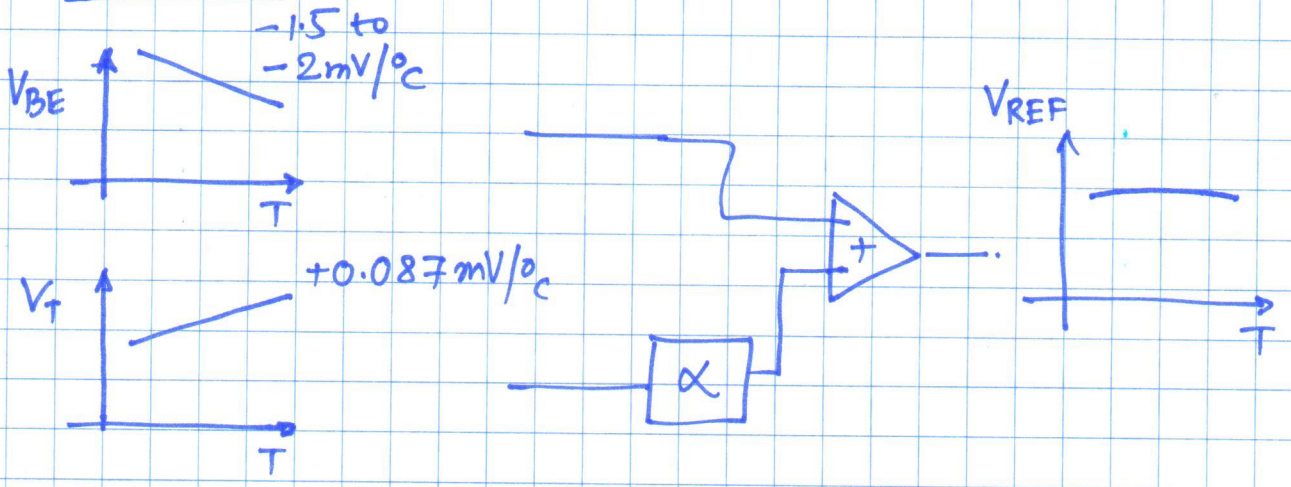
No Body effect for M_2.

Same Iout equation.

Use long channel devices to reduce Ch. length modulation.

Temperature Independent Reference

Concept



$$V_{REF} = V_{BE} + \alpha V_T$$

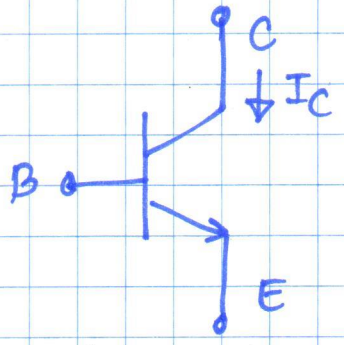
V_{BE}: -ve Temp Co

αV_T: +ve Temp Co

→ Process, Supply & Temp Independent

→ Need to use Bipolar Transistors

Bipolar Basics



$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right), \quad V_T = \frac{kT}{q}$$

Saturation current $\propto \mu k T n_i^2$

$\mu k T n_i^2$ ← (intrinsic carrier conc), Bandgap → 1.12 eV

mobility $\propto \mu_0 T^m$, $m \sim \left(-\frac{3}{2}\right)$; $\propto T^3 \exp\left[-E_g/kT\right]$

Overall $I_S = b\, T^{4+m} \exp\frac{-E_g}{kT}$

constant. indep. of T

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \cdot \ln\left(\frac{I_C}{I_S}\right) - \frac{V_T}{I_S}\frac{\partial I_S}{\partial T}$$

Simplification: I_C held constant

$$\frac{V_{BE}}{T} \qquad (4+m)\frac{V_T}{T} + \frac{E_g}{kT^2}V_T$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - E_g/q}{T}$$

Older Tech $V_{BE} = 0.7\,V$ $T = 300^\circ K$ $\Rightarrow \frac{\partial V_{BE}}{\partial T} \approx -1.9\,mV/^\circ K$

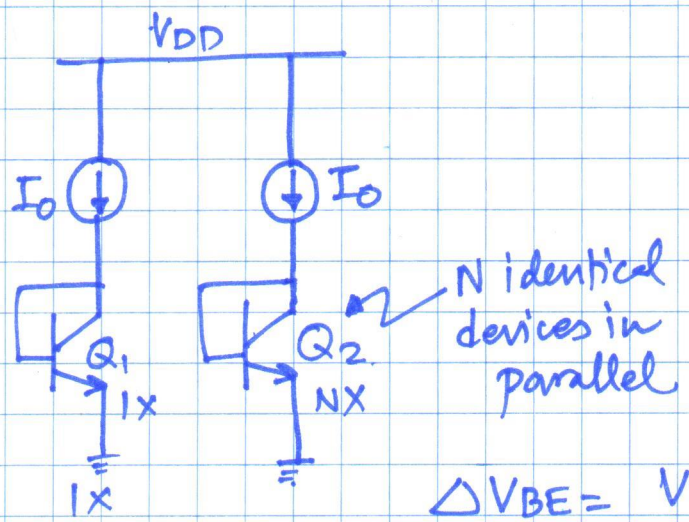
Modern Tech. $V_{BE} = 0.8\,V$ $T = 300^\circ K$ $\Rightarrow \frac{\partial V_{BE}}{\partial T} \approx -1.5\,mV/^\circ K$

NOTE: If you take into account collector current var^n ($I_C = \frac{V_T \ln N}{R}$), then equation modified as $(3+m)$ instead of $(4+m)$ (Razavi pp. 517)

How to generate the TC voltage?

PTAT Proportional to Absolute Temperature.

Hilbiber 1964



$$V_{BE_1} = V_T \ln\left(\frac{I_o}{I_s}\right)$$

$$V_{BE_2} = V_T \ln\left(\frac{I_o/N}{I_s}\right)$$

$$\Delta V_{BE} = V_{BE_1} - V_{BE_2}$$

$$= V_T \ln\left(\frac{I_o}{I_s}\right) - V_T \ln\left(\frac{I_o/N}{I_s}\right)$$

$$= V_T \ln(N) = \frac{kT}{q} \ln(N)$$

k, q constants $N \rightarrow$ scaling ratio

$\Delta V_{BE} \propto T$ indep of P.V.

$$V_{REF} = V_{BE} + \alpha V_T$$

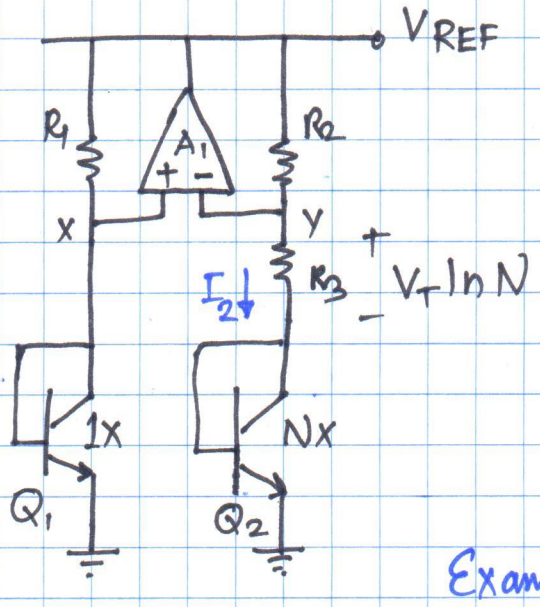
$-1.5\,mV/^\circ K$ $0.087\,mV/^\circ K$

$\alpha = 17.2$

$$V_{REF} = 800mV + (17.2 \times 26mV)$$

$$\cong 1.25\,V$$ (Bandgap Voltage)

Circuit Implementation

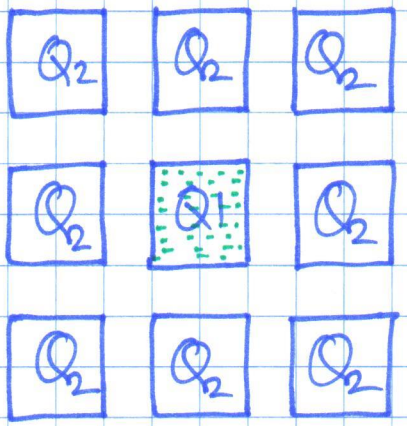


$$V_{REF} = (R_2+R_3)I_2 + V_{BE}$$

$$= V_{BE} + (R_2+R_3)\left(\frac{V_T \ln N}{R_3}\right)$$

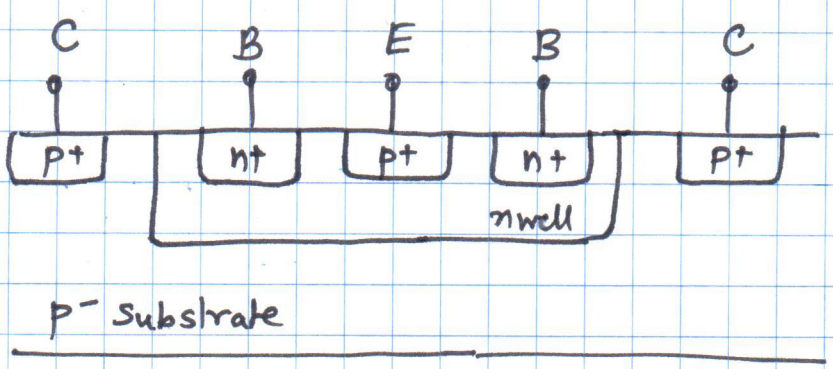
$$= V_{BE} + \left(1 + \frac{R_2}{R_3}\right) V_T \ln n.$$

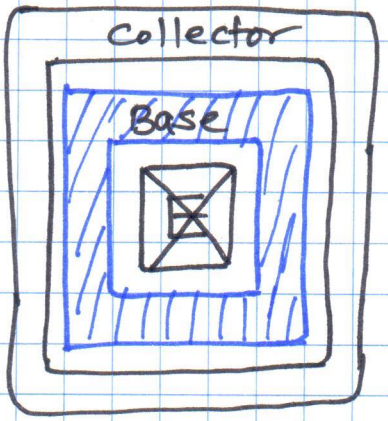
Example $n = 8$ $\quad \frac{R_2}{R_3} = 7.3$

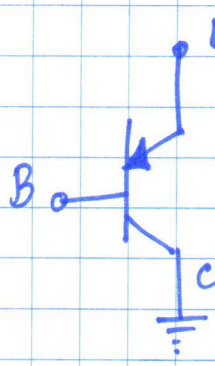


Common Centroid layout
— matching between Q_1 & Q_2

Bipolar Transistors in CMOS Technology

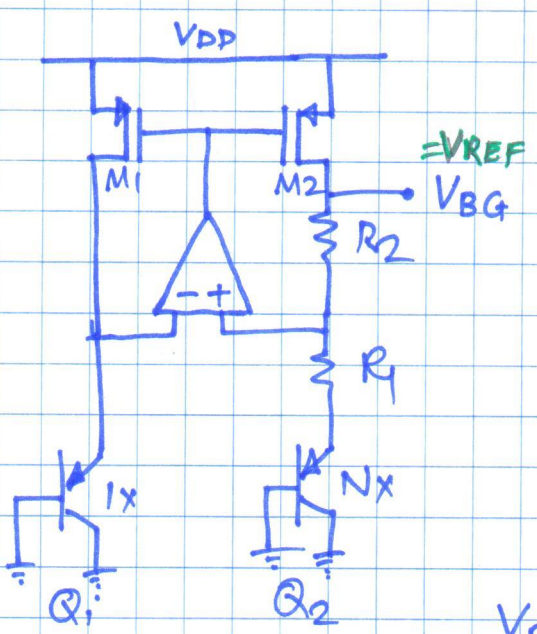






← Collector is always grounded [substrate]

CMOS implementation



$$x = \left(\frac{R_2+R_1}{R_1}\right)$$

$$V_{REF} = V_{BE} + xV_T \ln N$$

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{BE}}{\partial T} + x\frac{V_T}{T}\ln N = 0$$

for flat response...

$$-\frac{xV_T}{T}\ln N = \frac{V_{BE} - (4+m)V_T - E_g/q}{T}$$

Substitute

$$\Rightarrow xV_T \ln N = (4+m)V_T + \frac{E_g}{q} - V_{BE}$$

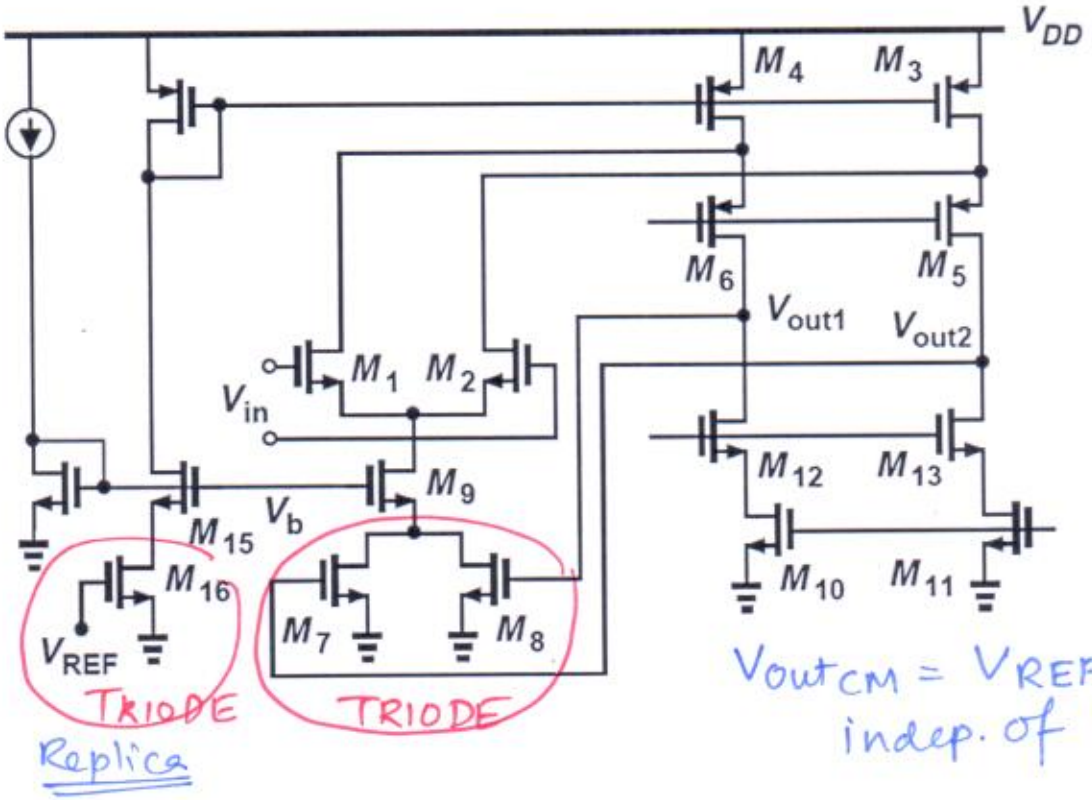
$$V_{REF} = \frac{E_g}{q} + (4+m)V_T$$

↑ μ Temp exponent

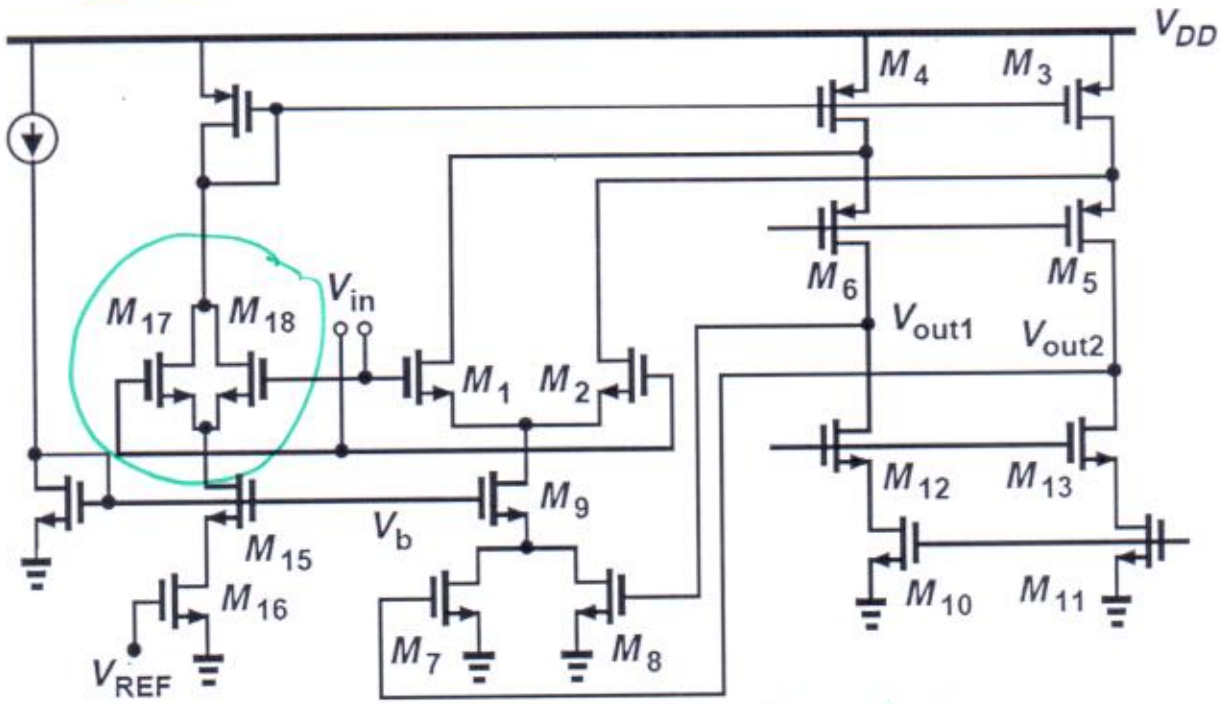
as $T \to 0$ $V_{REF} = \frac{E_g}{q}$ (Bandgap voltage)

Explain opamp +/- connection.

CMFB using triode region transistors



$V_{out_{CM}} = V_{REF}$ indep. of V_b.



M_{17} & M_{18} – Replica of diff pair

→ Make sure $V_{DS_{15}} = V_{DS_9}$

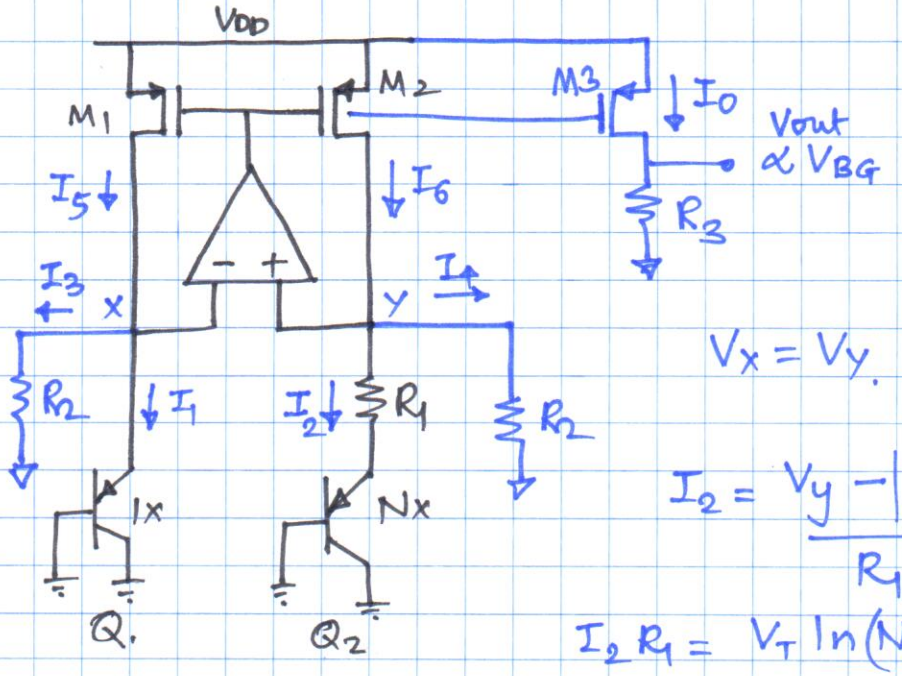
Indep. of Ch. length Mod?

Since $V_{REF} \cong 1.25V$ $V_{DD} > 1.25V$.

What about V_{REF} for $V_{DD} < 1V$.?

Reference

H. Banba "CMOS BGAP REF with Sub.1-V op" JSSC NOV 1997.



$V_x = V_y$ due to fbk (OPAMP)

$$I_2 = \frac{V_y - |V_{BE_2}|}{R_1} = \frac{|V_{BE_1}| - |V_{BE_2}|}{R_1}$$

$$I_2 R_1 = V_T \ln(N) \quad \text{—①}$$

Also $I_3 = I_4 = \frac{V_{BE1}}{R_2}$

$$I_6 = I_2 + I_4 = \frac{V_T \ln N}{R_1} + \frac{|V_{BE_1}|}{R_2} = \frac{1}{R_2}\left(|V_{BE_1}| + V_T \ln N \left(\frac{R_2}{R_1}\right)\right)$$

By choosing $\frac{R_2}{R_1}$. term inside brackets $= V_{BG}$

$$I_6 = \frac{V_{BG}}{R_2}$$

$$I_0 = \frac{V_{BG}}{R_2} \Rightarrow \boxed{V_{out} = \frac{R_3}{R_2} V_{BG}}$$

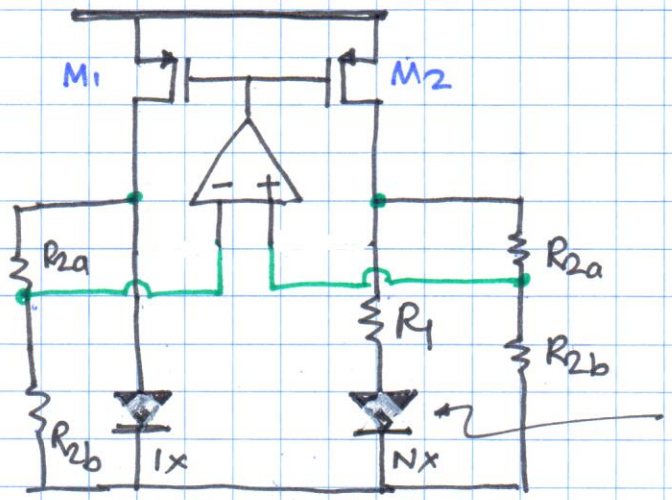
keep $\frac{R_3}{R_2} < 1$ for $V_{DD} < 1V$

Issue with Banba Bgap.

Nodes x & y DC voltage 0.7V — 0.9V ~

→ Input diff pair of opamp — Native NMOS ($V_T \simeq -0.2V$)

→ Leung / Mok solution | IEEE JSSC Apr. 2002 "A Sub-1-V 15-ppm/°C CMOS Bgap ...



Lower common mode i/p range of opamp using resistive divider.

V_{BE} junction shown as diode

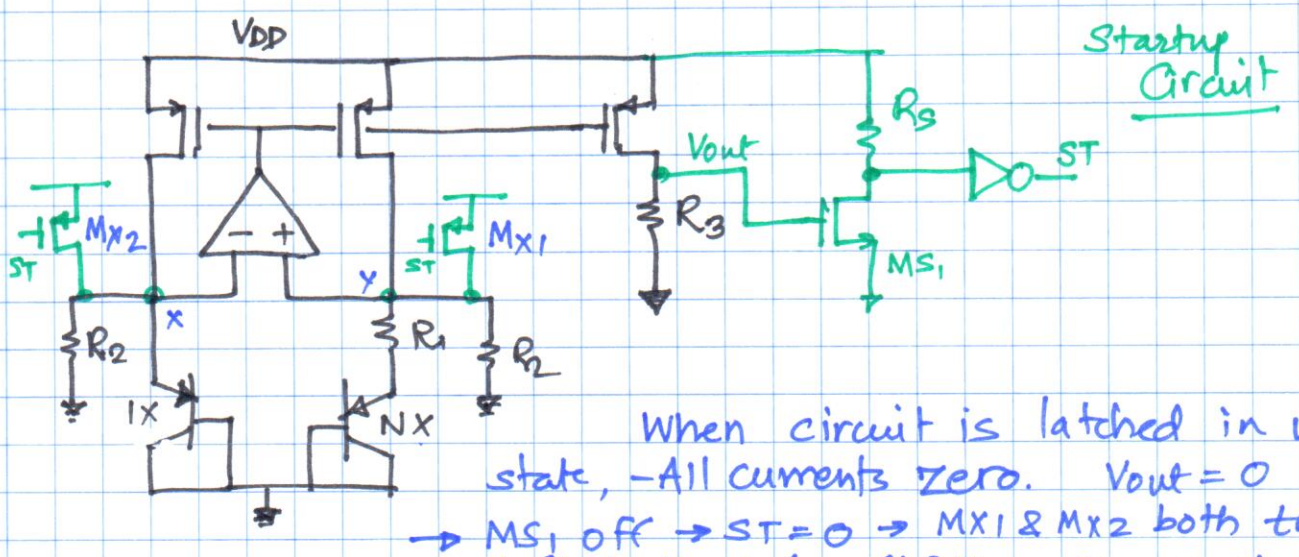
✱ Bandgap Startup Problem

→ Undesired Stable solution. - All currents zero.

→ Can be observed when you ramp up power supply.

→ Startup circuit detects this condition & pumps in juice to get to desired operation point.

Startup Solution (one possible)

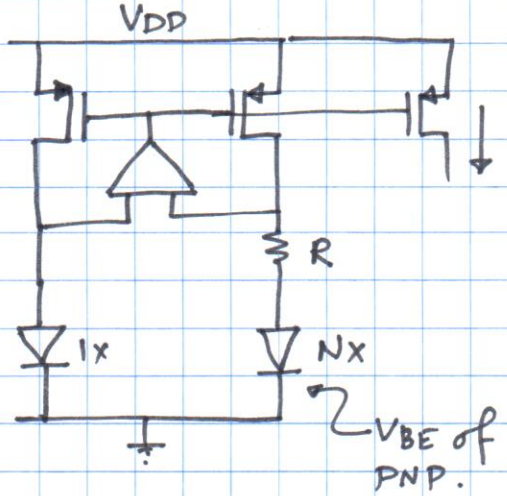


When circuit is latched in undesired state, -All currents zero. Vout = 0

→ MS1 off → ST = 0 → MX1 & MX2 both turn on

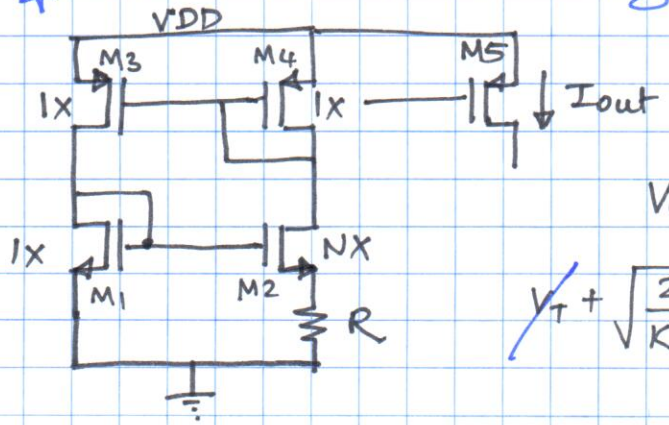
→ Lift both Nodes X & Y → Opamp starts to work.

✱ PTAT Current source



$$I_{out} = \frac{V_T \ln(N)}{R}$$

✱ Constant Gm Biasing → Gm → PVT independent



$$V_{GS_1} = V_{GS_2} + IR$$

$$V_T + \sqrt{\frac{2I}{K_n (W/L)_1}} = V_T + \sqrt{\frac{2I}{K_n N (\frac{W}{L})_1}} + IR$$

$$\Rightarrow I_{out} = I = \frac{2}{K_N\left(\frac{W}{L}\right)_1} \cdot \frac{1}{R^2} \cdot \left(1 - \frac{1}{\sqrt{N}}\right)^2$$

$$g_{m_1} = \sqrt{\underbrace{2\mu_n C_{ox}}_{K_N}\left(\frac{W}{L}\right)_1 I_1}$$

$$= \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_1 \times \frac{2}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}\left(\frac{1}{R^2}\left(1 - \frac{1}{\sqrt{N}}\right)^2\right)}$$

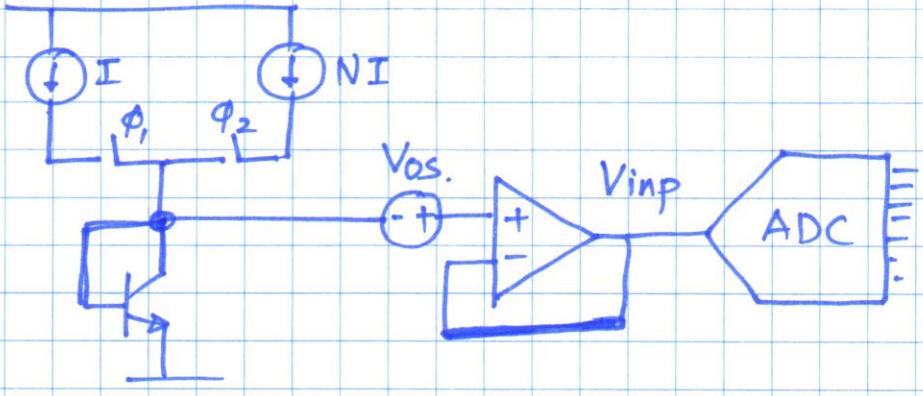
$$= \frac{2}{R}\left(1 - \frac{1}{\sqrt{N}}\right)$$

↑ on-chip or off chip

↖ Scaler Ratio

→ can be tuned digitally

On-Chip Temperature Sensor



In ϕ_1 $V_{inp} = V_{os} + V_T \ln\left(\frac{I}{I_s}\right)$

In ϕ_2 $V_{inp} = V_{os} + V_T \ln\left(\frac{NI}{I_s}\right)$

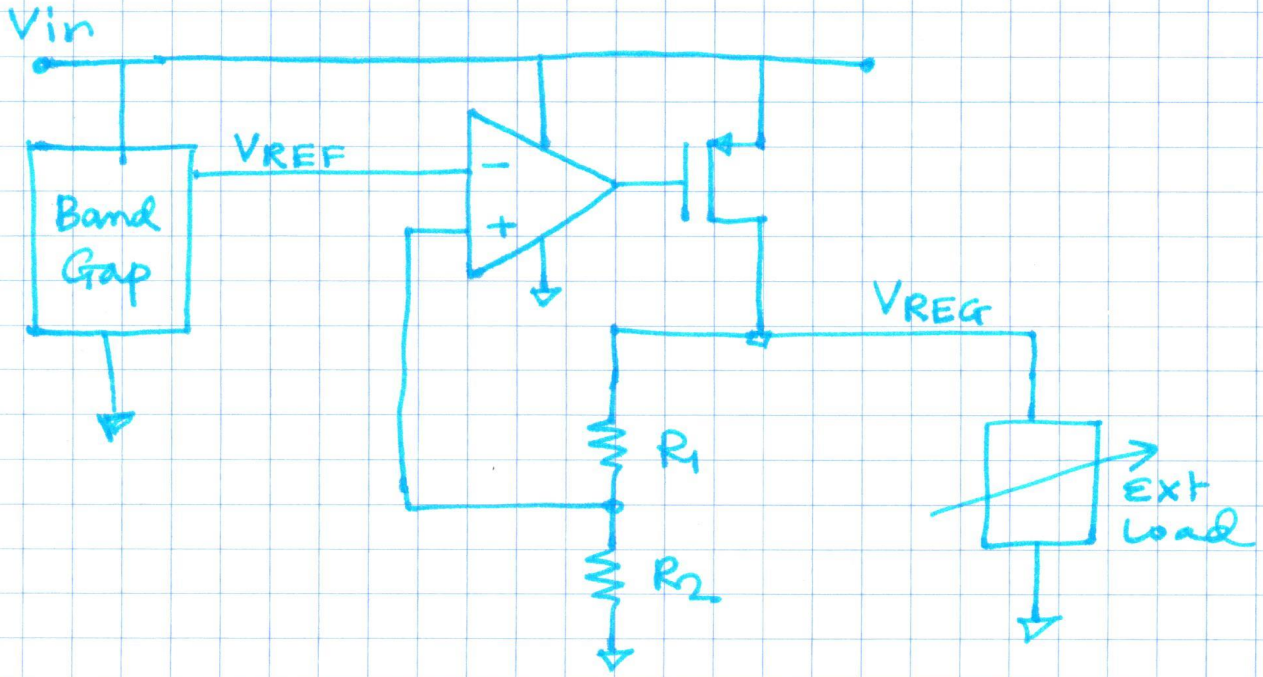
↘ A2D conversion & subtract digitally

Measure $V_T \ln(N)$ ⇒ Give T in °K

↑ Known Ratio

Voltage Regulator

→ is a constant voltage source independant of load current and input voltage.



→ V_{REF} — from Bandgap Reference. ~ 1.2V

→ Error Amplifier — OTA

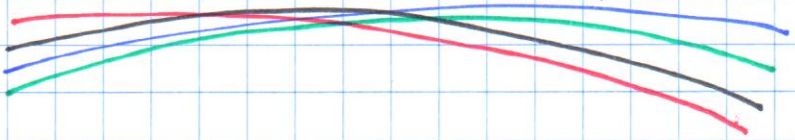
→ Feedback Network

→ Pass Transistor — V_{SG} increases as I_L increa

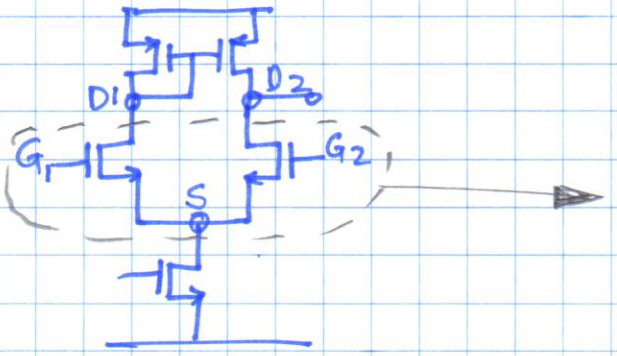
PMOS — large. — should be able to carry desired max load current.

$$V_{REG} = \left(1 + \frac{R_1}{R_2}\right) V_{REF}$$

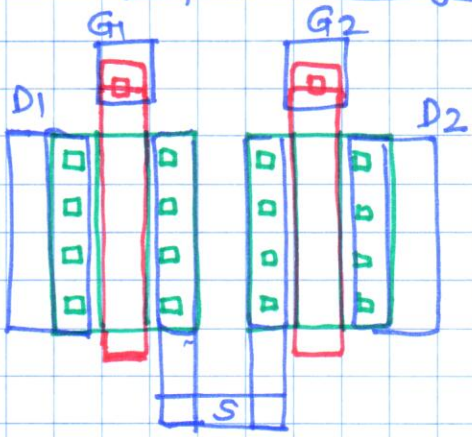
ANALOG LAYOUT TECHNIQUES



Schematic design



Layout design



In schematic design, only internal device parasitics are modeled for purpose of simulation.

Layout → Placement of all mask layers to create devices & interconnect. – New parasitics R, LC are added. when layout is created. – Can degrade performance of your circuits.

Circuit Design Engineer → EE background

Layout Design Engineer → Artists., good Engineering drawing skills
3.D visualization

Overall responsibility → you. as design Engineer

Layout Design.

DRC Design Rule Checks

— Guarantee Functional transistor & interconnects. in presence of process variations.

* Min Width.
* Min. Enclosure
* Min Spacing
* Min Extention.

Caliber tools

LVS Layout Vs. Schematic Check.

→ Layout → Netlist ↘ identical check.
Schematic → Netlist ↗ Device sizes same.

ERC Electrical Rule Check.

→ Electrical Connection of all wells, substrate
→ Devices connected to proper supply voltage
1V device → 1V supply.

Extraction PEX, RCX.

parasitic
→ R - only Resistance extracted - IR drop.
→ C → only p. Cap. extracted (to gnd)
→ CC → coupled cap. extracted (to adjacent lines)
→ R+CC → Final verdict for simulation.

→ L extraction → painful with std. tools
→ EMX used to model par. inductor
2-d simulator — Ind. Standard.

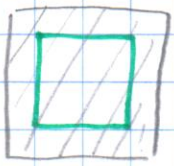
Crosssection of CMOS Technology.

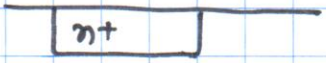
Reference: Chapter 18. Razavi CMOS Proc. Tech.
→ Review.

Slides discussed in class.

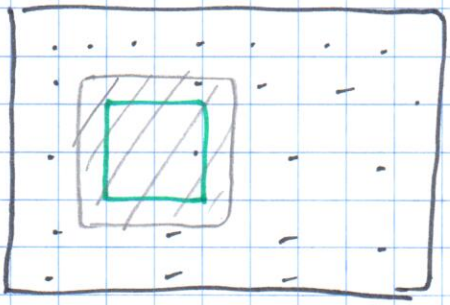
Nwell. poly Diffusion

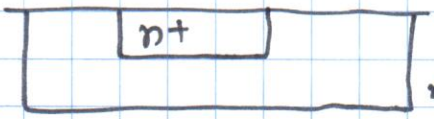
N type p-type



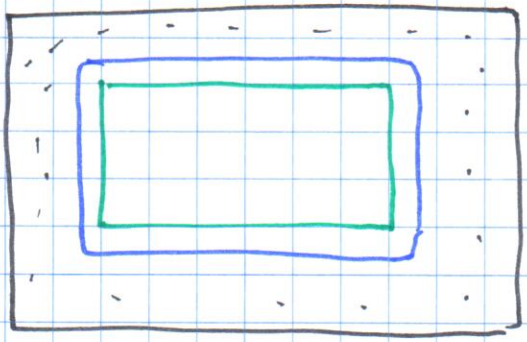


Diode

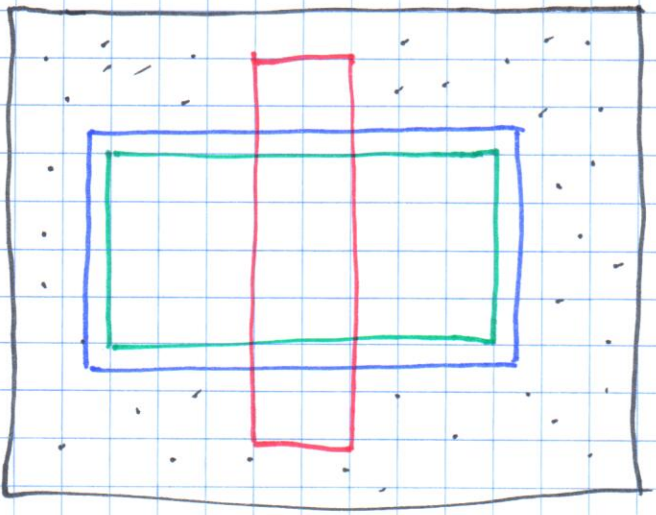


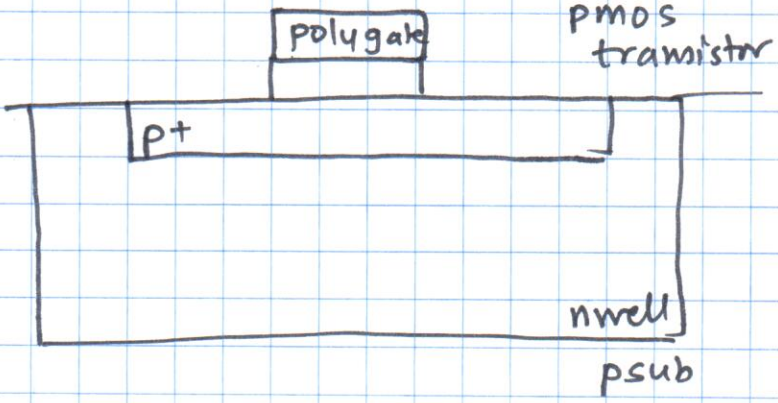


n-well contact



p+ - nwell diode





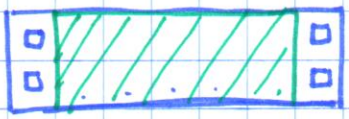
pmos transistor

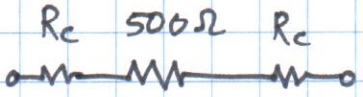
Device Parasitics

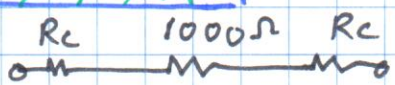
1. Resistor

$R_1 = 500\Omega$

$R_2 = 1000\Omega$





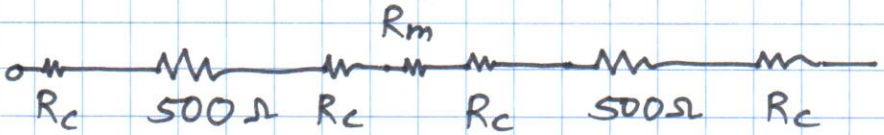


R_c - contact Resistance
- parasitic.

generally much higher than Metal R

Will NOT Match

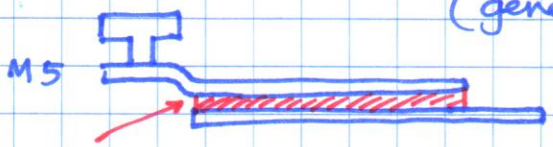
Better implementation



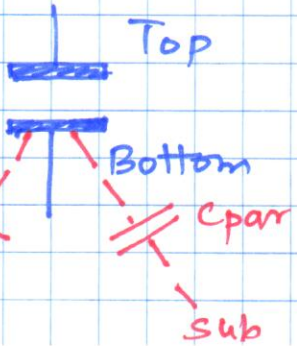
R_m - metal R
R_c - contact R
$R_m \ll R_c$

2. Capacitors

MIM - Metal Insulator Metal Cap
- Requires special mask layer to create thin oxide between two metals. (generally top two metals)

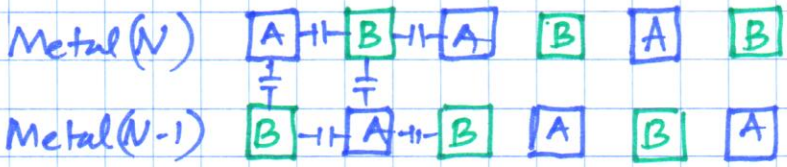


Thin ox - special mask layer



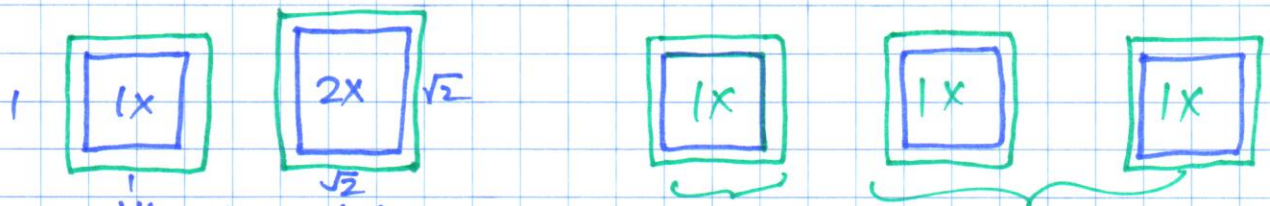
Bottom plate has large parasitics
← Try to use it as gnd connect.

MOM capacitor Metal Oxide Metal
— No special Mask needed



Good density in high Metal layer count process.

Cap Matching



Will not match

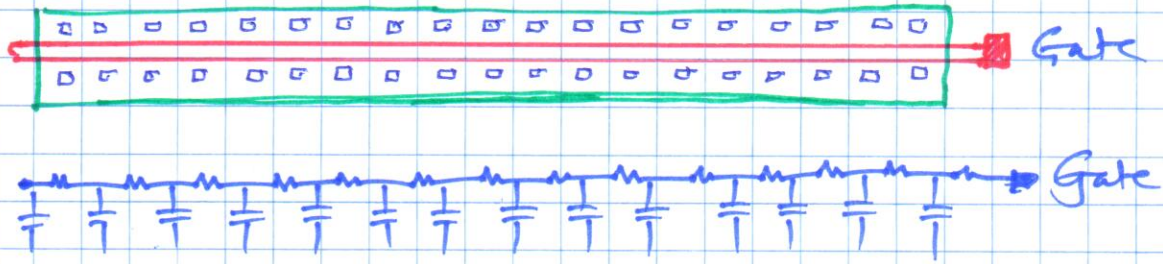
Better matching

→ Make sure you watch out for fringe cap.

→ Keep identical environment around matched caps.

3. MOS Devices.

Consider Device size W = 10 μm L = 0.05 μm.



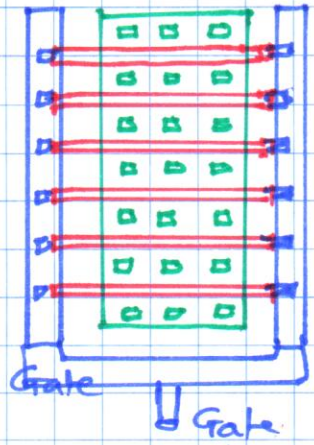
Long poly — large parasitic R + distributed cap.

→ Bad idea. → ↑ Noise

→ RC delay

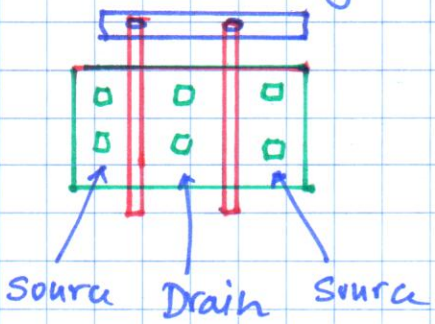
→ Cap Quality factor

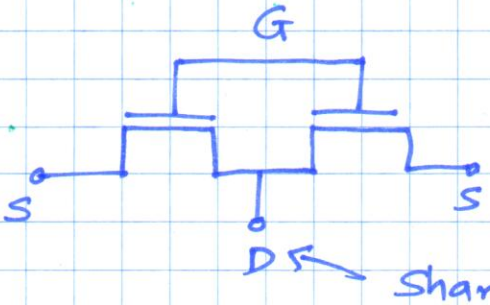
→ Increase number of fingers.
→ Connect gate with metal — poly resistance >> metal R.



→ Minimize gate resistance - RF performa

Reducing Drain Parasitics — Shared drain





Shared drain
→ Reduced parasitics

Well or Substrate connection for NMOS / PMOS

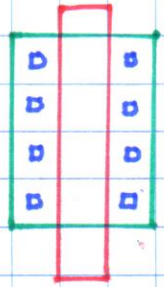
↳ Latchup consideration → Should have connection every 10 x 10 μm space (for example)

→ Connect to indiv. transistor or @ block level } judgement based on applicatio

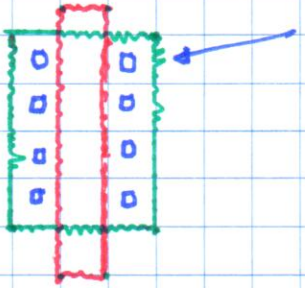
Matching

- Global variations
  - die 2 die
  - far away on same chip.
- Local Variations
  - mismatches
  - ↳ devices next to each other

Random Mismatch



Layout view



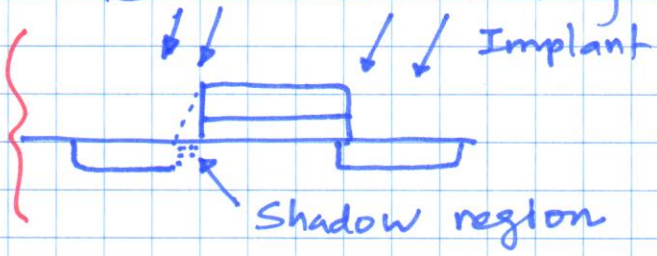
Actual After fabrication

Edge Effects due to
- → Etching uncertainities
- → Lithography

Matching Improves with increase in area (WL)
↳ Edge effects get averaged.

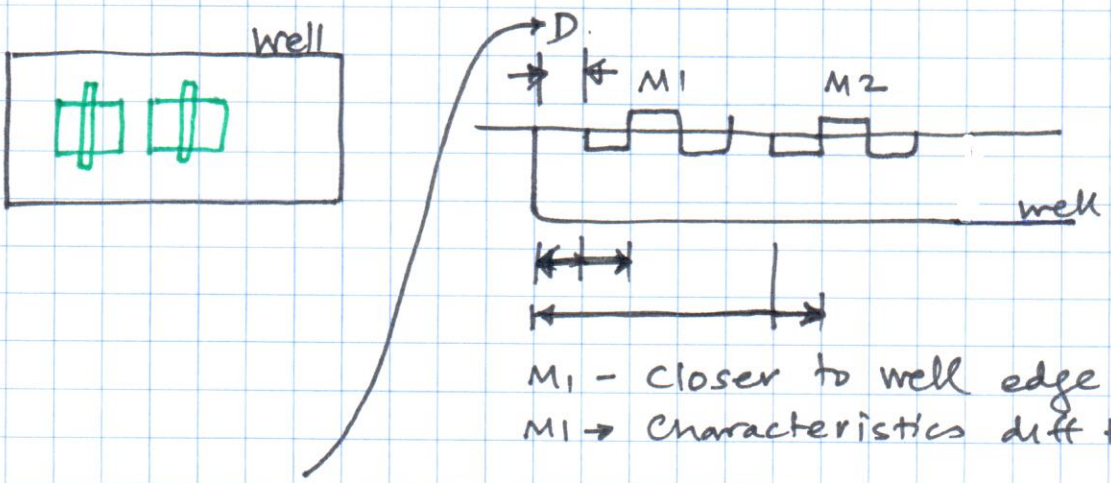
Process Variations → Due to inaccuracies in fab.

- → Mask Alignment
- → Shadowing effect



- → Proximity Effect
  - → Well prox. WPE
  - → STI - Shallow Trench Isol^{n}
- → Gradient Effect
- → Lateral Diffusion.

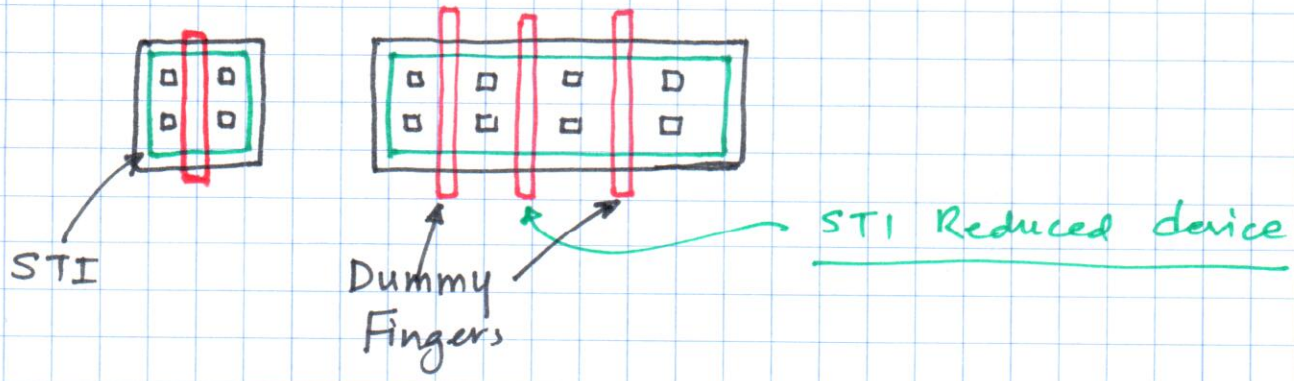
* WPE Well proximity effect



M_1 - closer to well edge than M2
M1 → Characteristics diff than M2

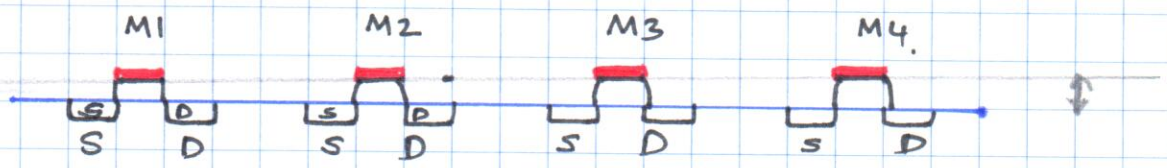
Increase D so that WPE is minimal.

* STI Shallow Trench Isolation effect



STI - to avoid formation of device between adjacent transistors. - Oxide trench. - Stress effect.

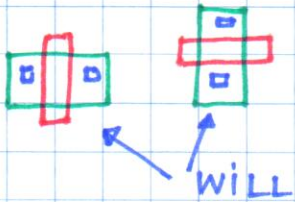
* Gradient Effect



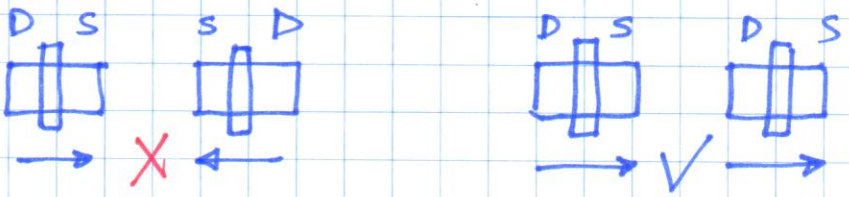
M4 & M1 will not match.
→ Common Centroid layout so that two dimentional gradient is cancelled out.

Critical Matching

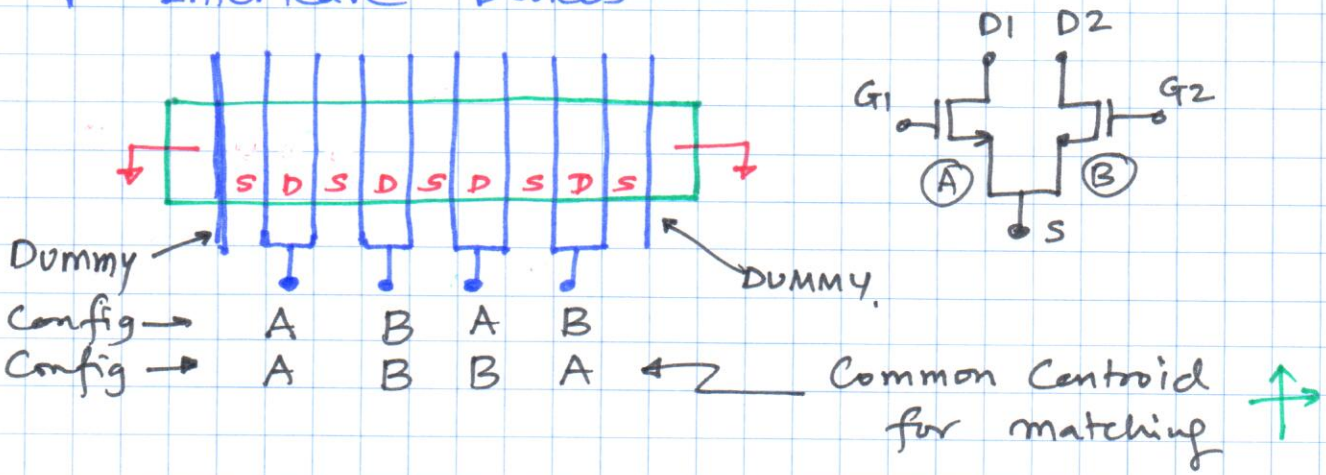
* Unit Cell layout
* Device orientation



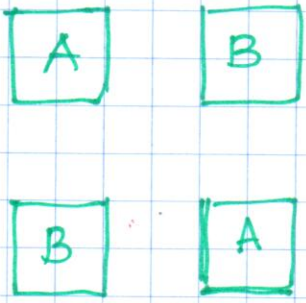
* Direction of current flow



* Interleave Devices



* Common Centroid layout



Gradient in any direction cancelled.

Keep dummy devices around matched devices to reduce edge effects.

* INTERCONNECT

→ parasitics R, L, C ↔ MINIMIZE / SYMMETRICALIZE"

High current lines – reduce R → IR drop ↓

High Frequency signals → Reduce C → Loading ↓

General Guideline

Use M1-M3 (lower Metals) for DC bias signals (Thin metals)

Use M_4-M_5-M_6 (High Freq) Signal Lines

↳ Reduce parasitic cap to substrate

Use Top thick metals (very low R) 2x, 4x thickness

↳ for VDD, GND lines.

Make these fat.

DO NOT SKIMP ON Metal.

(avoid overlap with signal lines)

In 28nm & below → Electromigration concern.

→ Burnin Issue.

Metals can carry limited current (Metal Width Shrinking)

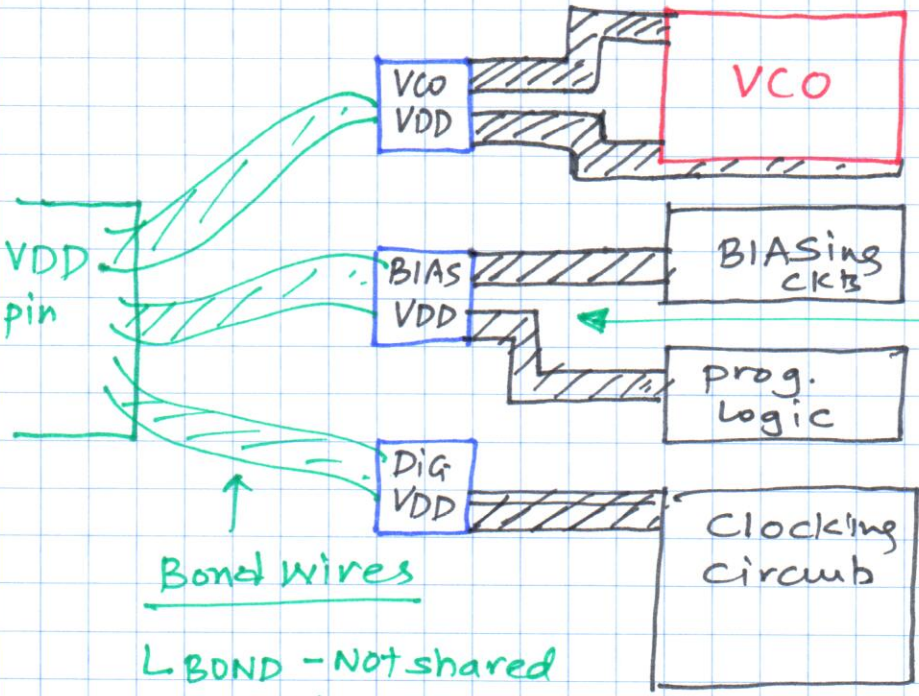
Strong Temperature Dependent

	115°C	125°	
1μm M1	X mA	0.7X mA	30% less.

→ CAD tools can be utilized to identify violation.

Voltus Fi

✱ Supply / Ground connections



✱ connection used.

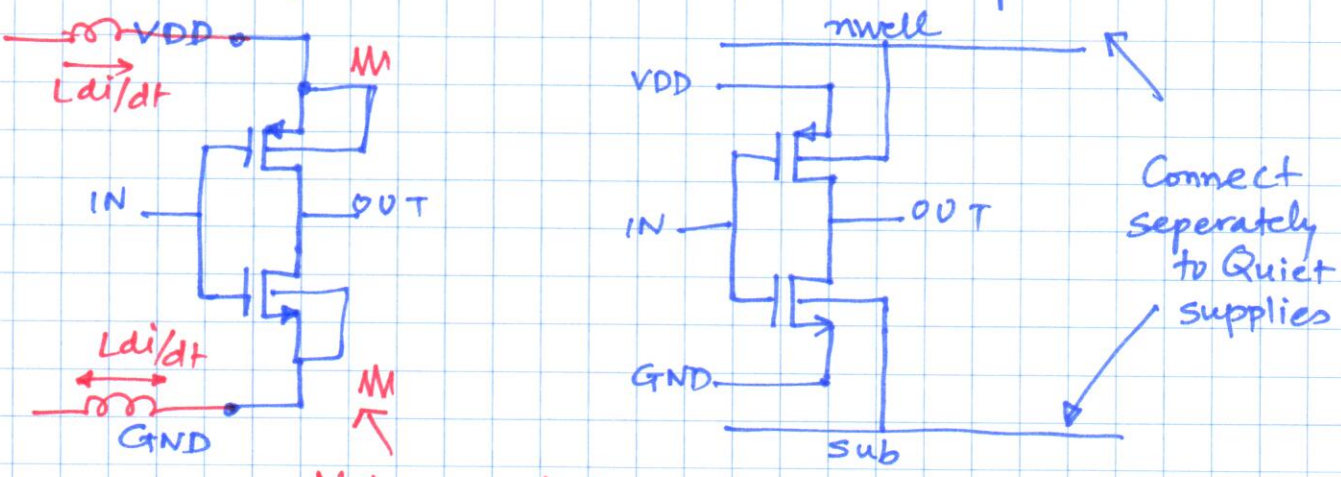
IR drop NOT shared

L_{BOND} - Not shared

$L\frac{di}{dt}$ → Noise coupling avoided.

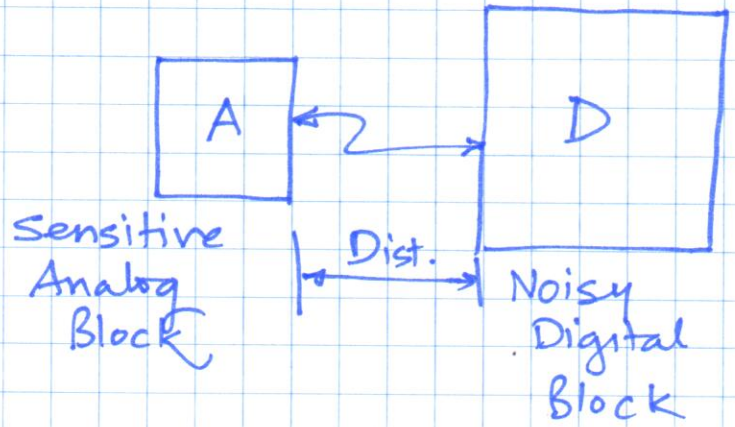
✱ Substrate & Well connection

→ Important to avoid latchup.



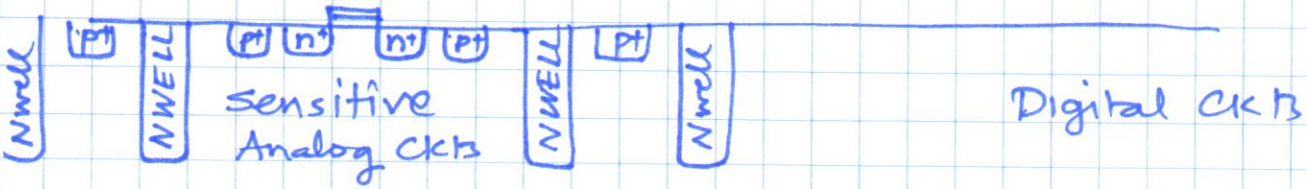
Locally generated noise (switching) is not transmitted to other (sensitive) circuits

✡ ISOLATION & COUPLING

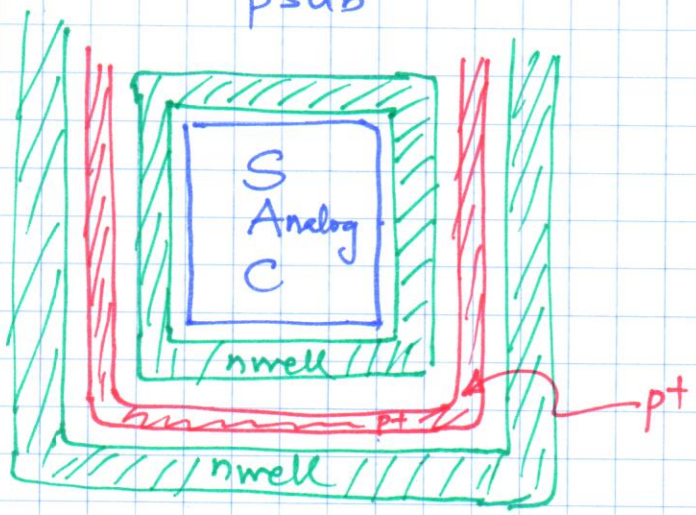


① → Maximize Distance D — Die area issues.

② → Guard Rings.



psub

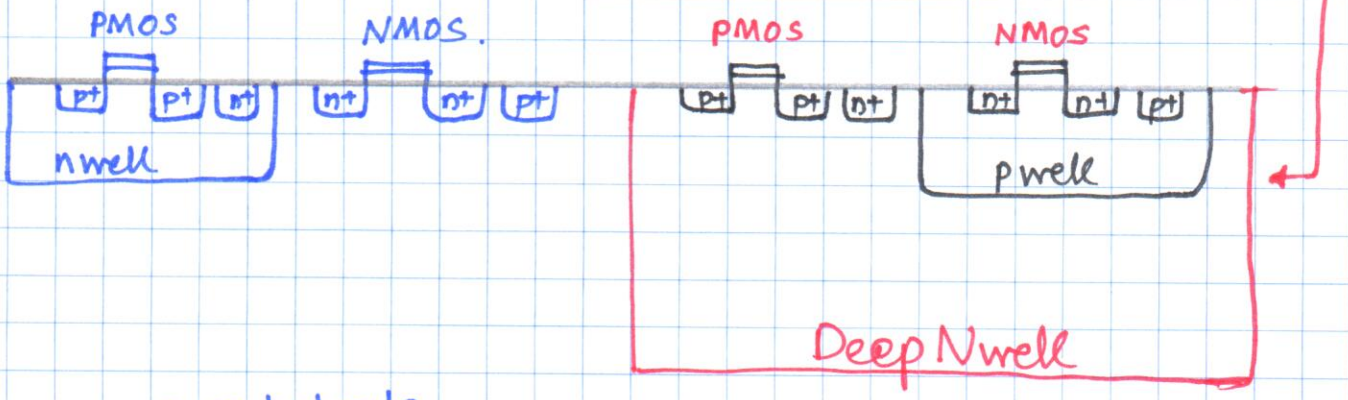


Like Moat around castle.

③ → Create isolated (Electrically) substrate

Deep-Nwell → Extra Mask Layer

Great for RF-Mixed Signal SOCs.



p-substrate

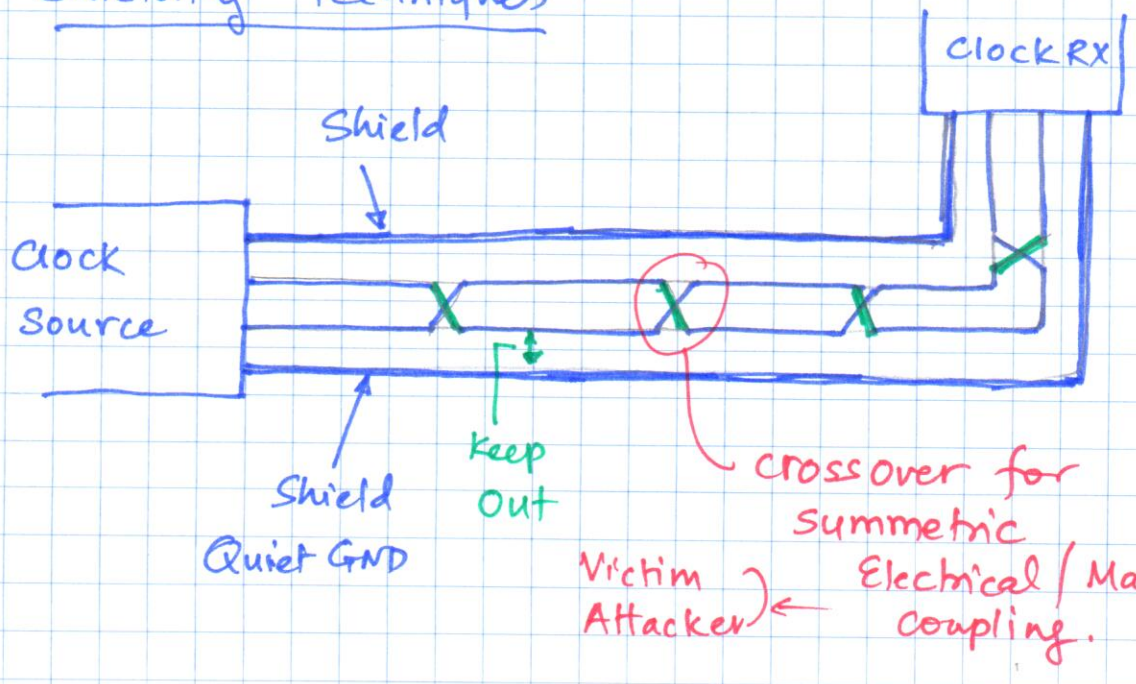
NMOS - in bare substrate

Body connection - sub → common ground

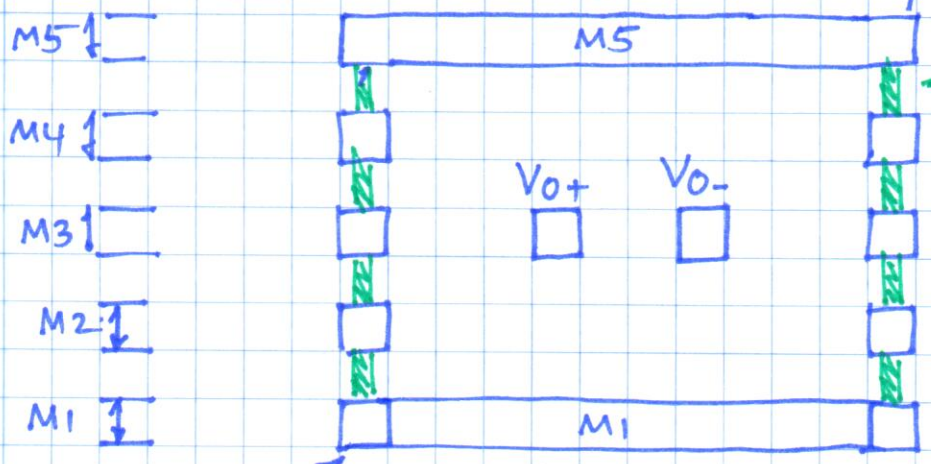
→ NMOS in isolated pwell.

→ Each Nmos can have separate well connection → isolated from substrate noise.

④ Shielding Techniques



Extra Shielding → Really Really Sensitive lines



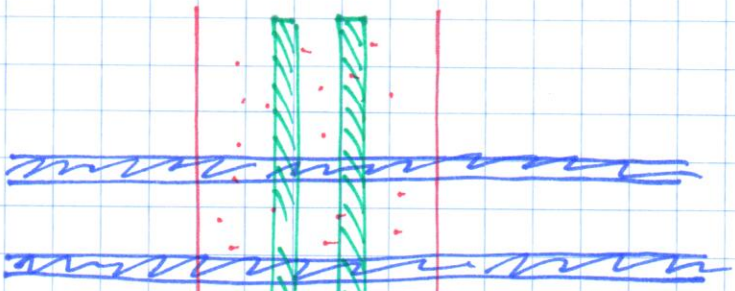
Coax Cable Type structure

2 CROSS-SECTION

Use M4 or M2 for crossovers

Connect Shield to good analog ground.

↳ Quiet with Low ohmic ~~resistance~~ impedance @ frequency of operation.

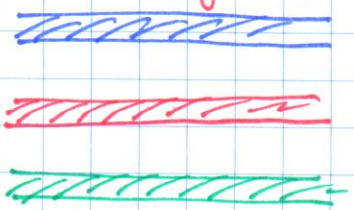


sensitive RF Lines.

Shield Metal (sandwitched)

Connect to good/Quiet AGND.

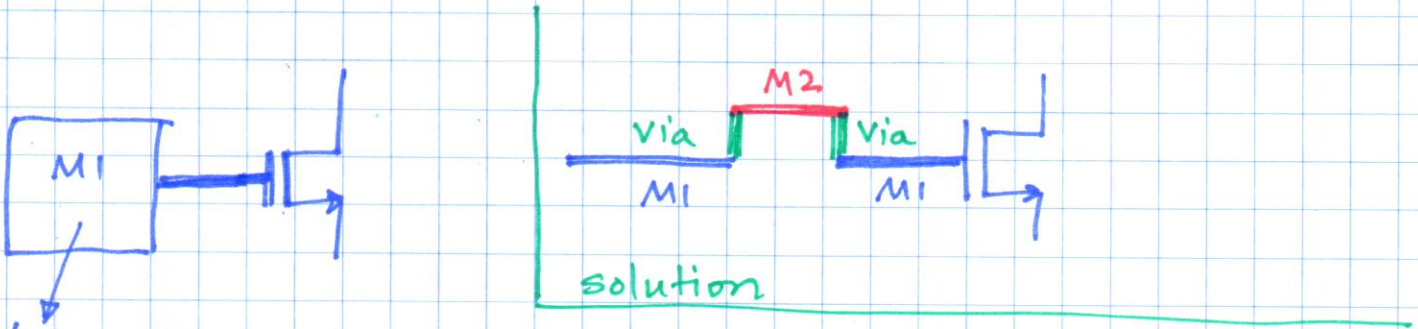
Noisy Digital Clock lines



Metal Stack crossection

Other Important Issues

✡ Antenna Effect



large piece of metal 1 Routing etc. → Collects ions/charge during etching + damages gate oxide.

→ Checked during DRC

✡ Metal Fills

In advance CMOS processes, with high number of metal layers, metal density needs to be carefully controlled within certain range.

→ depends on Fab requirement

→ Driven by Chemical Mechanical Polishing
→ plannerization of all metal layers

→ Design for manufacturability

→ After all Chip layout done
↓ auto tool adds/sprays sparkles of metal pieces to meet foundry requirement

→ Pieces of metal over sensitive circuits

can mess up symmetry, added coupling etc.

→ Do metal Fills @ block level

→ RF/analog senitive blocks – do manual fill & then extracted sims with fills

→ Can be a show-stopper if done@ last min.

✡ Planning For Metal Mask Changes

→ Assume you will have bugs

→ Add programmability / flexibility (digital)

→ Observability (test o/ps)

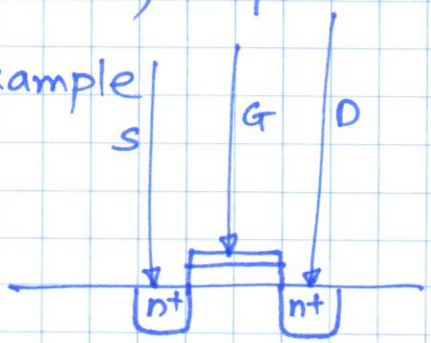
→ Add CyA-CyB circuit

→ Make sure you can use top metals to fix connection

Top metal mask 10K $

M1, Poly 50-60K $.

→ Example



Bring all S, G, D on all metals.

← spare kit

→ Keep them as fillers in empty spaces.

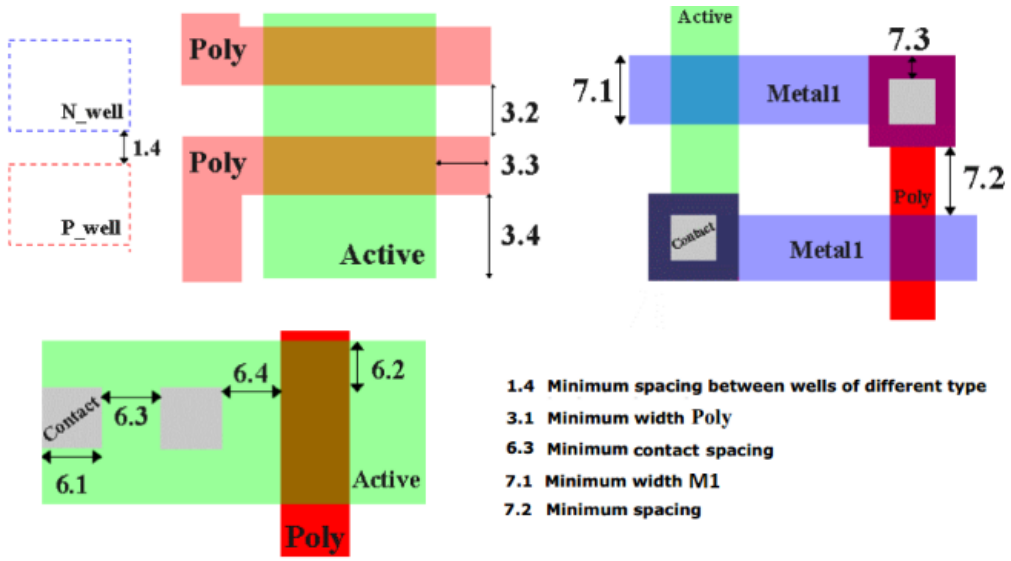
✡ Chip Planning

- City planning — architecture
- Board level layout / parasitics
- Supply / ground / Signal Routing @ board level
- Define package pin-outs / bonding diagram.
- Floorplan your chip — Analyze RF coupling issues
- Signal / Clocks / Vdd / Gnd flow
- Isolation between sensitive circuits
- Digital Circuits can also fail due to IR drops. Check VDD / GND IR drops
- Top level (chip level) connectivity Check
  - → Simulate → power up / down
    → Reliability Checks.
    → Electro-migration checks.
  - → make sure circuits somewhere else is not interacting with your ckts.
  - → Sensitive Routing R/L/C extraction to gain confidence

→ Just Maskset for 28nm CMOS can cost ~ 1 million $.
+ 4-6 K$ per wafer processed.

(i) Use all neurons / compute power before tape-out.

Sample of Design Rules provided by the foundry
(Below shown rules doesn't correspond to SCL process)

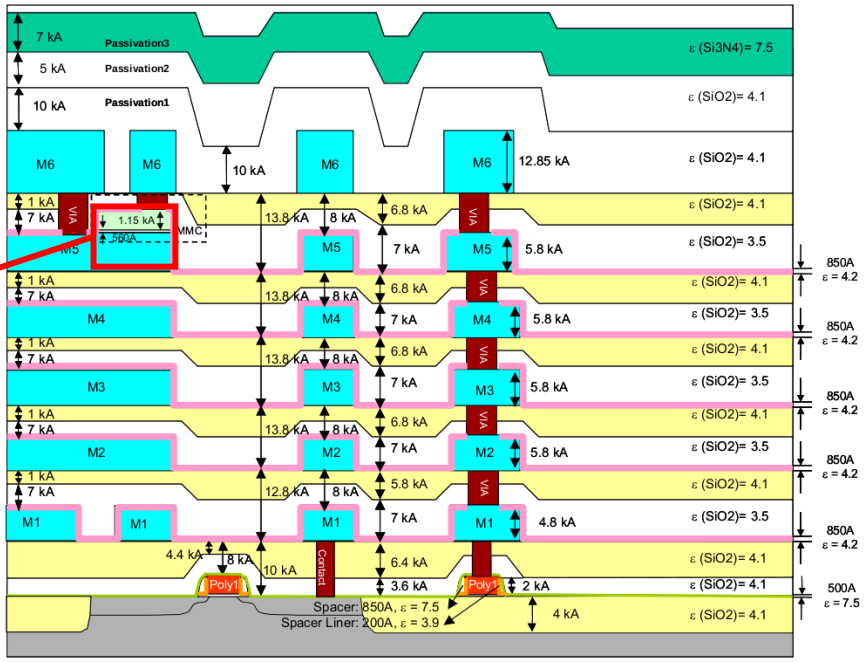


1.4 Minimum spacing between wells of different type
3.1 Minimum width Poly
6.3 Minimum contact spacing
7.1 Minimum width M1
7.2 Minimum spacing

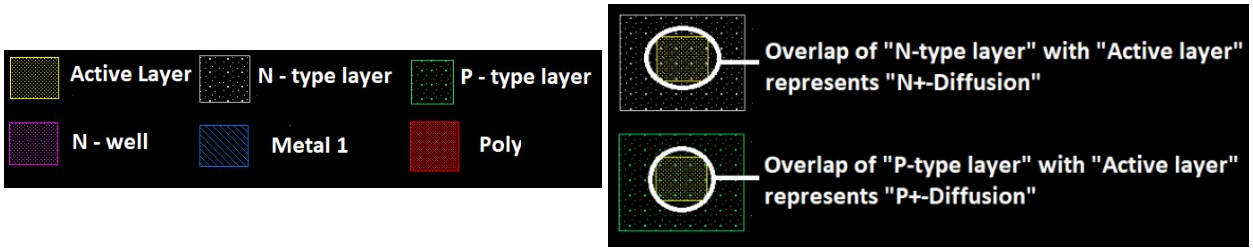
Interconnect layers (Doesn't correspond to SCL process)

MIM Capacitor
Top plate connected to M6
M5 acts as bottom plate

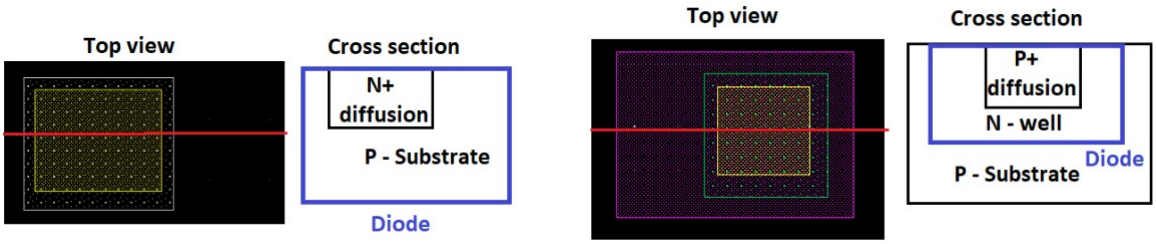
Dielectric thickness = 56nm



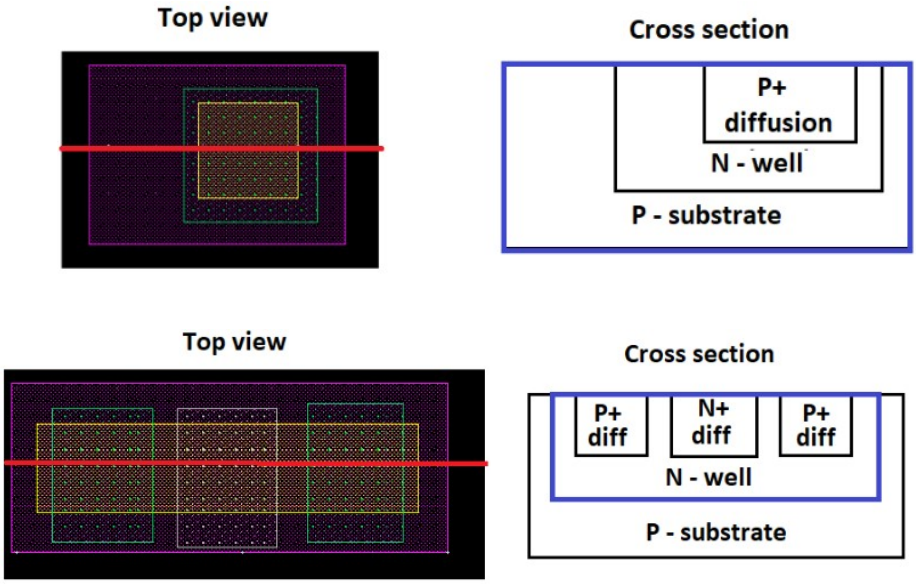
Basic Layers in SCL 180nm


Active Layer
N - type layer
P - type layer
N - well
Metal 1
Poly
Overlap of "N-type layer" with "Active layer" represents "N+-Diffusion"
Overlap of "P-type layer" with "Active layer" represents "P+-Diffusion"

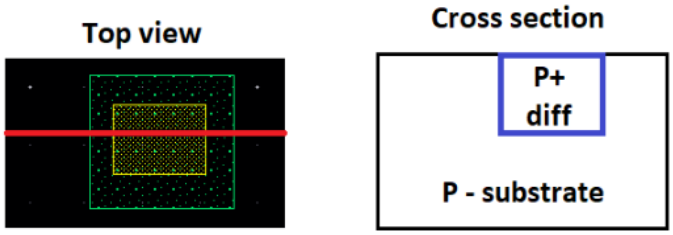
Different ways of forming Diode

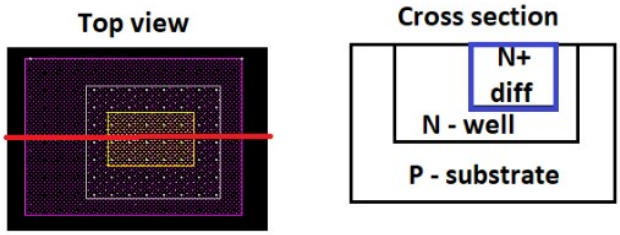


Different ways of forming BJT

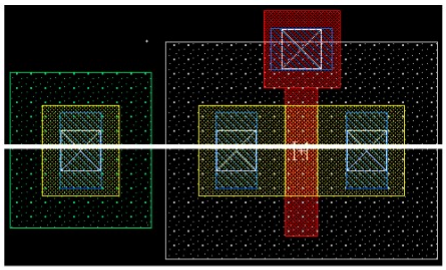


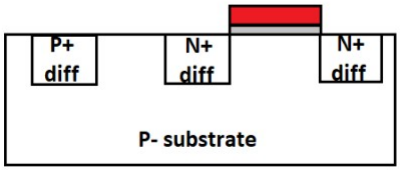
Contacts to regions





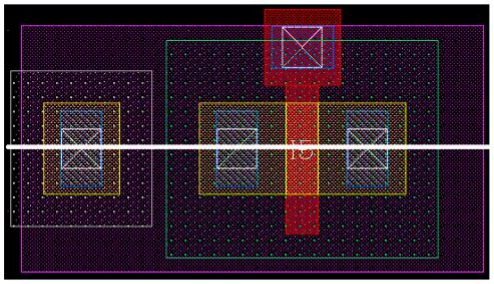
Top View of NMOS

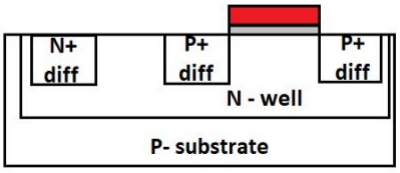




Cross sectional view of NMOS

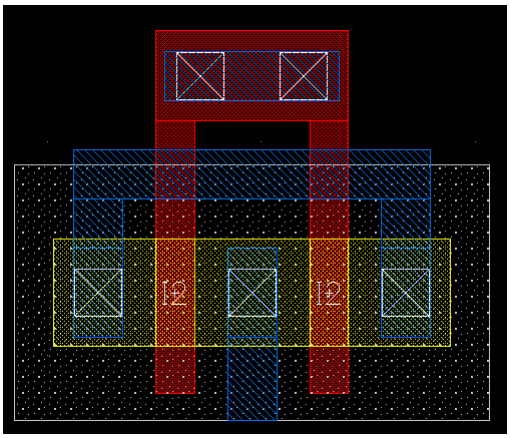
Top View of PMOS



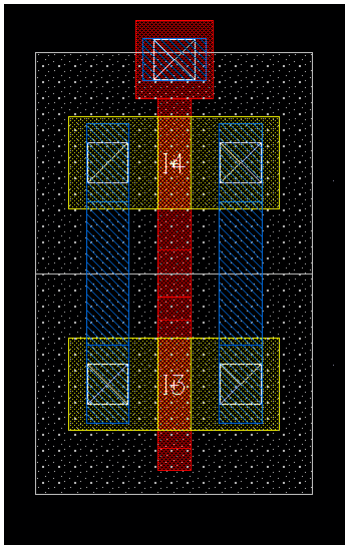


Cross sectional view of PMOS

NMOS
Total width = (0.5um) x 2 fingers = 1um
Length= 0.18 um

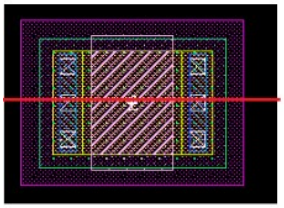


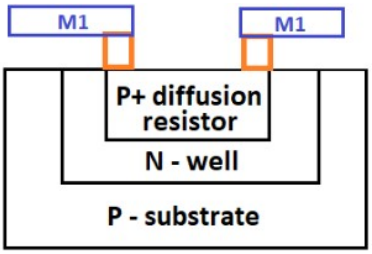
NMOS
Total width = (0.5um) x 2 multiples = 1um
Length= 0.18 um



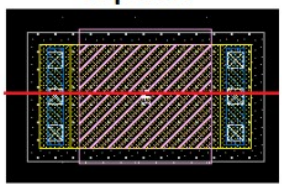
Diffusion resistors

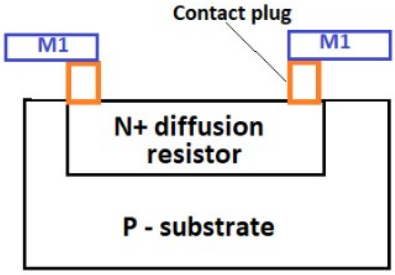
Top view



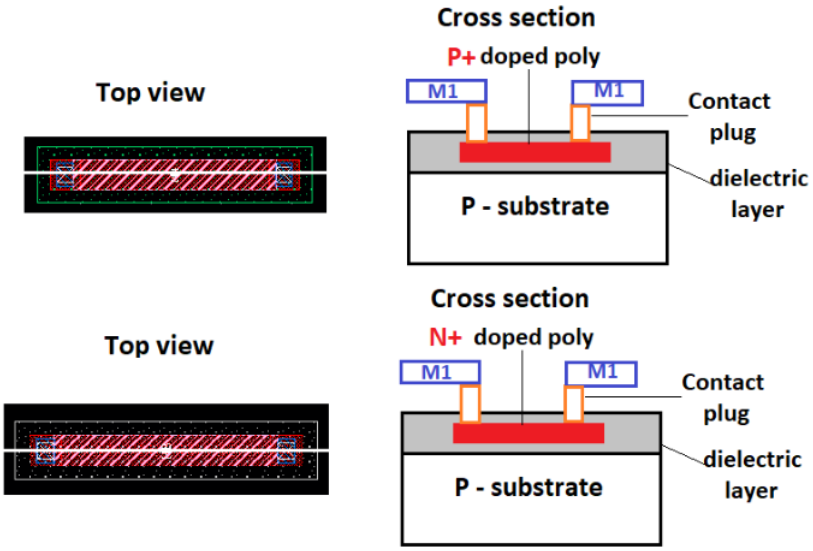


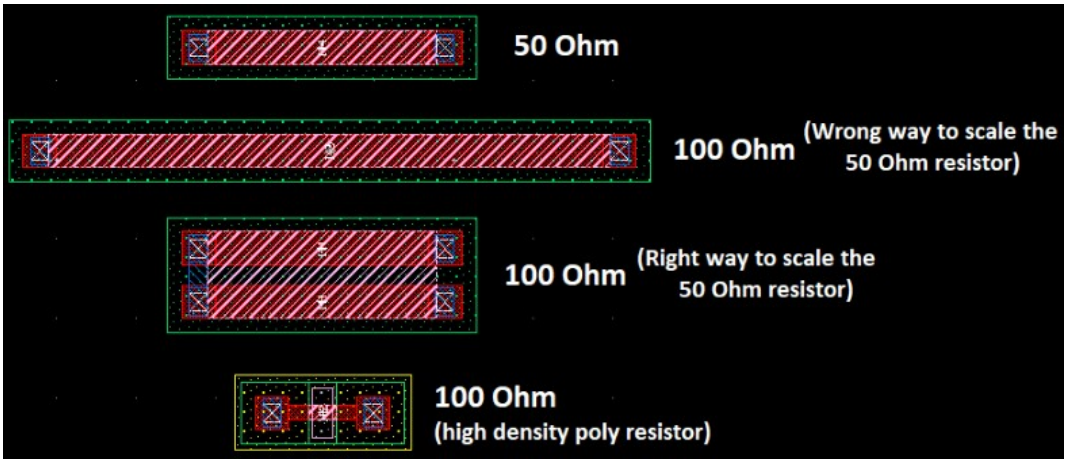
Top view



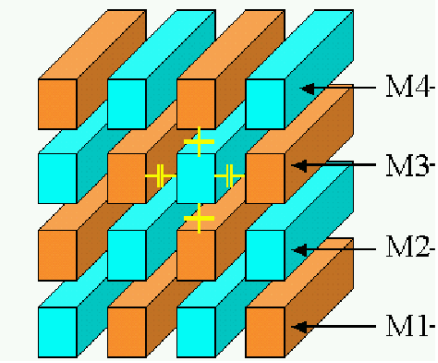


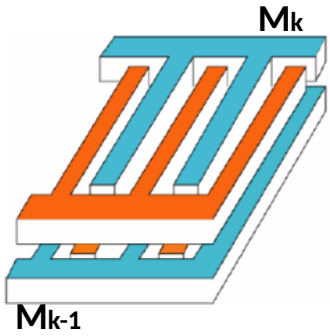
Poly resistors



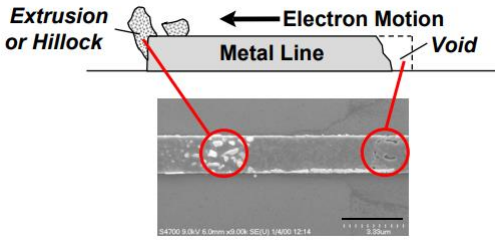

50 Ohm
100 Ohm
(Wrong way to scale the 50 Ohm resistor)
100 Ohm
(Right way to scale the 50 Ohm resistor)
100 Ohm
(high density poly resistor)

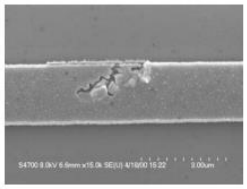
MOM Capacitors

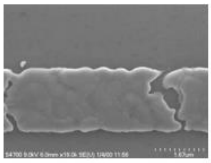


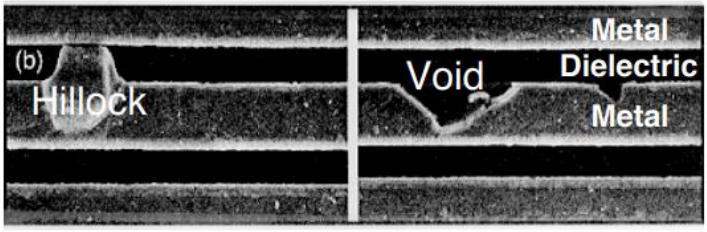


Electromigration failure



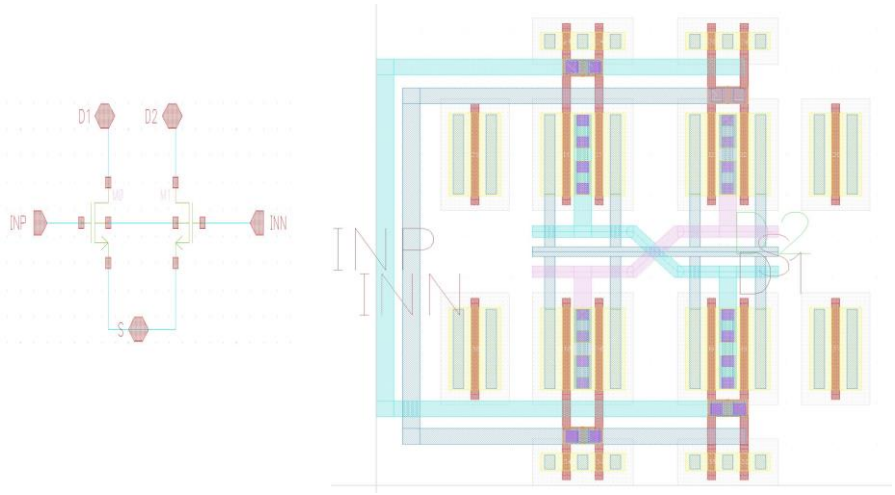




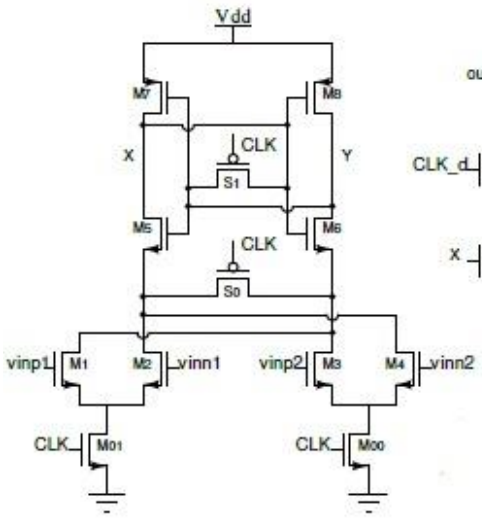


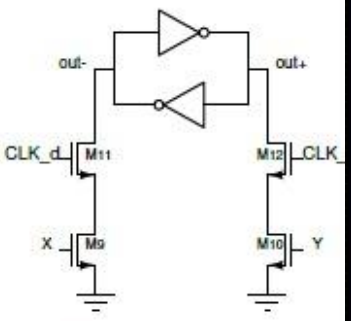
https://web.stanford.edu/class/ee311/NOTES/Interconnect_Al.pdf

Layout of the Input Pair of OpAmp using Common-Centroid

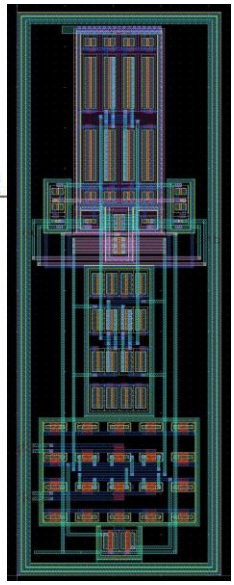


Comparator Schematic



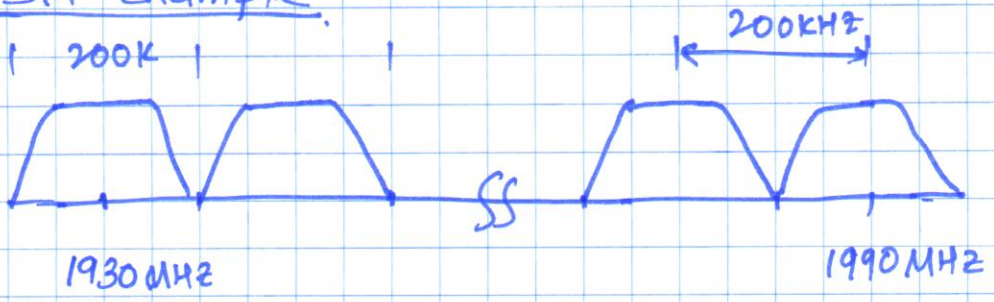


Layout



CONTINUOUS TIME FILTERS

GSM Example



AM, FM Radios – Common Medium Shared between multiple users.

Filters are used to provide frequency selectivity.

→ Keep desired spectrum (channel)
→ Attenuate undesired channels.

→ Wireline Communication Example

Filters used to compensate for Channel loss (frequency dependant)

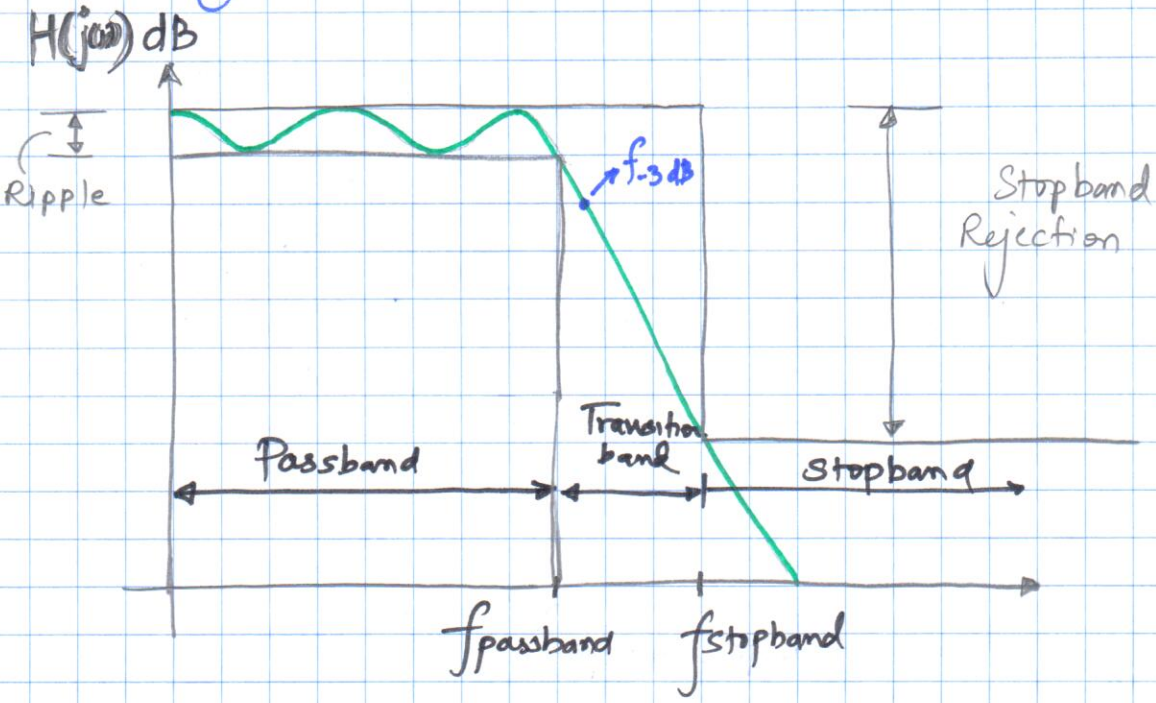
→ Equalization & pulse shaping.

→ Antialiasing filters for ADC

→ Smoothing filters for DAC.

Filter Specifications

Study Low Pass filters first – Then Xform to diff types.



Filter with transfer function H(s)

$$H(j\omega) = |H(j\omega)|\, e^{j\theta(\omega)}$$

Phase Delay $= \tau_{PD} = -\dfrac{\theta(\omega)}{\omega}$ (time units)

Group Delay $= \tau_{GR} = -\dfrac{d\theta(\omega)}{d\omega}$ (time units)

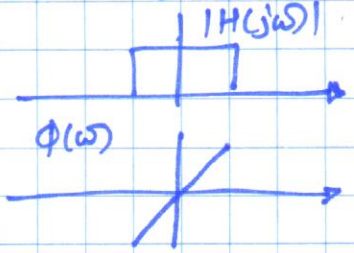
$\theta(\omega) = K\omega$ ← Constant — No phase distortion.

$\tau_{PD} = \tau_{GR} = -K$

Constant group delay.

→ This property is important for pulse-shaping in Wireline applications

Filter Approximations (Ideal Brickwall)



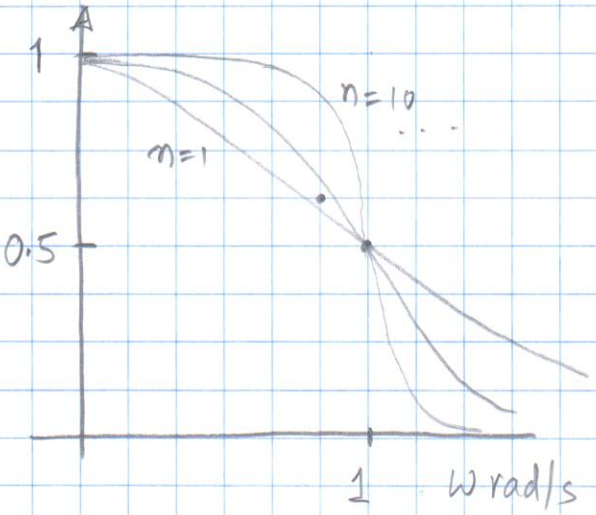
1. Butterworth Approximation

$$|H(j\omega)|^2 = \frac{1}{1+\omega^{2n}}$$

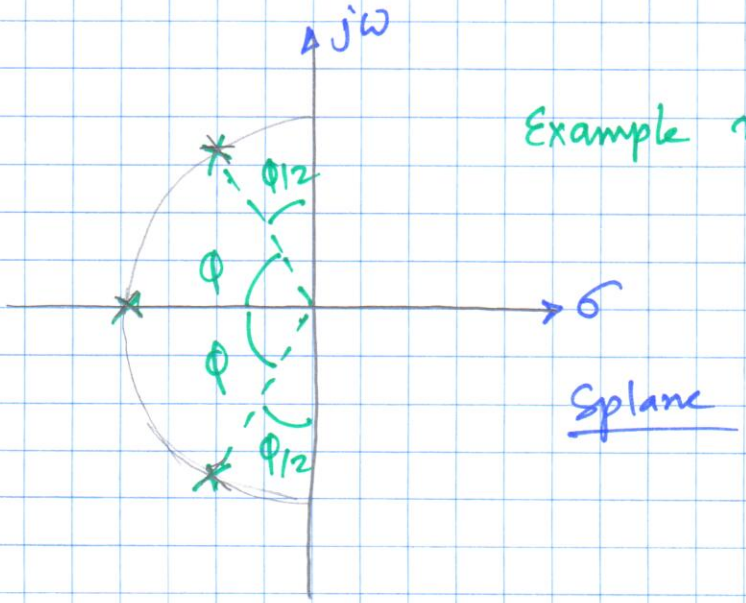
$|H(j0)|^2 = 1$; ~~$H(j0.5) =$~~

$|H(j1)|^2 = 0.5$

$|H(j\infty)|^2 = 0$

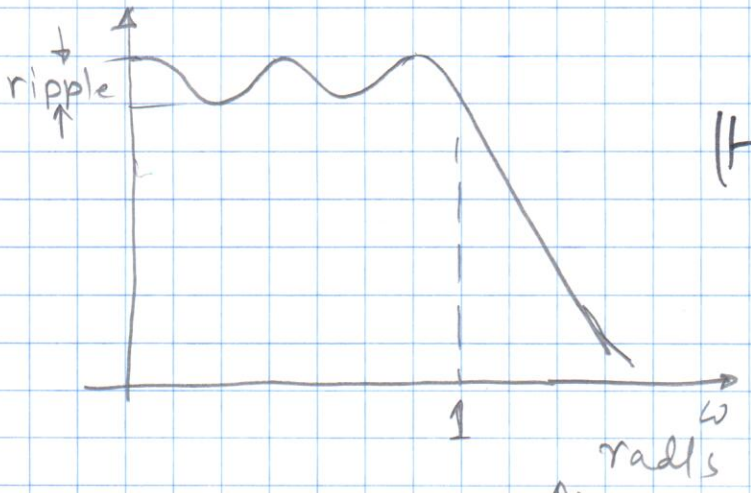


* Maximally flat passband @ $\omega = 0$.
* Moderate phase distortion. (Group delay)
* Poles located on unit circle



2. Chebyshev Approximation

→ keep attenuation in passband minimal
→ within Ripple spec.
→ Sharper transition band (compared to Butterw)
→ Poorer group delay distortion.
→ All poles located on Ellipse.

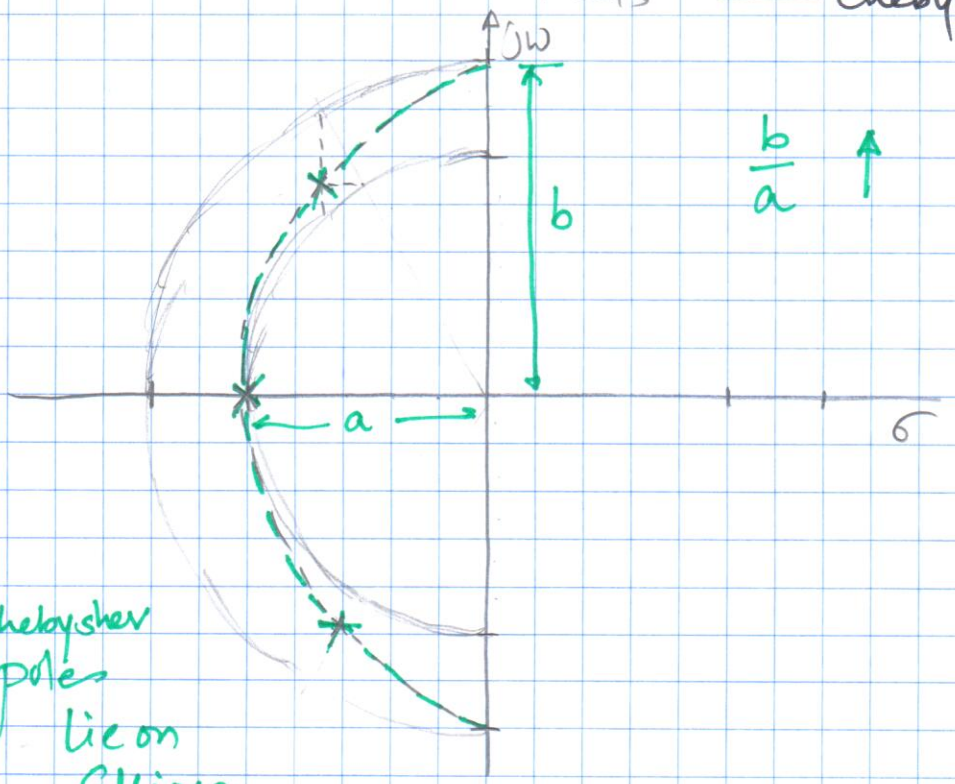


$$|H(j\omega)|^2 = \frac{1}{1+\epsilon^2 T_n^2(\omega)}$$

→ $T_n(\omega) = \cos(n\cos^{-1}\omega)$

ϵ - sets ripple amplitud

— Chebyshev polynomial (nth order)



$\frac{b}{a}$ ↑ ripple ↑

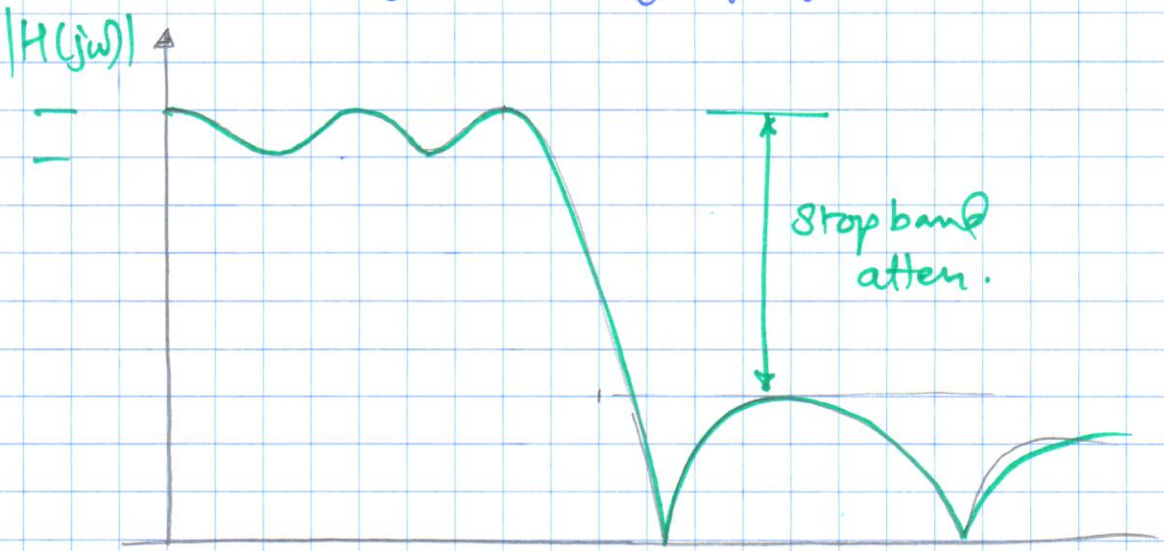
Chebyshev poles lie on Ellipse

3. Elliptic filters (Cauer filters)

→ Zeros in stopband, create nulls.

→ Very sharp transition band - highest atten with lowest order

→ poorest group delay performance.

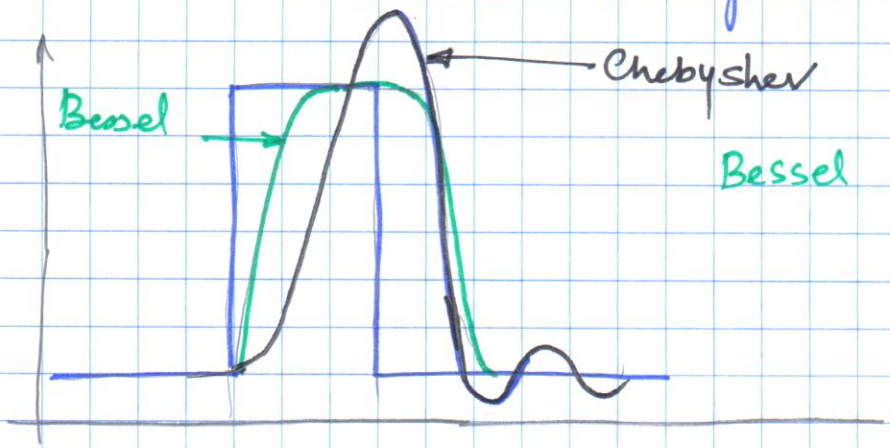


④ Bessel Approximation

→ Poles ~~on~~ outside unit circle (low Q)

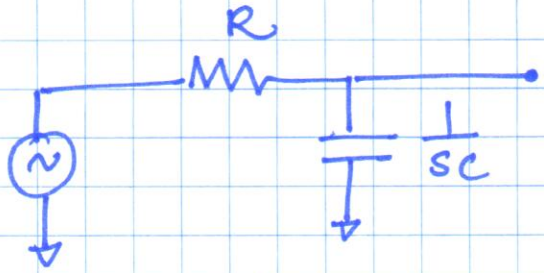
→ Maximally flat group delay

→ attenuation ∿ Not great.



Bessel - minimizes [S]

RC filter - 1st order Example

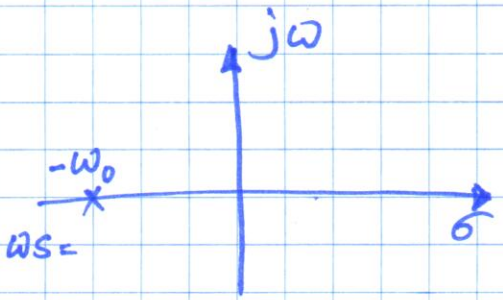


$$V_{out} = \frac{1/sC}{R + 1/sC} = \frac{1}{\left(1 + \frac{s}{1/RC}\right)}$$

$$\text{pole @ } -\omega_0 = -\frac{1}{RC}$$

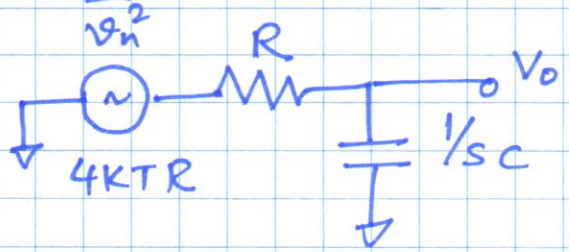
$$@\ s = j\omega_0 \quad |H(j\omega)| = \frac{1}{\sqrt{2}}$$

→ 3dB frequency



Note: parasitics across R will limit high freq. atten.

Noise Analysis



$$S_{out}(f) = 4KTR \cdot \frac{1}{4\pi^2 R^2 C^2 f^2 + 1}$$

Total integrated o/p noise

$$= \int_0^\infty \frac{4KTR}{4\pi^2 R^2 C^2 f^2 + 1}\, df$$

$$= \frac{kT}{C} \quad \text{indep of } R$$

Example 1pF cap → 64 μVrms @ 300°K

for complex filter (higher order)

$$\text{o/p noise} = x \frac{kT}{C}$$

x ↑ depends on order

Also - assumption - active circuits - lower noise.

$$\text{Filter Dynamic Range} = \frac{\text{Max Voltage Swing}}{\text{Min. discernible signal}}$$

Max Voltage Swing ← V_{DD}, Linearity

Min. discernible signal ↑ Noise

$$\text{Max Voltage Swing} = \frac{1}{\sqrt{2}} \frac{V_{DD}}{2} \quad \text{(Rms Voltage)}$$

$$\text{Min Voltage Swing} = \sqrt{x \frac{kT}{C}} \quad \text{(Rms Noise)}$$

$$DR = \frac{V_{DD}/2\sqrt{2}}{\sqrt{x \frac{kT}{C}}} = V_{DD} \sqrt{\frac{C}{8x kT}}$$

$$DR_{dB} = 20 \log_{10} \left(V_{DD} \sqrt{\frac{C}{8x kT}} \right)$$

$$= 20 \log_{10} \left(V_{DD} \sqrt{\frac{C}{x}} \right) + 75 \text{ dB}$$

(C in pF)

For $V_{DD} = 1V$ $C = 1pF$ $x = 1$

$$DR_{dB} = 75 \text{ dB} = (1.76 + 6.02N)$$

↑ # of bits

$N = 12$ bits Best possible

Reference - Haideh Khorramabadi classnotes.

FILTER DESIGN EXAMPLE

Design a Chebyshev filter to meet following req.

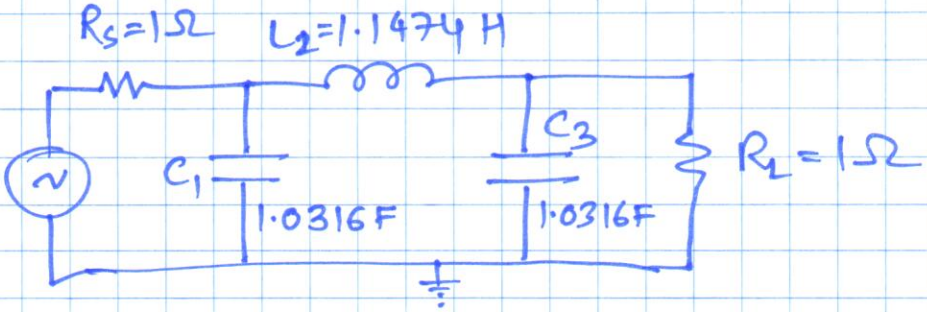
* 0.1dB ripple * 10MHz ripple BW.
* Stopband atten 40dB * Stopband 60MHz

→ Ripple BW/Stopband = 1/6

→ from 0.1dB ripple Chebyshev Atten chara. (Fig 8.15) for n=3 atten @ 6 rad/s = 42dB.

→ 3rd order filter

From Table 8-2

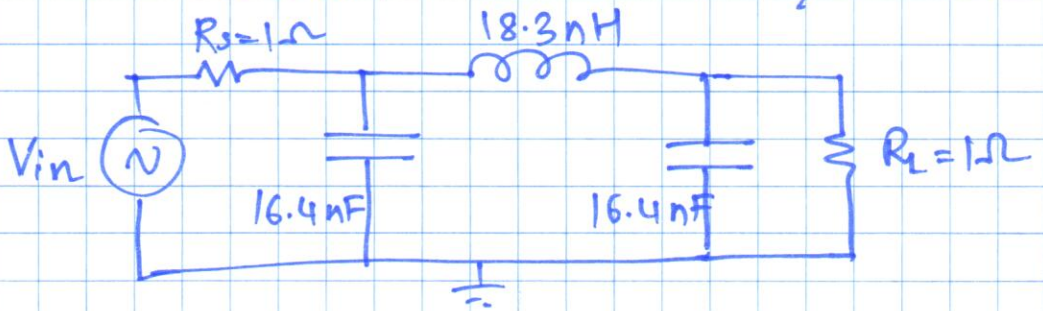


$\omega_{ripple\ BW}$ = 1 rad/s Desired $\omega_{ripple\ B}$ = 2π × 10 MHz = 62.8 M rad/s

$$C_1 = C_3 = \frac{1.0316\,F}{62.8\,M} = 16.4\,nF$$

$$L_2 = \frac{1.1474\,H}{62.8\,M} = 18.3\,nH$$

Impractical for IC implementation



ANALOG AND DIGITAL FILTERS: DESIGN AND REALIZATION

HARRY Y-F. LAM

Bell Telephone Laboratories, Inc.

Formerly with University of California, Berkeley

100680 Lam, Harry Y-F

Analog and digital filters : design

100680

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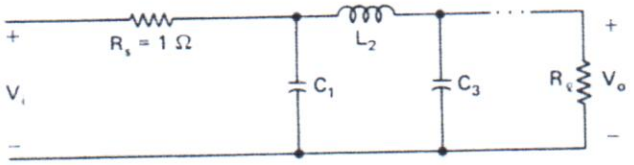
BUTTERWORTH FILTER



(c) $R_L = R_s$

Fig. 8-9 Circuit structures of low-pass Butterworth filters.

FILTER ORDER

TABLE 8-1 Element Values for the Circuit in Fig. 8-9(c)

n	C_1	L_2	C_3	L_4	C_5	L_6	C_7	L_8	C_9
1	2.0000								
2	1.4142	1.4142							
3	1.0000	2.0000	1.0000						
4	0.7654	1.8478	1.8478	0.7654					
5	0.6180	1.6180	2.0000	1.6180	0.6180				
6	0.5176	1.4142	1.9319	1.9319	1.4142	0.5176			
7	0.4450	1.2470	1.8019	2.0000	1.8019	1.2470	0.4450		
8	0.3902	1.1111	1.6629	1.9616	1.9616	1.6629	1.1111	0.3902	
9	0.3473	1.0000	1.5321	1.8794	2.0000	1.8794	1.5321	1.0000	0.3473

Chebyshev Filter

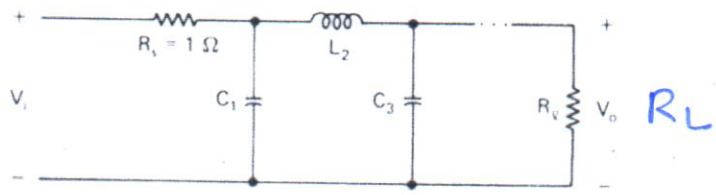


Fig. 8-17 Circuit structure of low-pass Chebyshev filters.

Ripple 0.1dB

TABLE 8-2 Values of Circuit Elements in Chebyshev Filters when $A_{max} = 0.1$ dB (R_L)

n	R_ℓ	C_1	L_2	C_3	L_4	C_5	L_6	C_7	L_8	C_9
1	1.0	0.3052								
2	0.5	1.5715	0.2880							
3	1.0	1.0316	1.1474	1.0316						
4	0.5	2.3545	0.7973	2.6600	0.3626					
5	1.0	1.1468	1.3712	1.9750	1.3712	1.1468				
6	0.5	2.5561	0.8962	3.3962	0.8761	2.8071	0.3785			
7	1.0	1.1812	1.4228	2.0967	1.5734	2.0967	1.4228	1.1812		
8	0.5	2.6324	0.9285	3.5762	0.9619	3.5095	0.8950	2.8547	0.3843	
9	1.0	1.1957	1.4426	2.1346	1.6167	2.2054	1.6167	2.1346	1.4426	1.1957

Ripple 1dB

TABLE 8-3 Values of Circuit Elements in Chebyshev Filters when $A_{max} = 1$ dB (R_L)

n	R_ℓ	C_1	L_2	C_3	L_4	C_5	L_6	C_7	L_8	C_9
1	1.00	1.0177								
2	0.25	3.7779	0.3001							
3	1.00	2.0236	0.9941	2.0236						
4	0.25	4.5699	0.5428	5.3680	0.3406					
5	1.00	2.1349	1.0911	3.0009	1.0911	2.1349				
6	0.25	4.7366	0.5716	6.0240	0.5764	5.5353	0.3486			
7	1.00	2.1666	1.1115	3.0936	1.1735	3.0936	1.1115	2.1666		
8	0.25	4.7966	0.5803	6.1592	0.6005	6.1501	0.5836	5.5869	0.3515	
9	1.00	2.1797	1.1192	3.1214	1.1897	3.1746	1.1897	3.1214	1.1192	2.1797

Bessel Filter

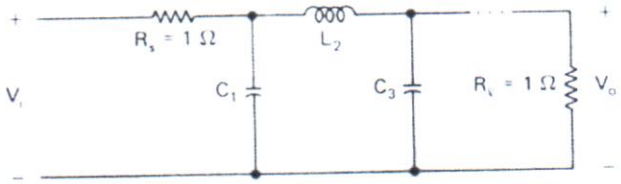


Fig. 8-23 A basic circuit structure for low-pass Bessel filters.

Filter order

TABLE 8-4 Values of Circuit Elements in Bessel Filters

n	C_1	L_2	C_3	L_4	C_5	L_6	C_7	L_8	C_9
1	2.0000								
2	1.5774	0.4226							
3	1.2550	0.5528	0.1922						
4	1.0598	0.5116	0.3181	0.1104					
5	0.9303	0.4577	0.3312	0.2090	0.0718				
6	0.8377	0.4116	0.3158	0.2364	0.1480	0.0505			
7	0.7677	0.3744	0.2944	0.2378	0.1778	0.1104	0.0375		
8	0.7125	0.3446	0.2735	0.2297	0.1867	0.1387	0.0855	0.0289	
9	0.6678	0.3203	0.2547	0.2184	0.1859	0.1506	0.1111	0.0682	0.0230

FILTER TRANSFORMATIONS

TABLE 8-5 Frequency and Element Transformations

From Normalized Low-pass Filter to:	Frequency Transformations	$R\ \Omega$	L H.	C F.
A low-pass filter with cutoff frequency ω_c	$s \longrightarrow \frac{s}{\omega_c}$	$R\ \Omega$	$\frac{L}{\omega_c}$ H.	$\frac{C}{\omega_c}$ F.
A bandpass filter with center frequency ω_0 and bandwith B	$s \longrightarrow \frac{s^2 + \omega_0^2}{Bs}$	$R\ \Omega$	$\frac{L}{B}$ H $\frac{B}{\omega_0^2 L}$ F.	$\frac{C}{B}$ F. $\frac{B}{\omega_0^2 C}$
A band-reject filter with center frequency ω_0 and rejection bandwidth B	$s \longrightarrow \frac{Bs}{s^2 + \omega_0^2}$	$R\ \Omega$	$\frac{1}{BL}$ F. $\frac{BL}{\omega_0^2}$ H.	$\frac{1}{BC}$ H. $\frac{BC}{\omega_0^2}$ F.
A high-pass filter with cutoff frequency ω_c	$s \longrightarrow \frac{\omega_c}{s}$	$R\ \Omega$	$\frac{1}{L\omega_c}$ F.	$\frac{1}{C\omega_c}$ H.
Impedance scaling by A	No change	$AR\ \Omega$	AL H.	$\frac{C}{A}$ F.

Selected Plots from

ANALOG AND DIGITAL FILTERS: DESIGN AND REALIZATION -- Harry Y-F. LAM

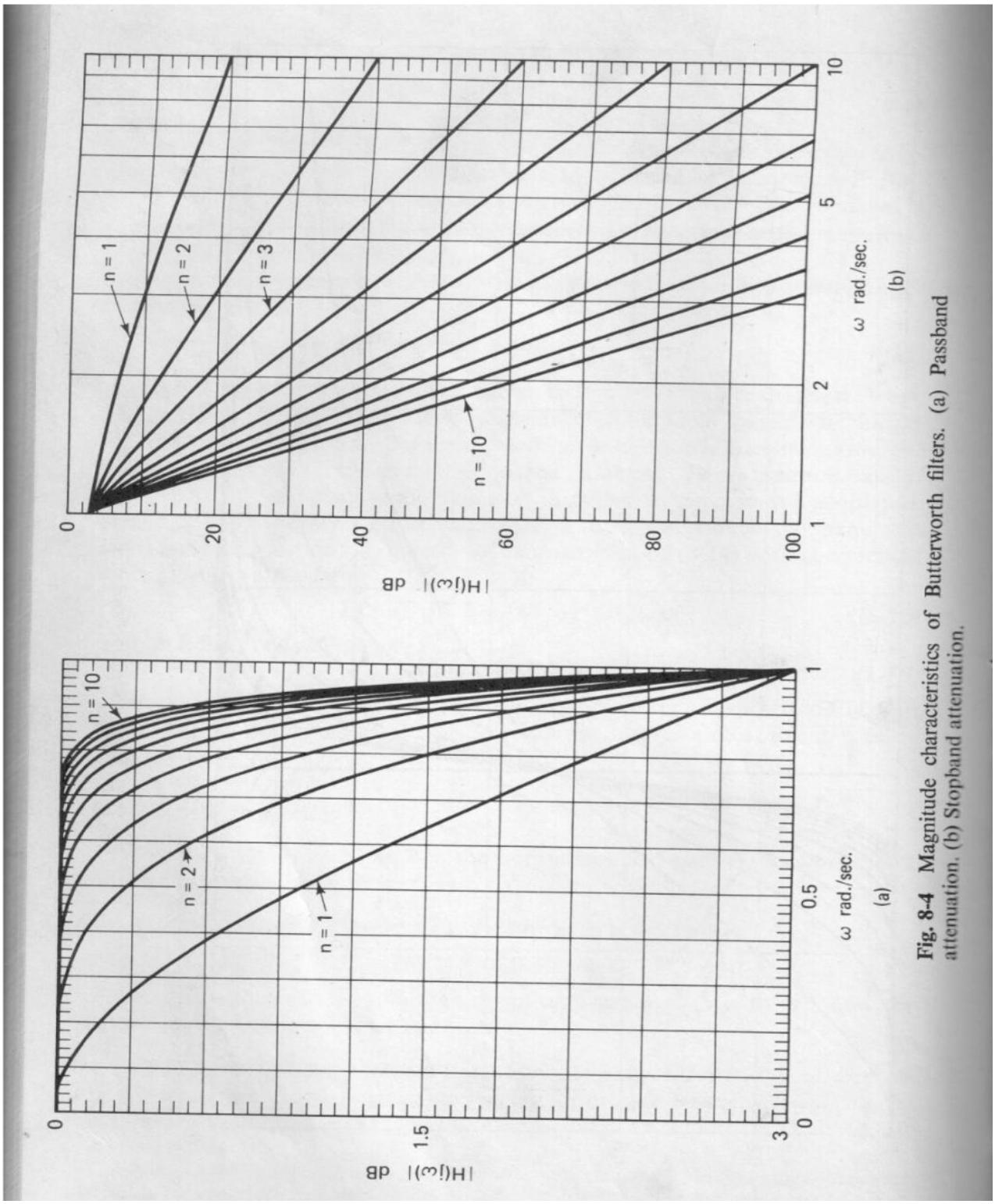


Fig. 8-4 Magnitude characteristics of Butterworth filters. (a) Passband attenuation. (b) Stopband attenuation.

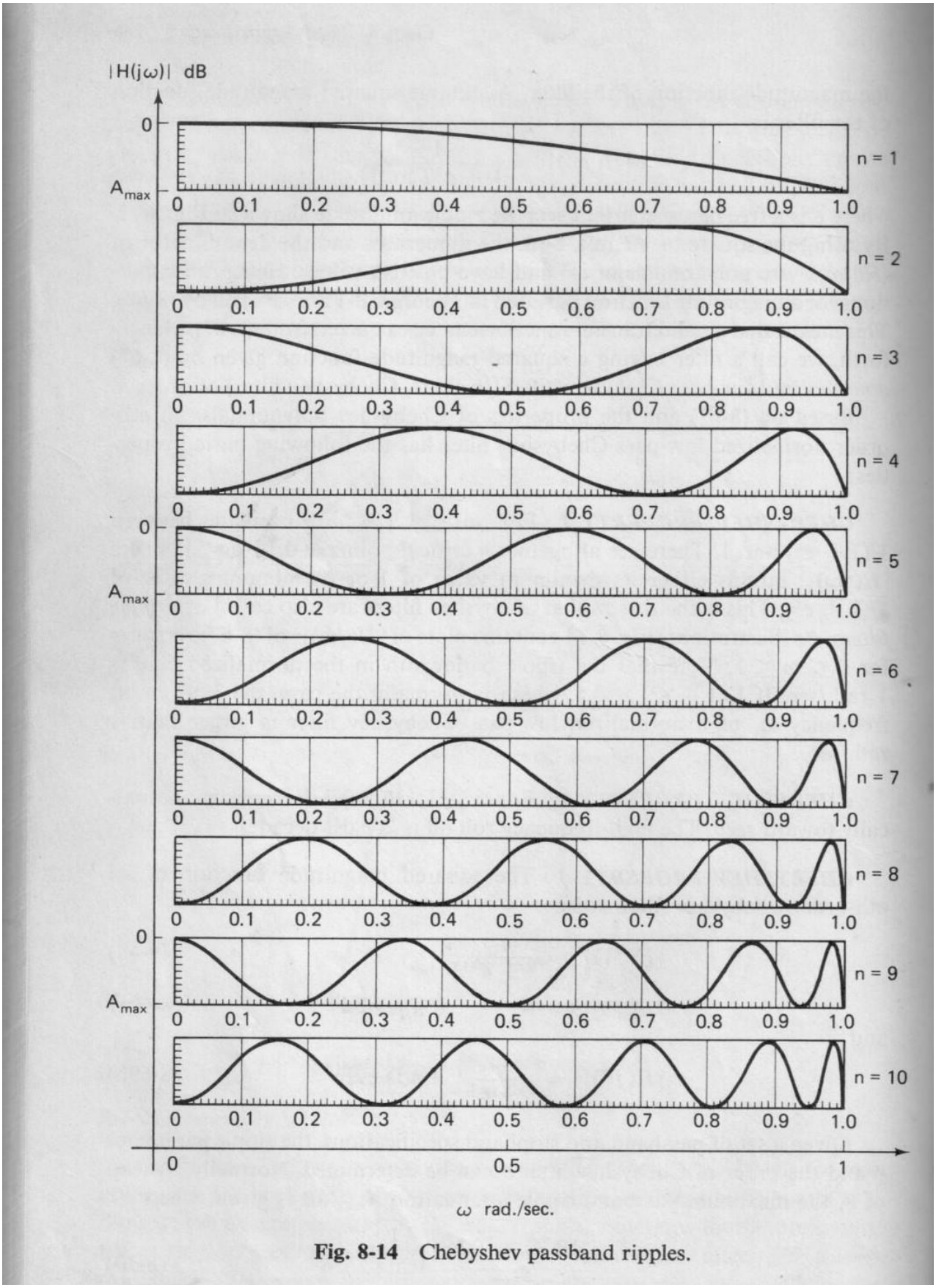


Fig. 8-14 Chebyshev passband ripples.

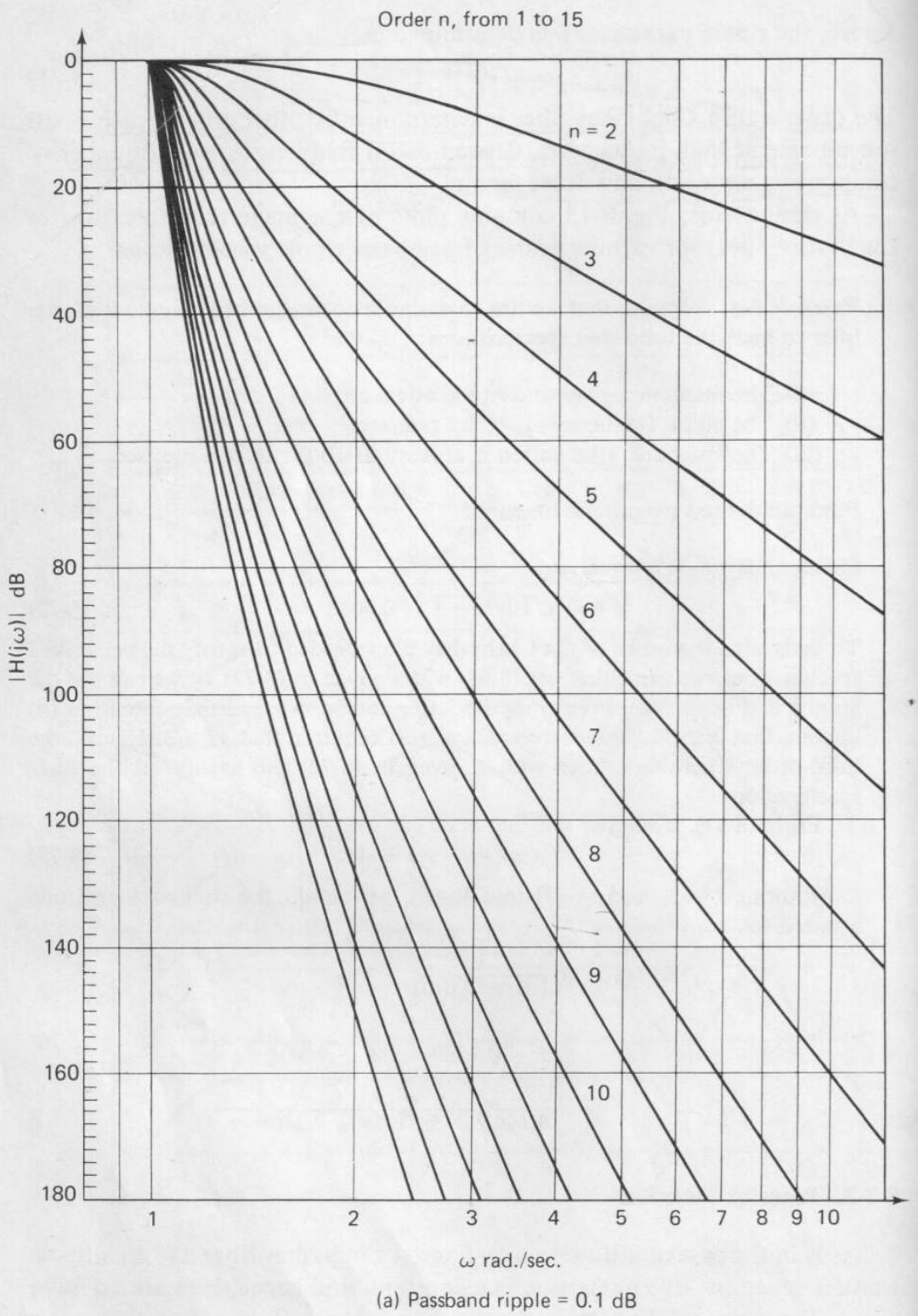
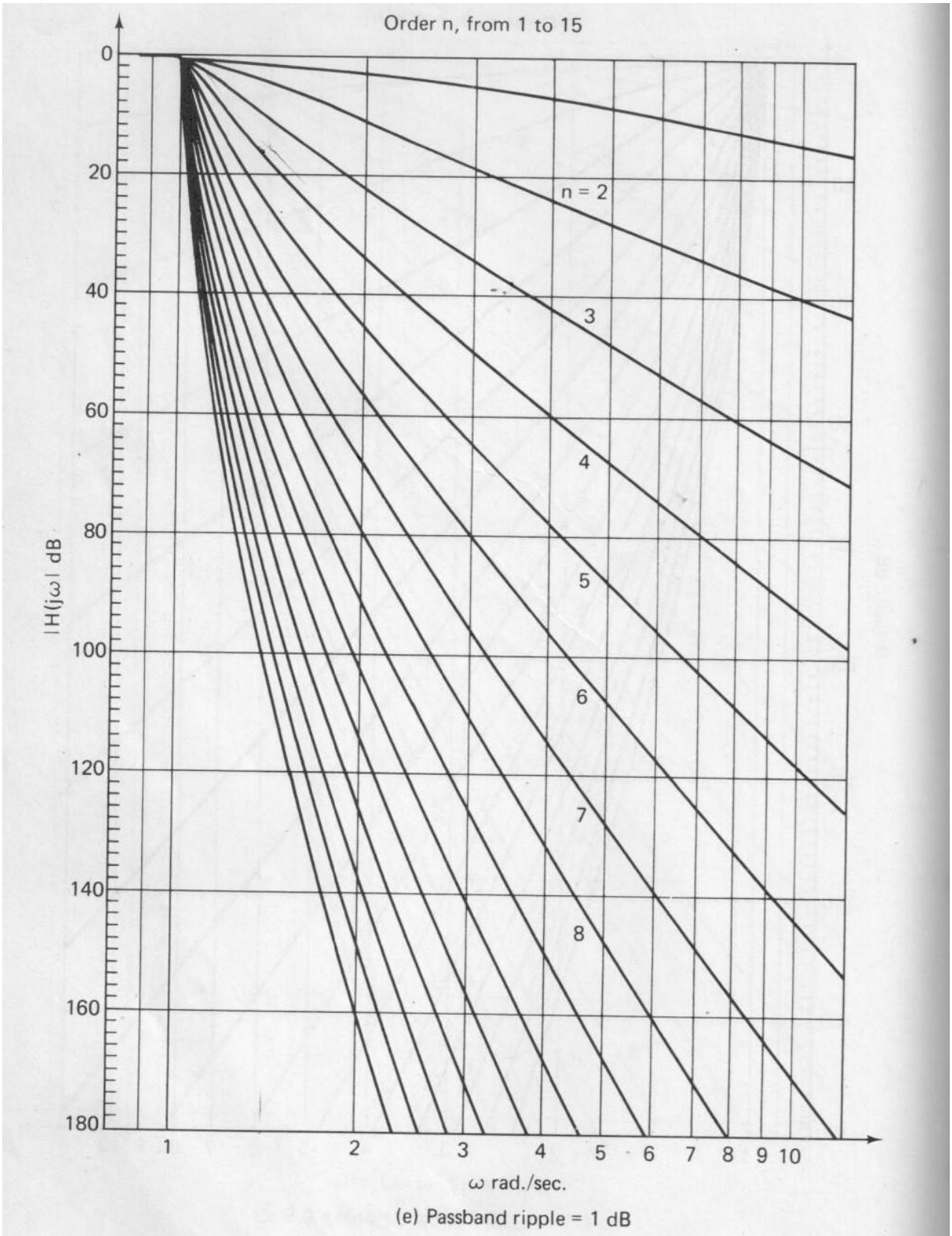


Fig. 8-15 Attenuation characteristics of Chebyshev filters.



(e) Passband ripple = 1 dB

Fig. 8-15 (continued)

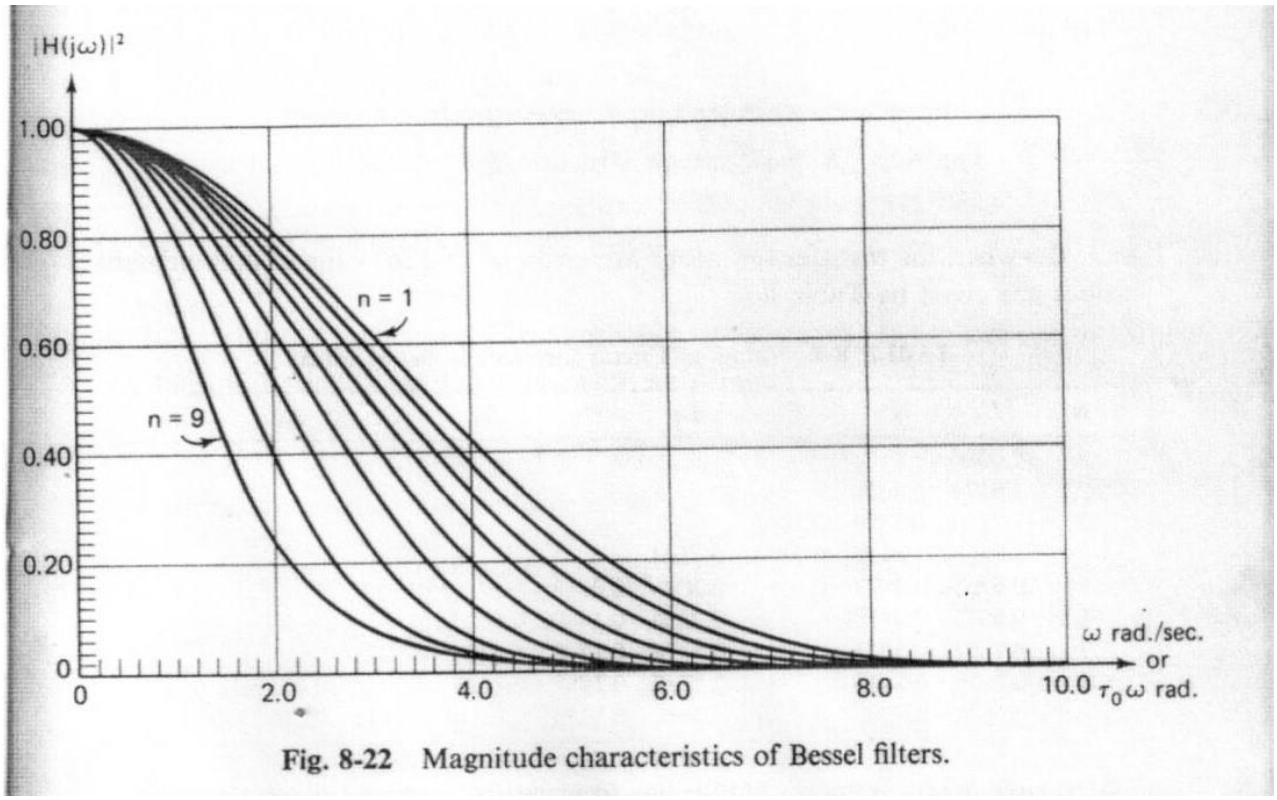


Fig. 8-22 Magnitude characteristics of Bessel filters.

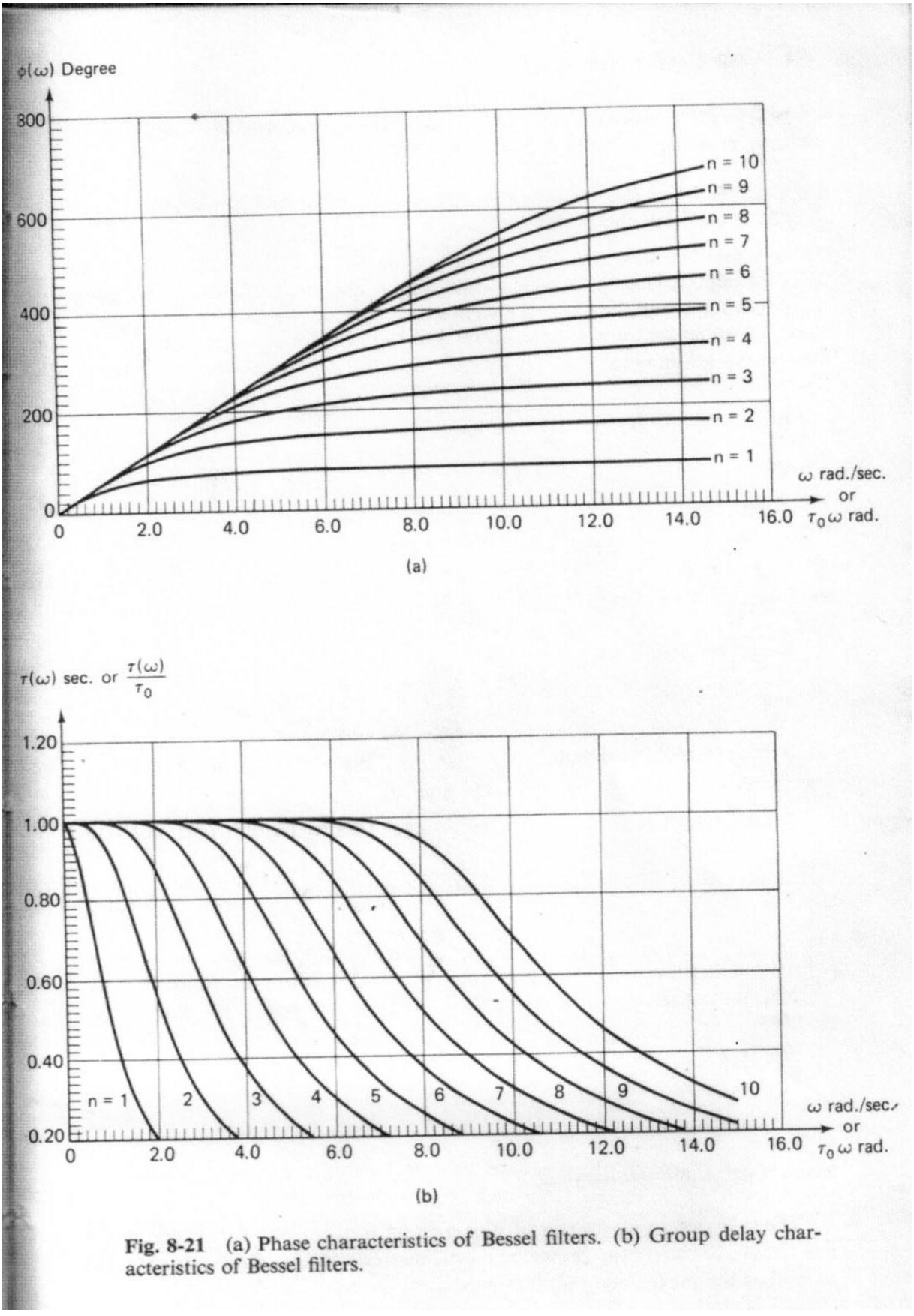


Fig. 8-21 (a) Phase characteristics of Bessel filters. (b) Group delay characteristics of Bessel filters.

CMOS Analog VLSI Design

Natural

Can you think of a digital signal in the world?

World around you is analog. Sound light Color

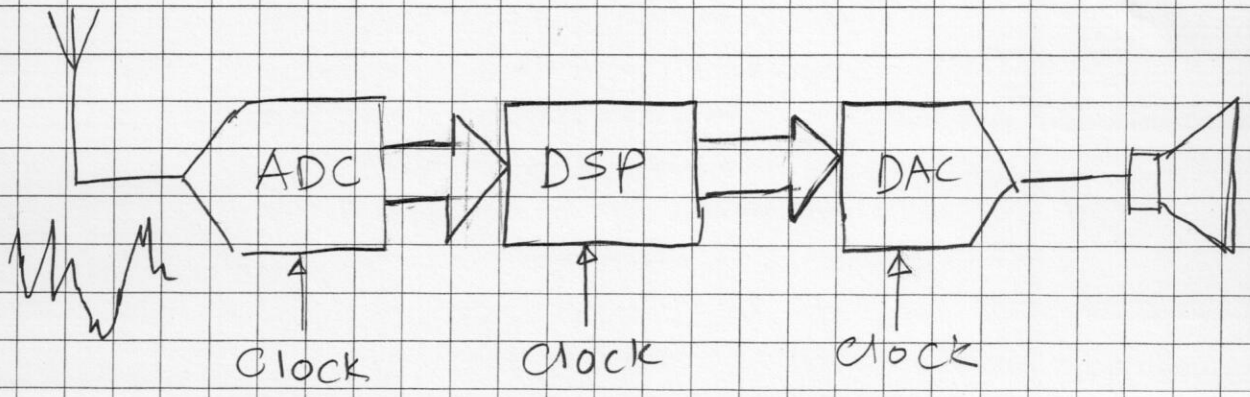
Signal processing in Analog is very difficult.

Digital Signal processing — Bits - Code.

— Repeatable - Reliable.

— Convert to digital as soon as possible

Example



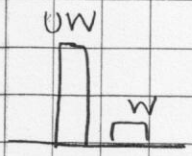
Example — 2.4GHz Wifi

→ At least 10G Clock frequency

→ Huge # of bits Needed to capture Strongest & Weakest signal.

→ Impractical

Analog Design



- Take continuous-time signal (from sensor)
- Remove unwanted signals.
- Sift out only desired signals.
- May be Shift them to lower frequen
- Amplify and condition the signals.
- ADC with lowest sampling rate
  - Save power - area.

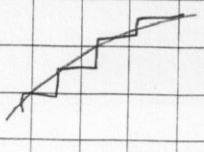
Then DSP takes over

On the other Side

Take digital signal.

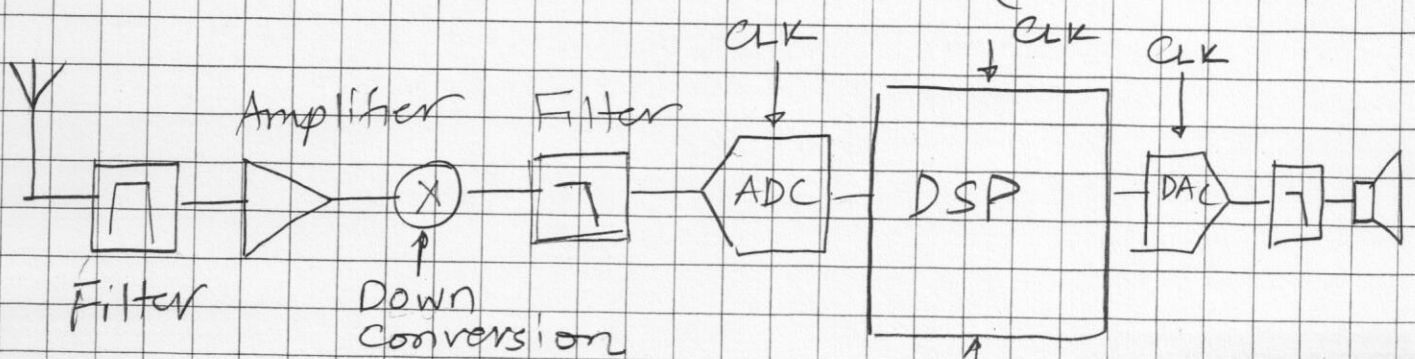
→ Convert to analog

→ Remove digital artifacts.



→ Amplify / condition signal

→ Drive speakers - other devices. (Actuators)

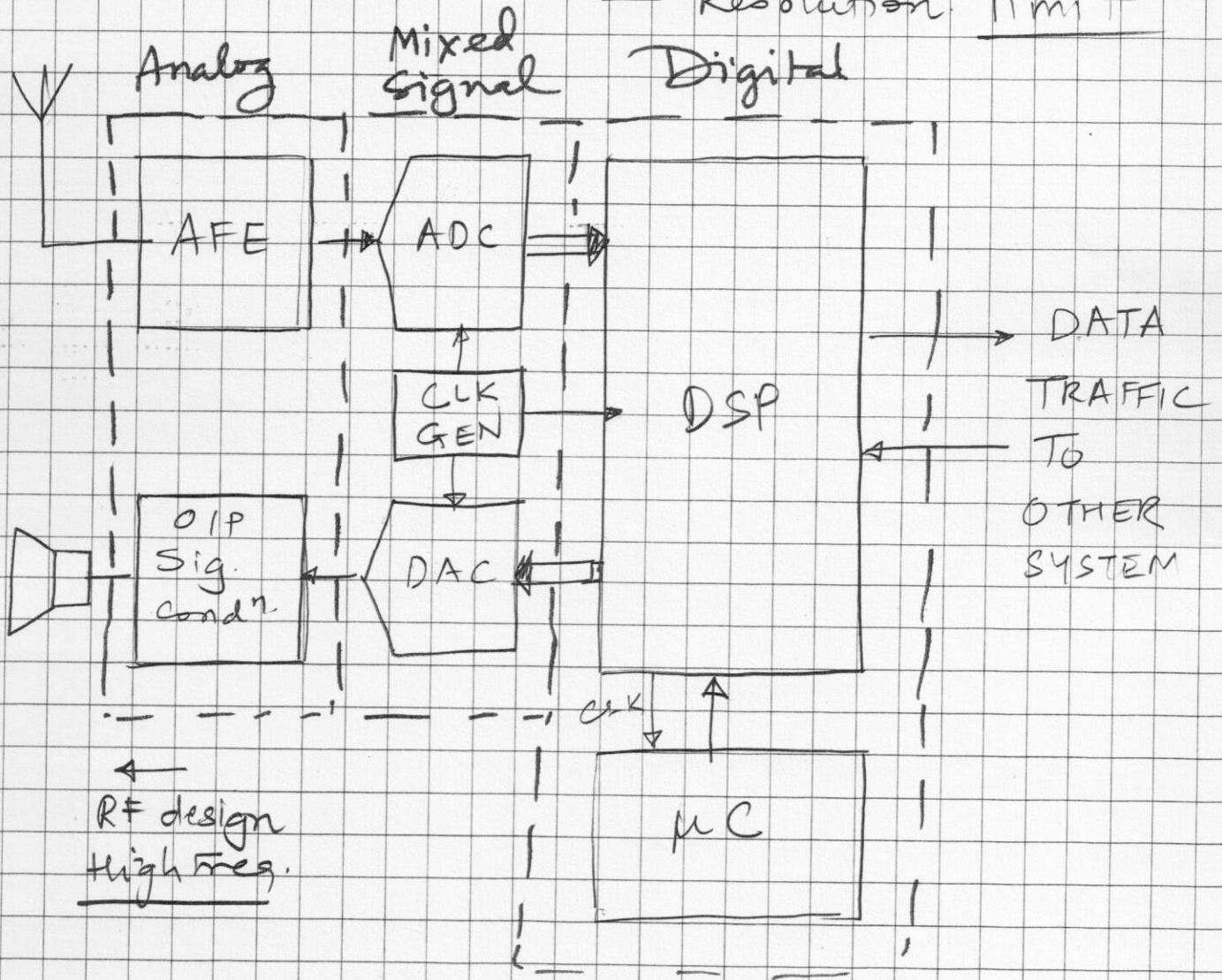


Analog TV example – Gradual Degradation of SNR

Digital TV – Near perfect picture till just it dies.

Analog signal – susceptible to Noise

Digital signal – # of bits you process → Resolution limit



All together System-on-chip.

→ Implications Noise coupling

ANALOG DESIGN CHALLENGES

① Device ← NOISE, LINEARITY → Performance Degradation

② Digital drives → Feature size → (Bad analog beh)
supply voltage downwards.
↳ Analog dynamic range ↓

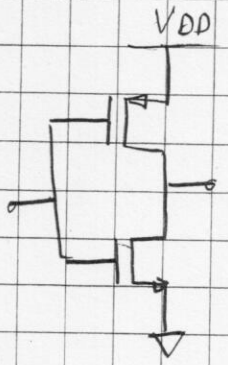
③ Circuit complexity high. to make analog performance independet of
PVT → operating Temperature
process variations
Supply voltage Variation

④ 65nm Technology → 28nm Technology
Digital will scale - Automated to most extent
Analog Handcrafted artwork
→ Redo

Analog-Mixed-Signal - RF designers always in high demand.
— commanding in job prospect
— Experience imp if you are good

CMOS Technology

◎ Show crosssection here



Main Driver → 2 devices for inverter
→ Zero static power
→ scalable (dimensions)
→ minimum # of mask
→ Vdd ↓ lower power
CV^2f

Bipolar - vertical devices - supersmall base width region
└ superfast - HF

$V_{BE} = 0.7V$

$V_{DD} = \sim 2V$ min

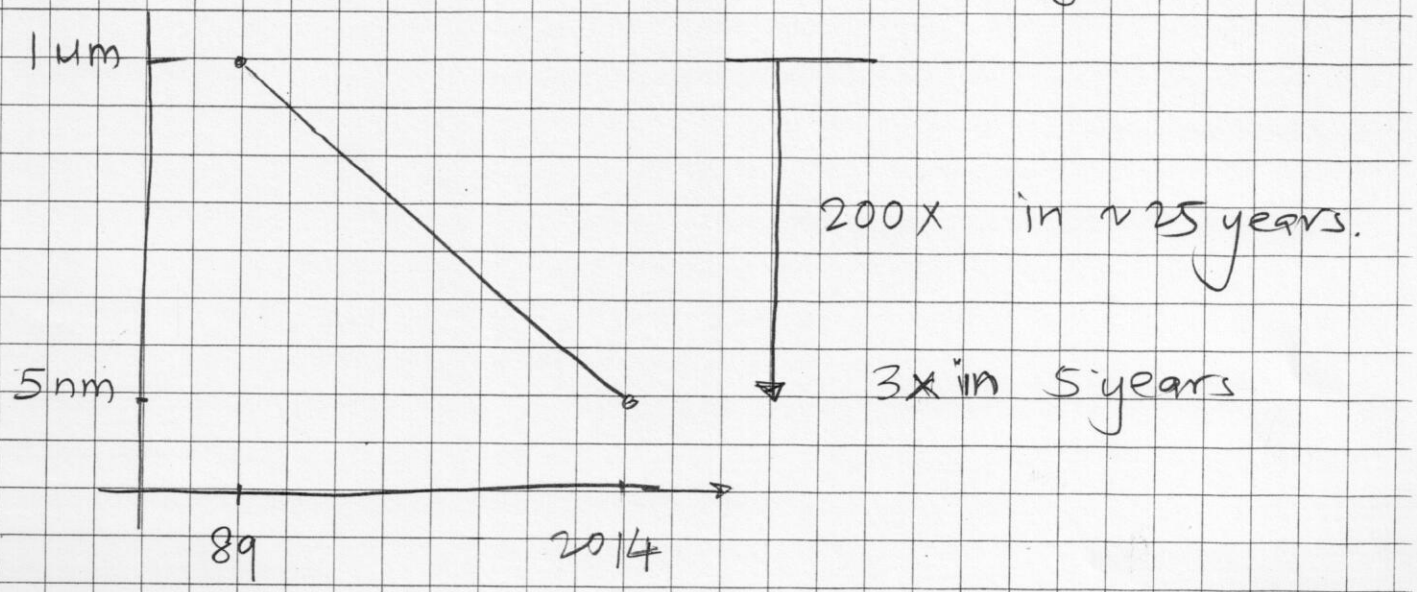
CMOS - action happens laterally - gate length
- slower compared to Bipolar.
- with scaling Lmin 28nm - going down to 5nm
- Speed matches Bipolars. f_T 100GHz +
- analog performance of transistors suffers with scaling
- Digital free - use to compensate analog ckt imperfection.

Vdd ↓ to 1V
↓
lower power designs

Analog + digital integration advantage.

→ Process complexity
→ Models accuracy
→ supply voltage. - challenge to do HV design

CMOS Feature Size → (min Gate length)



As Analog Girl / Guy

→ Creativity must to solve tough problems due to reducing supply voltage & transistor dimensions

→ In SOC (System-on-chip) - Sensitive Analog must co-exist with very Noisy digital.

- Noise insensitive architecture (diff ckts)
- Effect of Substrate / bondwire / magnetic / electrical Coupling
- Effect of Packaging. - must take into account at beginning
- Floorplanning very important

Analog parts - often run on high voltage
→ Device reliability - Important

- Device modeling
- Layout dependent effects.
  - Transistor matching
  - Layout parasitics
  - Electro-migration in metals.

A lot of Neurons

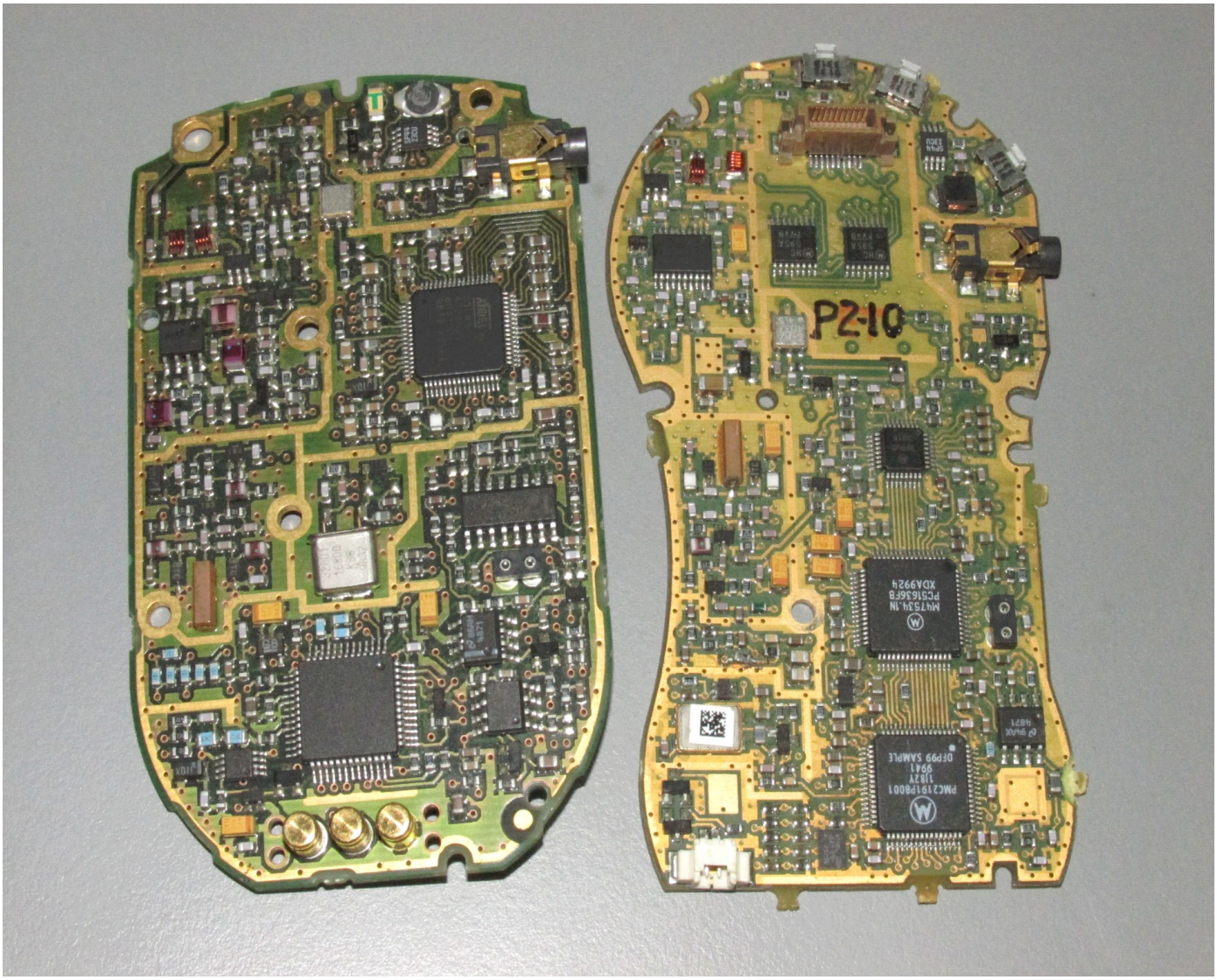
Efforts

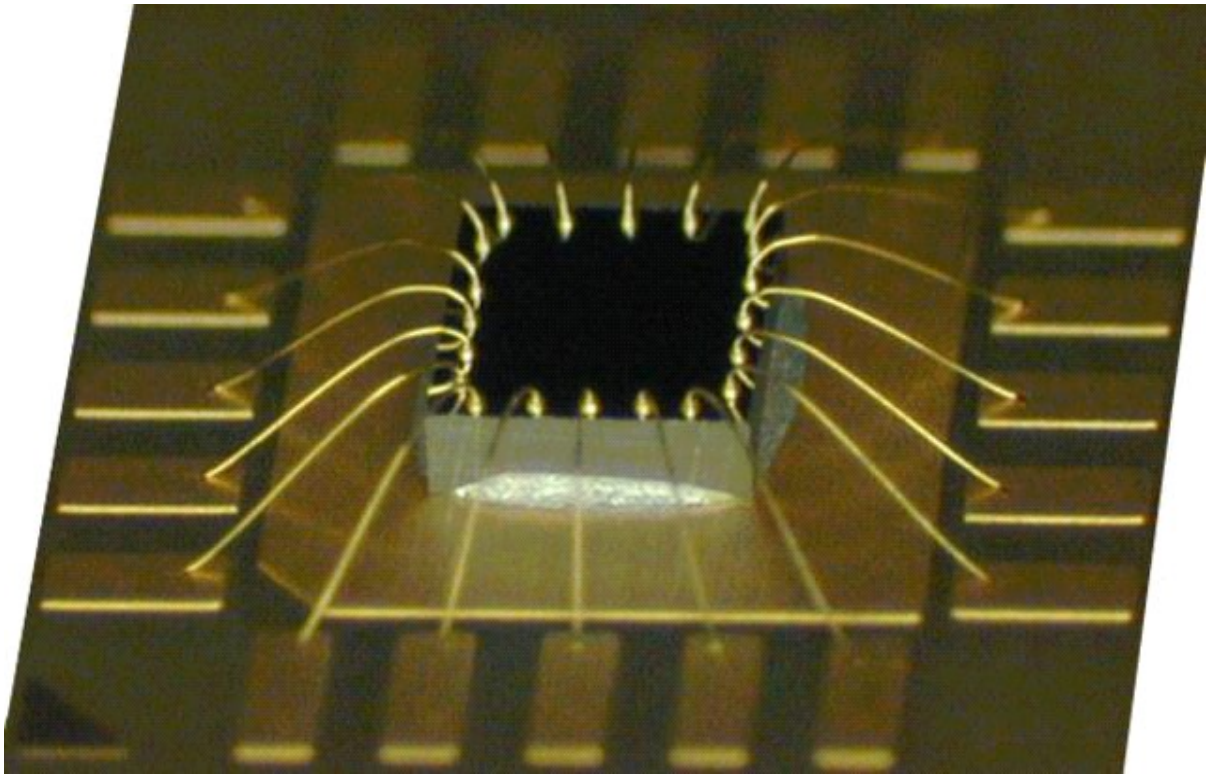
1/3	1/3	1/3
schematic design	Layout effects	Measurement & debug

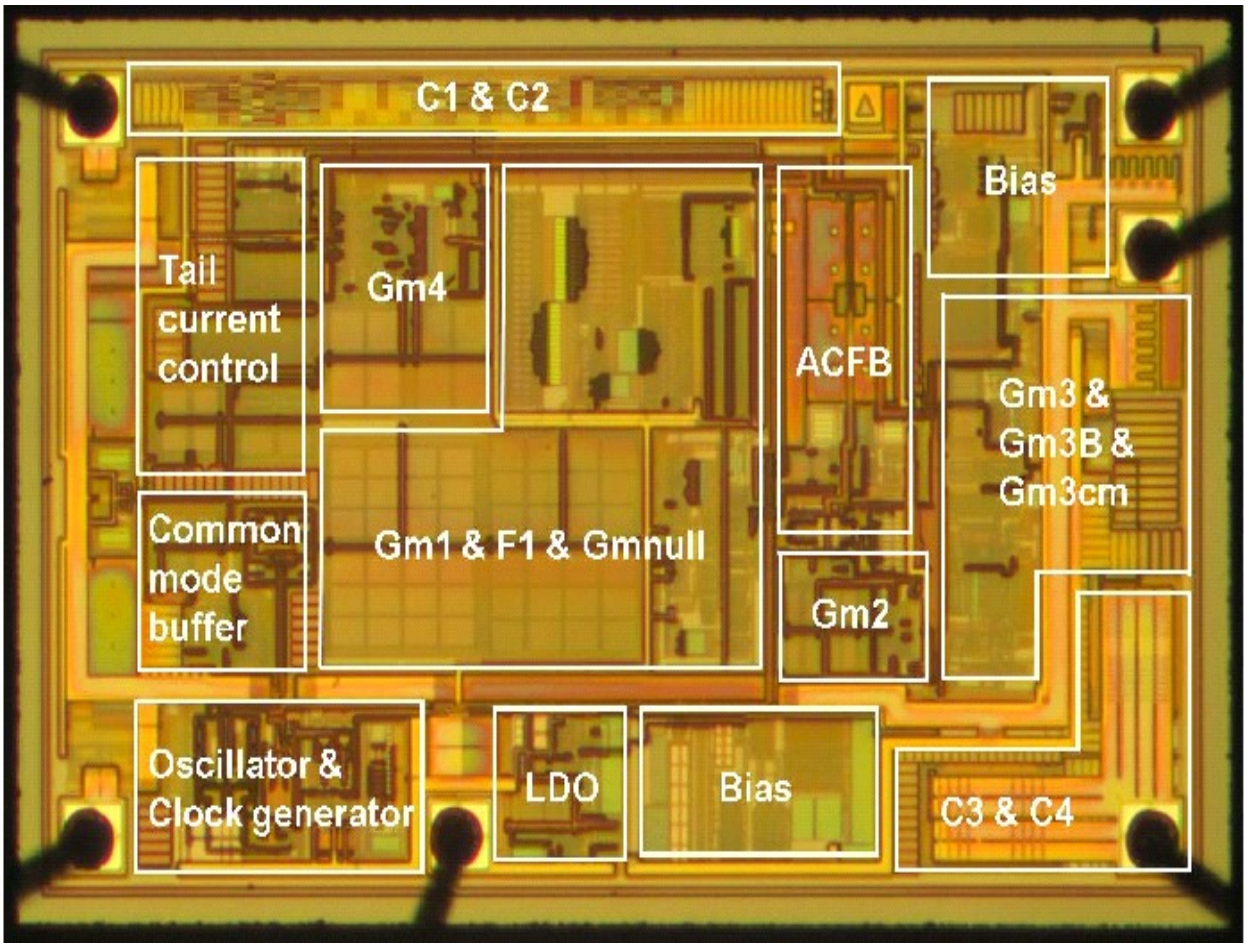
SHOW & TELL

TEXT BOOK

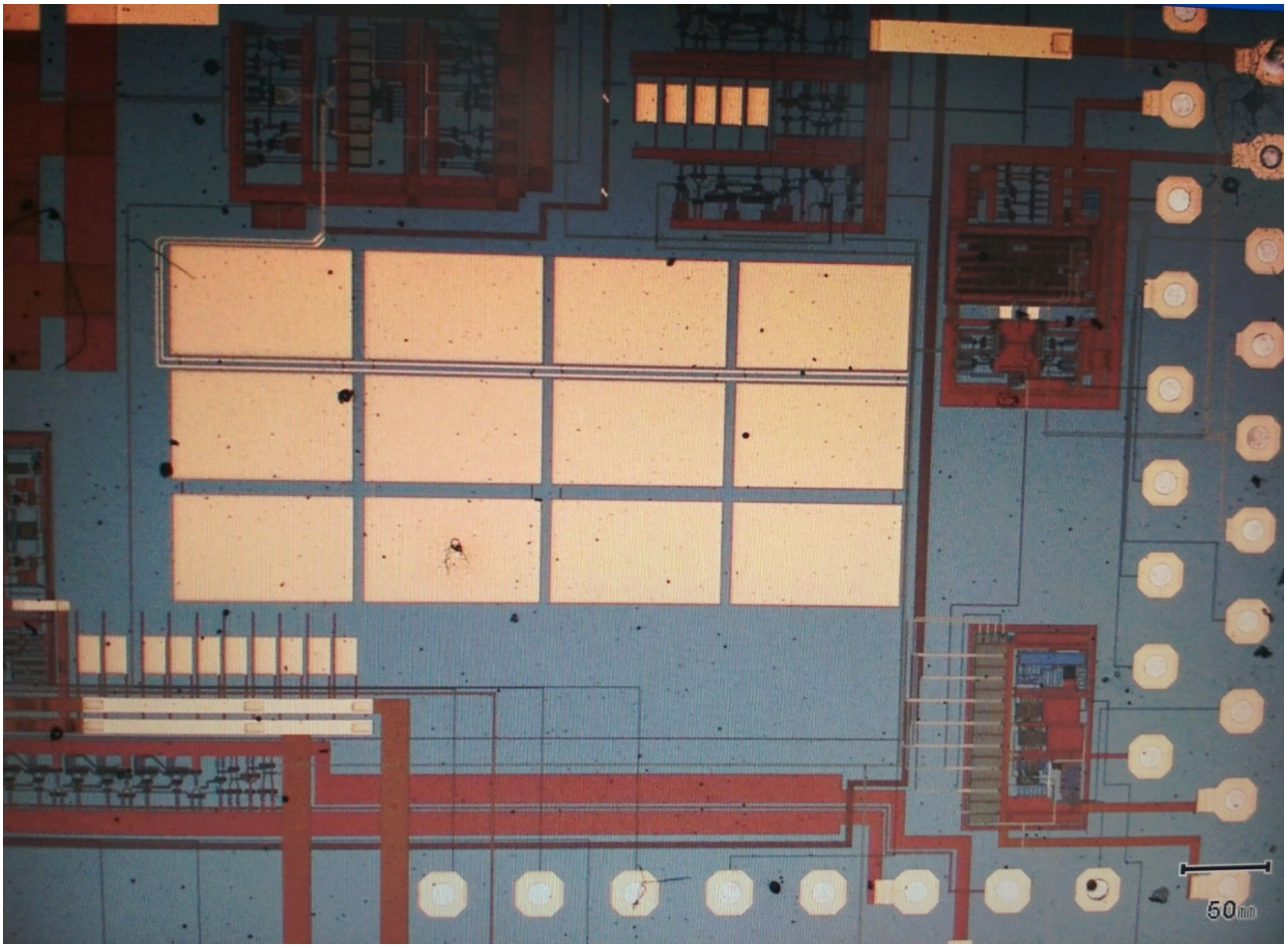
- Design of Analog CMOS ICs
  - B. Razavi (1st or 2nd Edition)
- Various papers for specific topics.

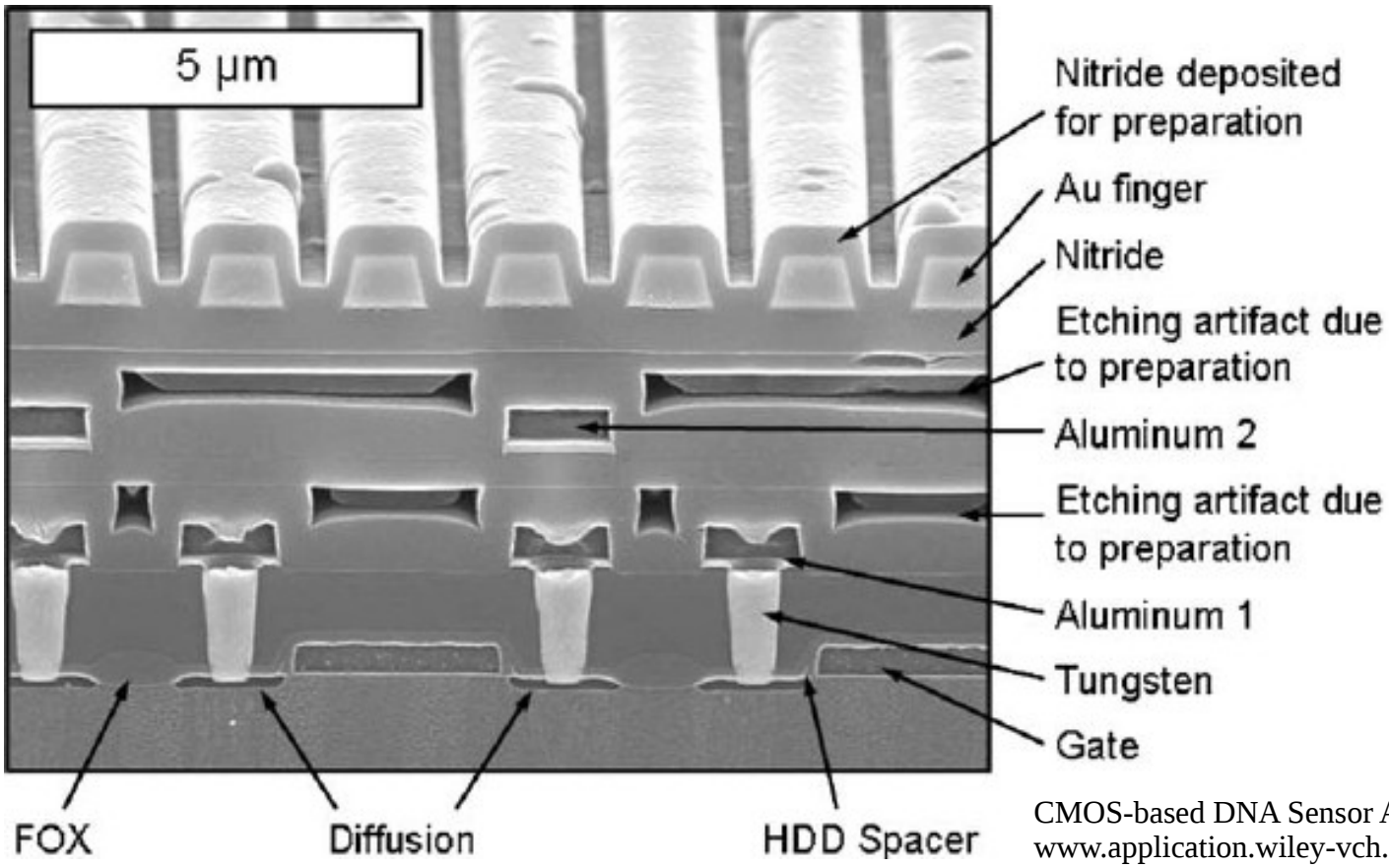

P2-10





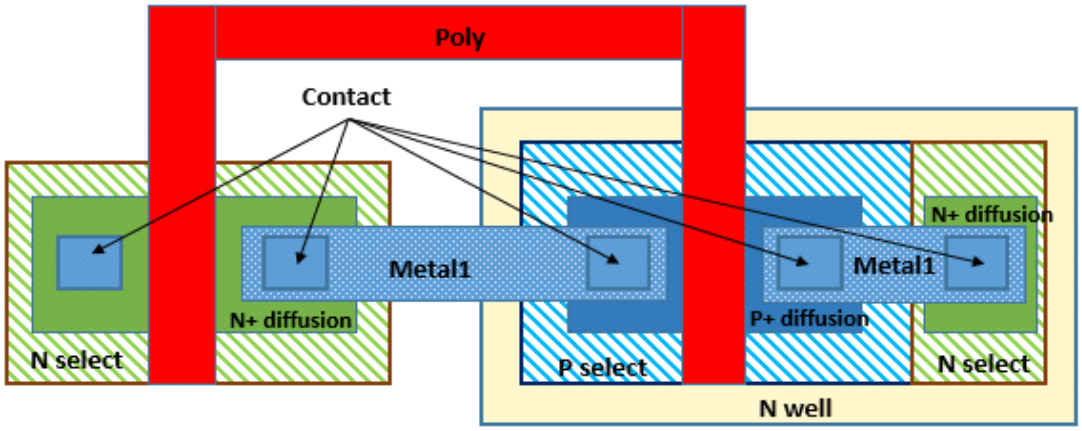
DOI:10.1109/JSSC.2016.2577626



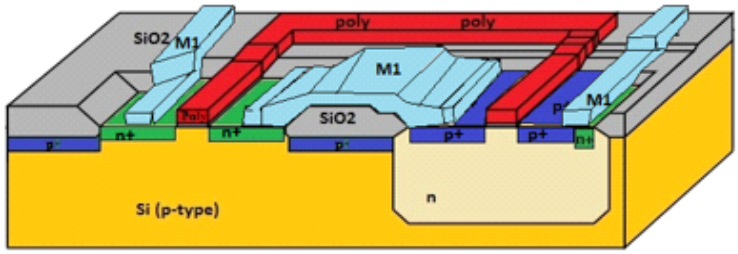


CMOS-based DNA Sensor Arrays
www.application.wiley-vch.de

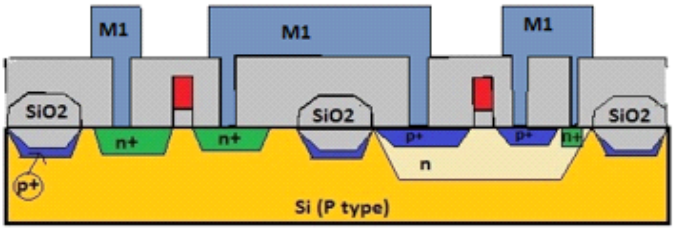
Top View



3D View

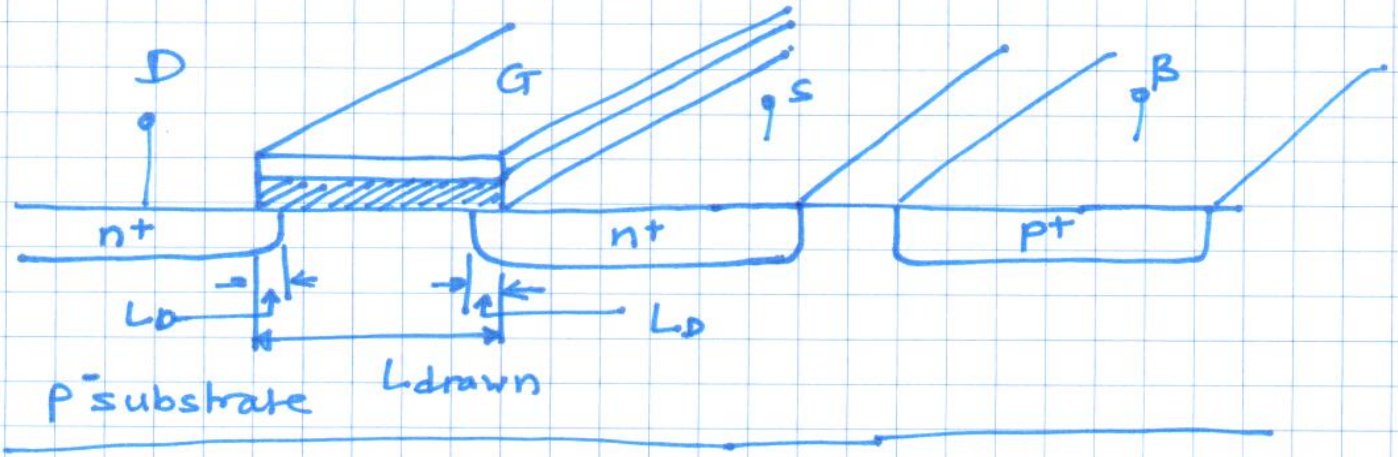


Side View



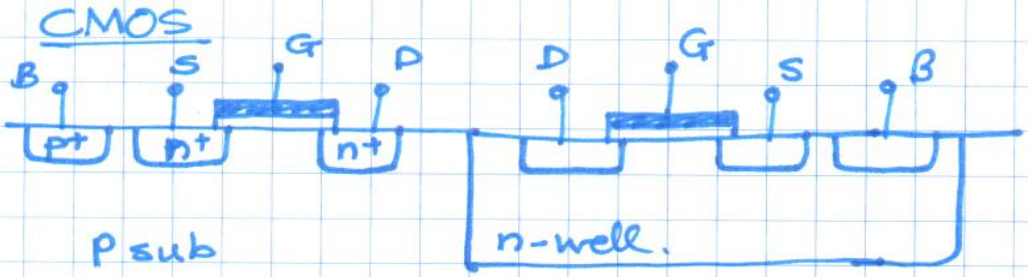
2AUG2019

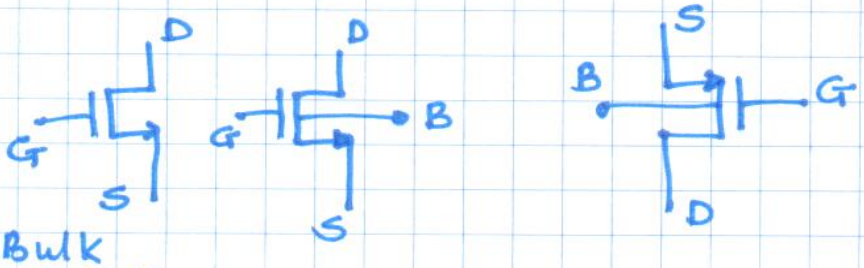
NMOS transistor



* L_D due to side diffusion
* $L_{eff} = L_{drawn} - 2.L_D$.
* S-D interChangable
* S- source of charge carriers
  D - drain - collects charge carriers & removes them.

CMOS





Bulk implicit gnd.

Bulk connection implicit Vdd.

* Why polysilicon instead of Metal for gate

→ Polysilicon – allows transistor gate definition very accurately – self aligned process. → smaller & faster transistor.

→ doping process – high temp

→ poly can withstand high temp. Metal/AL melt

→ V_T reduction ϕ_{ms} ← poly to s work function.

with Metal. – high V_T.

$$\phi_{ms} = \phi_{F_{sub}} - \phi_{F_{gate}}$$

n type poly.

$$= \frac{KT}{q} \ln\left(\frac{n_i}{N_A}\right) - \frac{KT}{q} \ln\left(\frac{N_D}{n_i}\right)$$

N_A – psub

$$= \frac{KT}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right)$$ ← can be changed.

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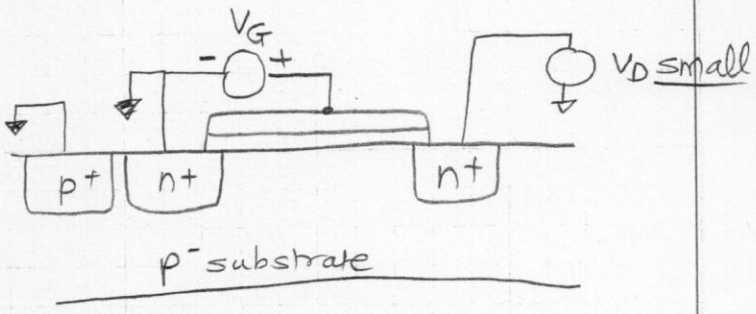
ANALOG CMOS IC DESIGN

MOS DEVICE PHYSICS BASICS

NMOS crosssection



As V_G ↑, holes in p-substrate repelled leaving behind -ve ions. (depletion region). As V_G ↑ further width of depletion region increases. Cap divider effect between gate - oxide interface - substrate. When V_G increases beyond V_{TH} sufficient positive value, e^- flow from source to the interface & drain - channel formed. (Inversion)

V_{TH} - Threshold voltage $= \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}$

Φ_{MS} - work function difference bet^n gate & sub.

Surface potential $\Phi_F = \frac{KT}{q} \ln\left(\frac{N_{sub}}{N_i}\right)$ → doping density; → e^- density in undoped Si

Q_{dep} = Charge in depletion region.

$= \sqrt{4q\epsilon_{si}|\Phi_F|N_{sub}}$

ϵ_{si} ~ dielectric constant

C_{ox} - Gate Oxide cap.

$\epsilon_{si} = 11.68$

$\epsilon_{SiO_2} = 3.97$

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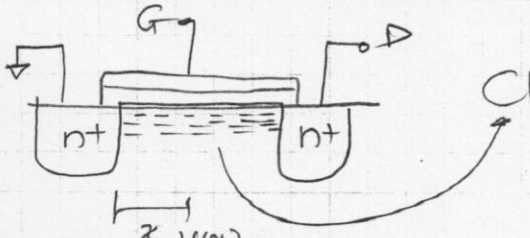
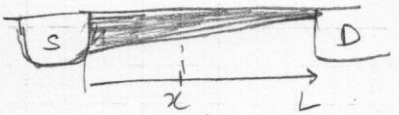


$Q_d = W C_{ox} (V_{GS} - V_{TH})$ @ $V_{GS} = V_{TH}$ Channel Begins to form.

$$Q_d(x) = W C_{ox} [V_{GS} - V(x) - V_{TH}]$$



↑ Channel potential @ position x from source.

$$I_{DS}(x) = -W C_{ox} [V_{GS} - V(x) - V_{TH}] v \leftarrow \text{Charge velocity}$$

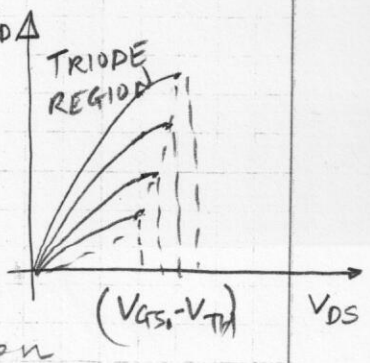
$$= \mu_n E = \mu_n \frac{dV(x)}{dx}$$

$$I_{DS} = W C_{ox} [V_{GS} - V(x) - V_{TH}] \mu_n \frac{dV(x)}{dx}$$

$$\int_0^L I_{DS}\, dx = \int_0^{V_{DS}} \mu_n W C_{ox} [V_{GS} - V(x) - V_{TH}]\, dV(x)$$

$$L \cdot I_{DS} = \mu_n C_{ox} W \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$



TRIODE Region

for $V_{DS} \ll 2(V_{GS} - V_{TH})$

$$I_{DS} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$$

$$R_{ON} = \left(\frac{\partial I_{DS}}{\partial V_{DS}} \right)^{-1} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_{TH})}$$

Linear Region

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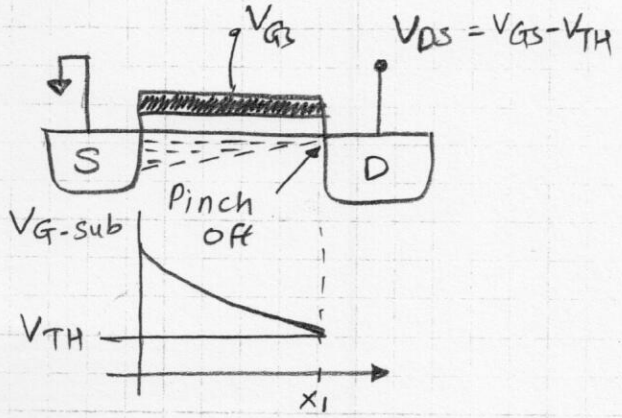
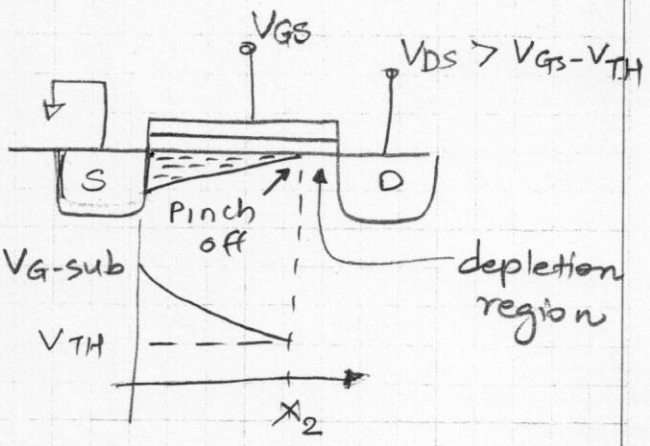
When $V_{DS} > V_{GS} - V_{TH}$





$V(x_1) = V_{GS} - V_{TH}$

Remember $Q_d(x) = W C_{ox} [V_{GS} - V(x) - V_{TH}]$

@ pinch off point $Q_d(x) = 0$ $V(x) = V_{GS} - V_{TH}$

As e^- (carriers) approach pinch-off point, their velocity rises big time. ($v = I/Q_d$) → electrons shoot through the depletion region. & arrive @ drain.

After pinch-off - device is in saturation region.

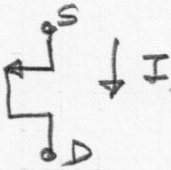
$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L'} (V_{GS} - V_{TH})^2$$

{ integration from $V(x) = 0 \rightarrow (V_{GS} - V_{TH})$

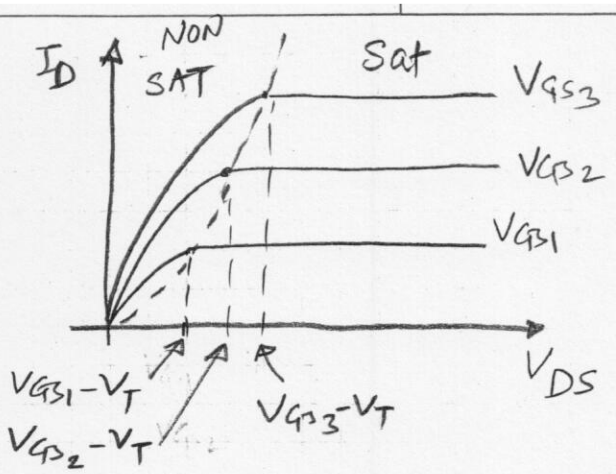
L' where channel pinches off

$V_{GS} - V_{TH}$ ⇒ called V_{dsat}

$V_{DS} > V_{dsat}$ Required for Saturation region op.

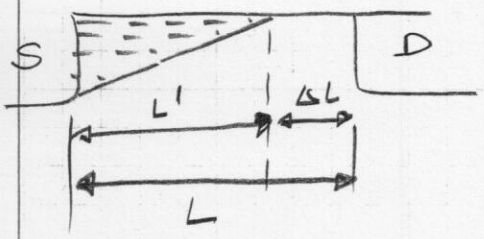
* PMOS devices 

$$I_D = \frac{1}{2} \mu_p C_{ox} \frac{W}{L'} (V_{SG} - |V_{THp}|)^2$$



Channel length Modulation

Recall pinch-off in saturation



L' is function of V_{DS}

$$\frac{\Delta L}{L} = \lambda V_{DS} \quad \text{(in saturation)}$$

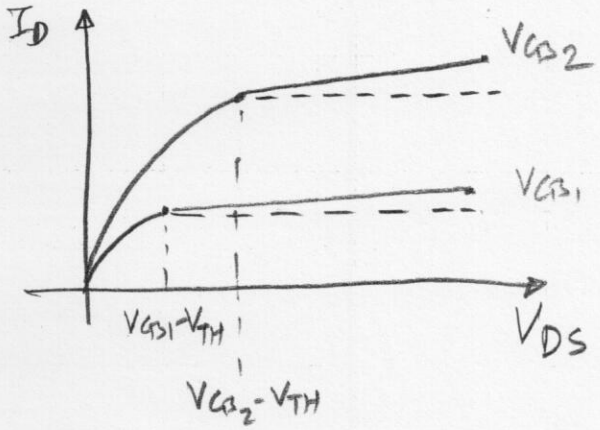
$$\frac{L'}{L} = \frac{L-\Delta L}{L} = (1-\lambda V_{DS})$$

$$\frac{1}{L'} = (1+\lambda V_{DS})\frac{1}{L}$$

$\lambda \rightarrow$ Channel length modulation coeff.

Substituting in sat equation

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$



$$\frac{\Delta L}{L} = \lambda V_{DS}$$

Relative variation in length, due to V_{DS}

Longer L

Smaller λ

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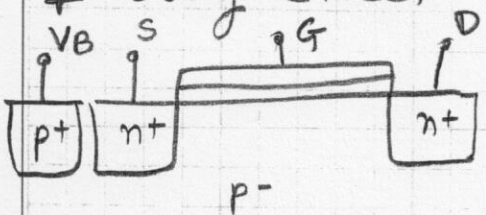
★ Body Effect



Body - backgate acts like another gate affecting channel

$\uparrow V_{SB} \rightarrow \uparrow V_T$

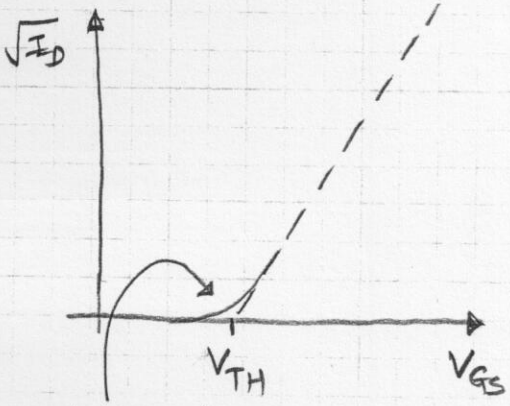
$$V_{TH} = V_{TH_0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right) \qquad \gamma = 2$$

Body Effect Coefficient $\gamma = \dfrac{\sqrt{2q\epsilon_{Si}N_{sub}}}{C_{ox}} \sim 0.3\text{-}0.4\ \sqrt{V}$

$\uparrow V_{BS}$ $\downarrow V_T$ can be used to reduce V_T by forward biasing V_{BS}.

→ make sure current is limited after forward biasing.

★ Subthreshold Conduction.



Subthreshold (weak inversion)

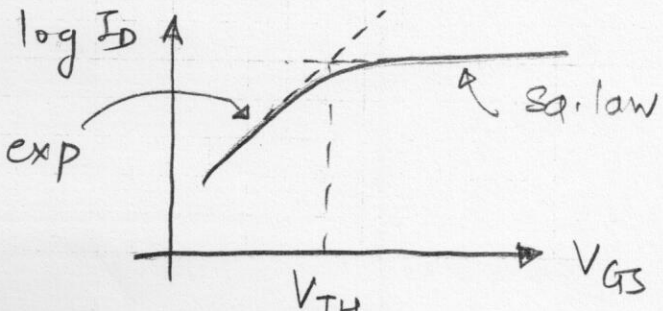
Even for $V_{GS} < V_{TH}$

— finite I_D - exponential dependence on V_{GS}

$$I_D = I_0 \exp\frac{V_{GS}}{\xi V_T}$$

$\xi > 1$; $V_T = \dfrac{kT}{q}$

Similar to $I_C - V_{BE}$ of bipolar transistor



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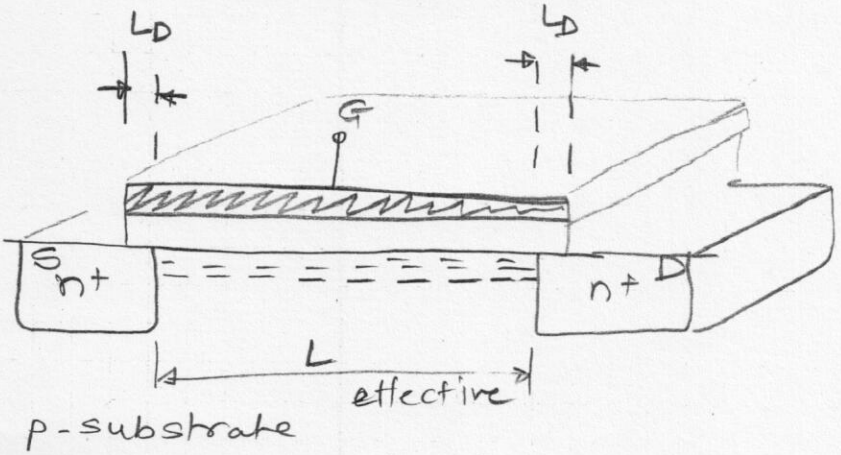
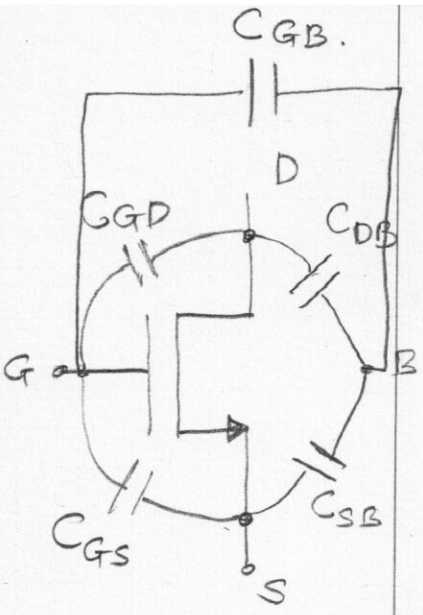
MOS device Capacitances





Device is off

$C_{GD} = C_{GS} = C_{ov} \cdot W$ ($C_{ov} = L_D \cdot C_{ox}$)

$C_{GB} = C_{ox} WL$ series with C_d ← depletion sub. cap. $= WL\sqrt{q\epsilon_{si}\frac{N_{sub}}{\phi_F}}$

Device is in triode region — $WL\,C_{ox}$ equally divided both gate & source/drain term.

$$C_{GD} = C_{GS} = \frac{WL\,C_{ox}}{2} + W\,C_{ov}$$

($C_{ov} = L_D \cdot C_{ox}$)

$C_{GB} = 0$

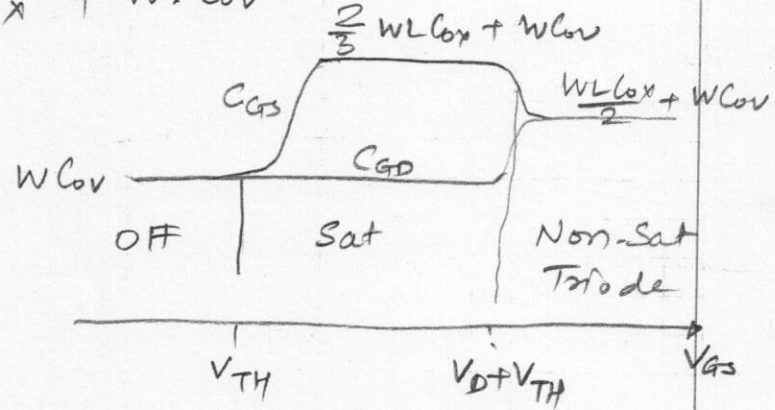
Device is in saturation region — pinch off channel

$C_{GD} = C_{ov} \cdot W$

$C_{GS} = \frac{2}{3} WL\,C_{ox} + W \cdot C_{ov}$ ($C_{ov} = L_D \cdot C_{ox}$)

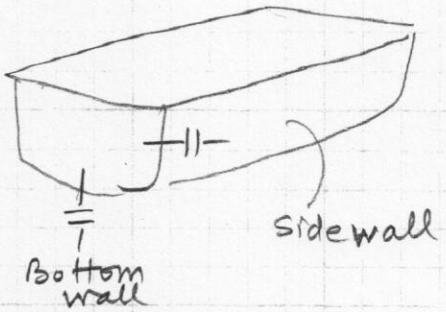
Muller Kamins proof ←

$C_{GB} \approx 0$



Drain / source → bulk cap.

$$C_{DB} = \underbrace{\frac{C_J \cdot A_D}{\left(1 + \frac{V_{DB}}{P_B}\right)^{MJ}}}_{\text{Bottomwall}} + \underbrace{\frac{C_{JSW} \cdot P_D}{\left(1 + \frac{V_{DB}}{P_B}\right)^{MJSW}}}_{\text{Sidewall}}$$



$$C_{SB} = \frac{C_J \cdot A_S}{\left(1 + \frac{V_{SB}}{P_B}\right)^{MJ}} + \frac{C_{JSW} \cdot P_S}{\left(1 + \frac{V_{SB}}{P_B}\right)^{MJSW}}$$

C_J → source/drain bottomplate j^n cap/area F/m²

C_{JSW} → sidewall F/m

P_B → source/drain junction built-in potential V

MJ, MJSW → exponents (unitless) 0.3 to 0.4

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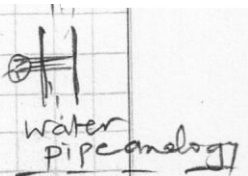
MOS small-signal MODEL in saturation

✱ Transconductance $g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}\text{ constant sat}}$



$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

V_{dsat}

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \cong \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})$$

$$g_m = \frac{2I_D}{(V_{GS}-V_{TH})} \quad \boxed{\text{EXACT}}$$

$$g_m \cong \sqrt{2\mu_n C_{ox}\frac{W}{L}\cdot I_D}$$

IMP. to commit to memory g_m transconductance

Insight Bipolar transistor $I_C = I_0 \cdot \exp\left(\frac{V_{BE}}{V_T}\right)$

Bipolar $g_m = \frac{\partial I_C}{\partial V_{BE}} = \frac{I_C}{V_T} \leftarrow 26\,mV$ $\quad \boxed{V_T = \frac{kT}{q}}$

Compare with MOS $g_m = \frac{I_D}{(V_{GS}-V_{TH})/2} = \frac{I_D}{100\,mV}$

$V_{dsat} \longrightarrow (V_{GS}-V_{TH})/2 \sim 200\,mV$

Bipolar g_m is 4x higher than MOS g_m for same current.

✱ Backgate transconductance

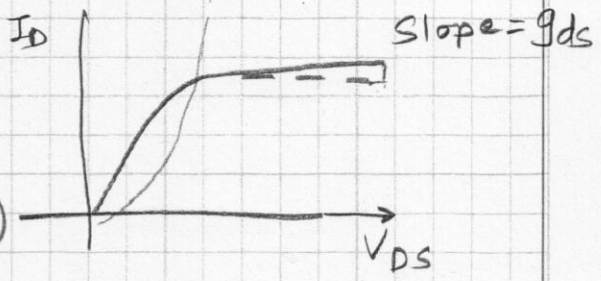
$$g_{mbs} = \frac{\partial I_D}{\partial V_{BS}} = \frac{\partial I_D}{\partial V_{TH}}\cdot\frac{\partial V_{TH}}{\partial V_{BS}} = \frac{\gamma}{2\sqrt{V_{SB}+2\phi_F}}\cdot g_m$$

$\frac{\partial I_D}{\partial V_{TH}} = -g_m$

$$= \eta\, g_m \quad (\eta \approx 0.25)$$

$$V_{TH} = V_{TH_0} + \gamma\left(\sqrt{V_{SB}+2\phi_F} - \sqrt{2\phi_F}\right)$$

Output conductance g_{ds}



$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

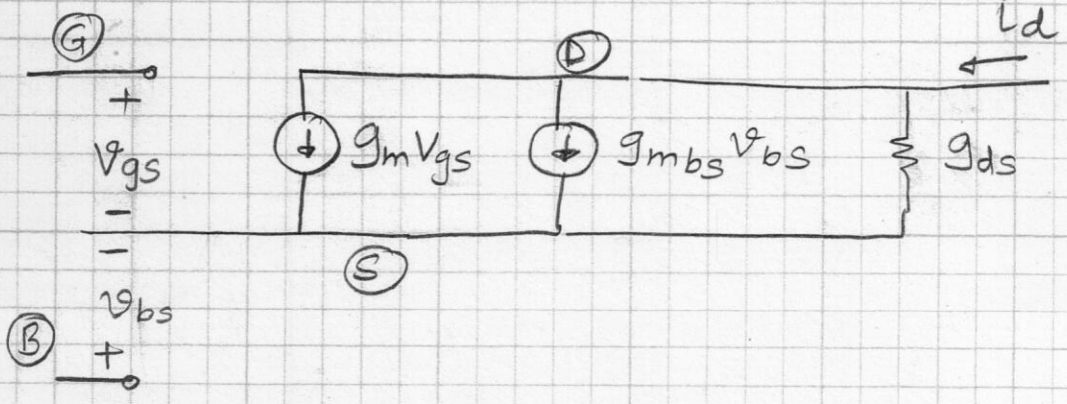
$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{TH})^2 \cdot \lambda = \frac{\lambda I_D}{(1+\lambda V_{DS})}$$

$$g_{ds} \simeq \lambda I_D \quad (\text{since } \lambda V_{DS} \ll 1)$$

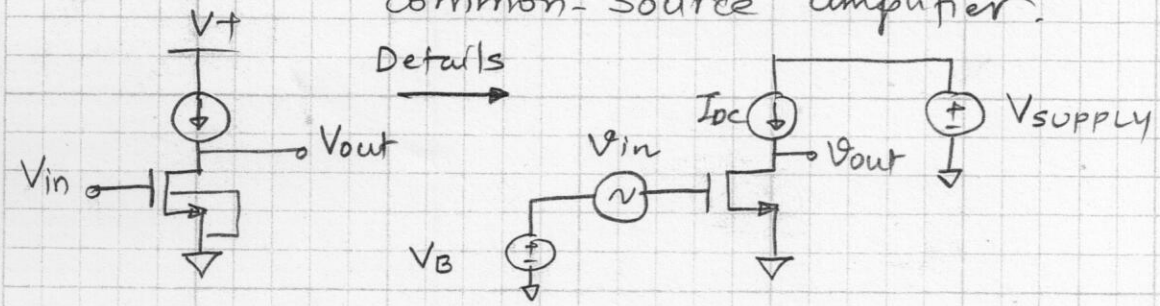
$$r_{ds} = \frac{1}{g_{ds}} = \frac{1}{\lambda I_D}$$

small signal parameter

MOS DC Small Signal Model. (low frequency)



Example - small-signal L.F voltage gain for common-source amplifier.



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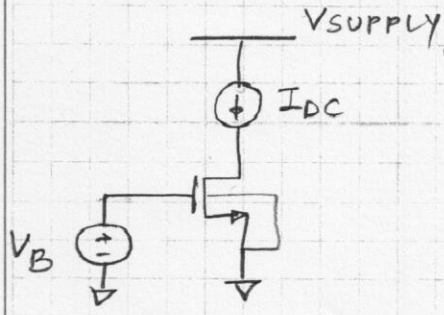
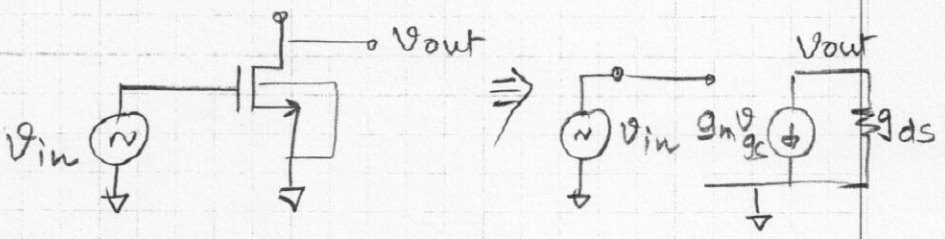
DC circuit



AC circuit



$$v_{out} = -g_m v_{in} \cdot \frac{1}{g_{ds}}$$

open ckt gain

self gain

$$\text{gain} \quad a_v = \frac{v_{out}}{v_{in}} = -\frac{g_m}{g_{ds}}$$

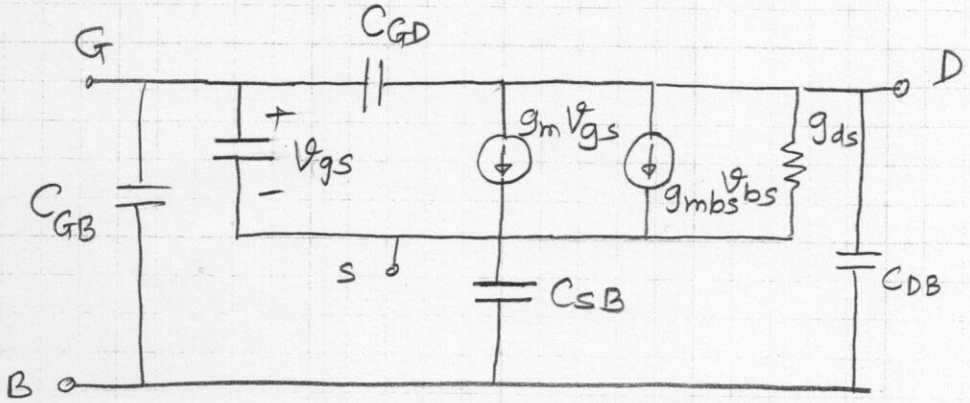
$$a_v = -\frac{g_m}{g_{ds}} = \frac{-\sqrt{2\mu_n C_{ox}(W/L) I_D}}{\lambda I_D} \propto \frac{1}{\sqrt{I_D}}$$

$$= -\frac{g_m}{g_{ds}} = \frac{2 I_D/(V_{GS}-V_{TH})}{\lambda I_D} = \frac{2}{\lambda (V_{GS}-V_T)}$$

insight large channel length → small λ → high gain

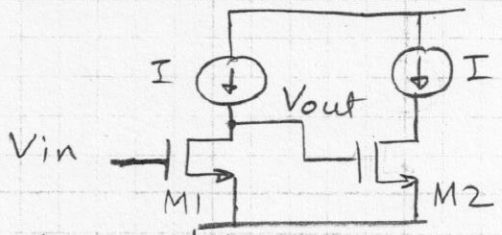
small $(V_{GS}-V_{TH})$ → higher gain

High frequency small-signal Model



Engineer's Computation Pad

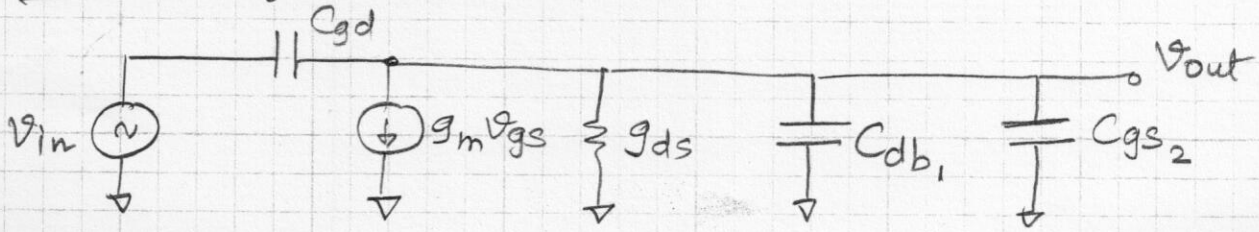
Speed of CMOS



C_{gs_1}, C_{gb_1} – ignore – source driven

g_{mbs}, C_{sb} – ignore. (No backgate effect)

Small Signal model.



KCL @ Vout

$$sC_{gd}(V_{in} - v_{out}) = g_m v_{in} + g_{ds} v_{out} + s(C_{gs} + C_{db}) v_{out}$$

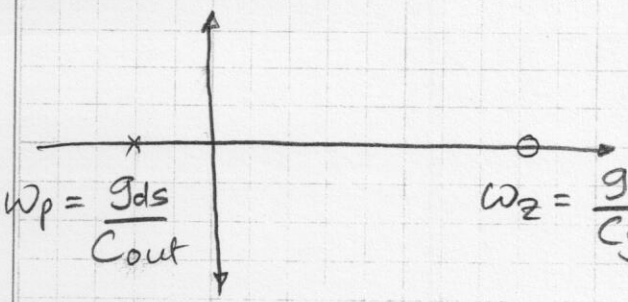
$$-(g_m - sC_{gd}) v_{in} = v_{out}\left[g_{ds} + s(C_{gs} + C_{db} + C_{gd}) \right]$$

$$A_V(s) = \frac{v_{out}}{v_{in}} = -\boxed{\frac{g_m}{g_{ds}}} \frac{\left(1 - s\frac{C_{gd}}{g_m}\right)}{\left(1 + s\frac{(C_{gs} + C_{gd} + C_{db})}{g_{ds}}\right)}$$

← RHP zero

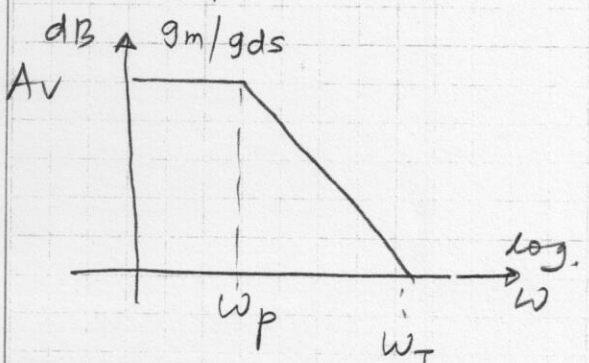
DC gain

$C_{out} = C_{gs} + C_{gd} + C_{db}$ ← LHP pole



Assume $\omega_z >> \omega_p$

& $C_{gs} >> C_{db} + C_{gd}$.



$$A_V(s) = -\frac{g_m}{g_{ds}} \frac{1}{\left(1 + s\frac{C_{gs}}{g_{ds}}\right)}$$

Transition frequency ω_T.

ω_T = gain ; BW product.

$$\omega_T = \frac{g_m}{g_{ds}} \cdot \frac{g_{ds}}{C_{gs}} = \frac{g_m}{C_{gs}} \text{ (rad/s.)}$$

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$$\omega_T = \frac{g_m}{C_{gs}} = \frac{\mu_n C_{ox}(W/L)\cdot(V_{GS}-V_{TH})}{\frac{2}{3} C_{ox}\cdot(W\cdot L)} \qquad V_{dsat}$$

$$= \frac{3}{2}\cdot\frac{\mu_n (V_{GS}-V_{TH})}{L^2}$$

Example: $\mu_n = 350\ cm^2/V/s$

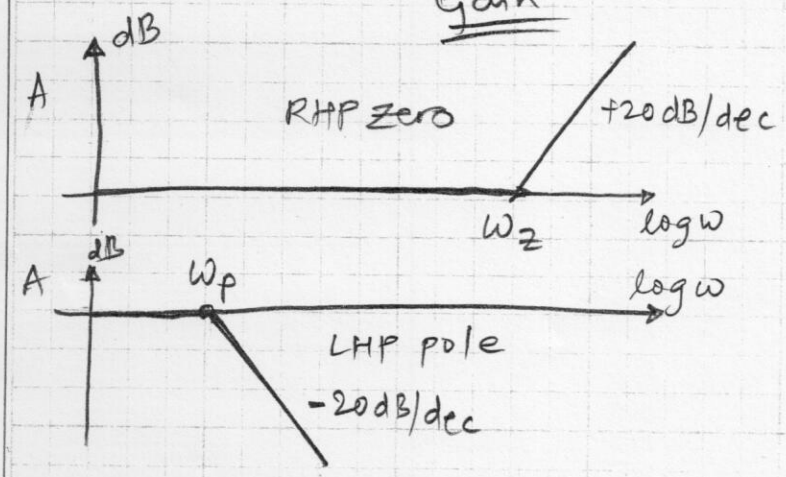
$V_{GS}-V_{TH} = 200\,mV$

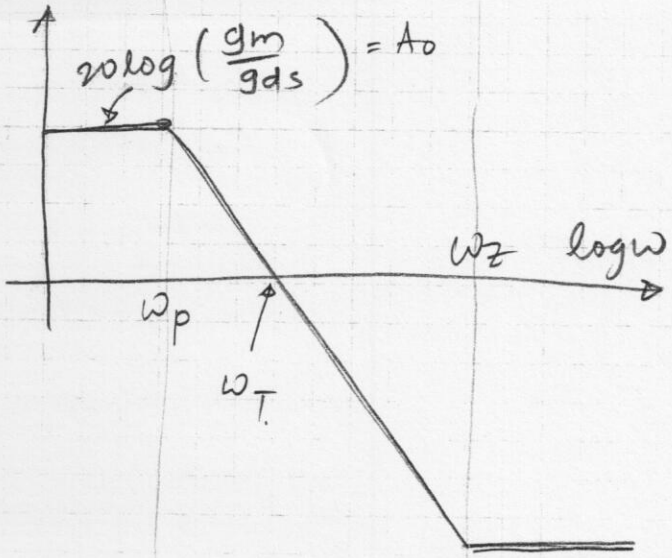
$L = 100nm.$

$$f_T = \frac{3}{2}\cdot\frac{350\times 0.2}{2\times\pi\times(100\times 10^{-7})^2} = 167.1\ GHz.$$

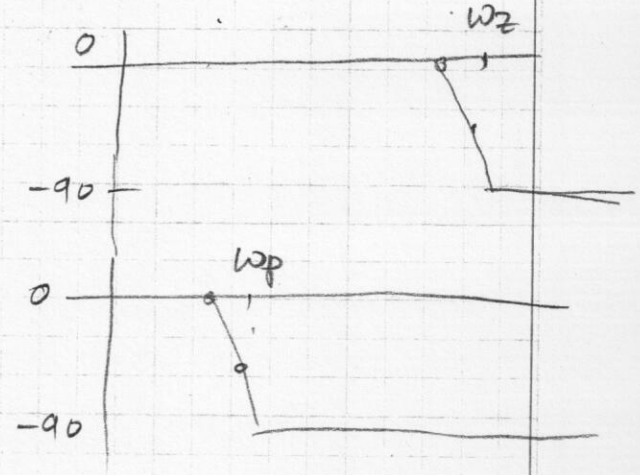
Bode Plot

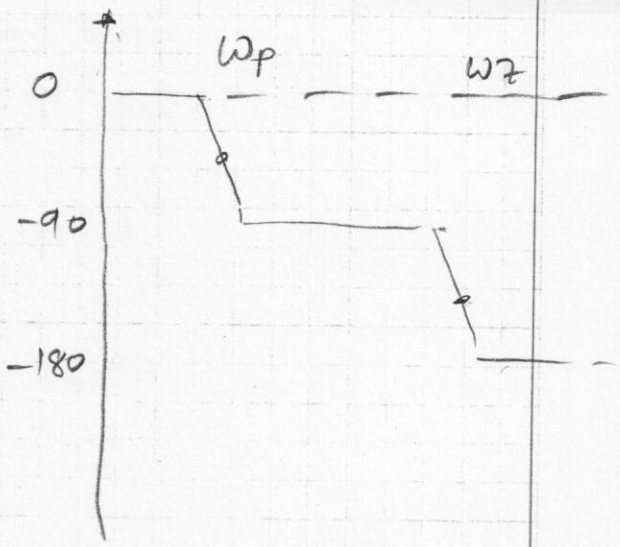
Gain





Phase





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Example values for all transistor parameters

Example process $L_{min} = 0.5\mu m$

	NMOS	PMOS
VTO (V) Threshold voltage	+0.5	−0.6
GAMMA (body Effect coef $V^{-1/2}$)	0.45	0.4
TOX (A)	90	90
UO (mobility $cm^2/V/s$)	350	100
LAMBDA (λ - ch. length modulation Coef V^{-1})	0.1	0.2
PHI ($2\phi_F$) V	0.9	0.8

$$C_{ox} = \frac{\epsilon_{ox}\epsilon_0}{t_{ox}} = \frac{3.97 \times 8.85 \times 10^{-12}\ (F/m)}{(90 \times 10^{-10})\ m} = 3.9 \times 10^{-3}\ F/m^2$$

$$= 3.9\ fF/\mu m^2$$

$$\lambda_n = \frac{0.1\ V^{-1} \times 0.5\mu m}{L_n} = \frac{0.05}{L_n}\ V^{-1} \leftarrow L_n \text{ in } \mu m$$

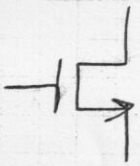
$$\lambda_p = \frac{0.2 \times 0.5}{L_p} = \frac{0.1}{L_p}\ V^{-1} \leftarrow L_p \text{ in } \mu m$$

$$\mu_n C_{ox} = 350\ cm^2/V/s \times 3.9\ fF/\mu m^2$$

$$= 350 \times 10^{-4} \times 3.9 \times \frac{10^{-15}}{10^{-12}}\ A/V^2 = 136.5\ \mu A/V^2$$

$$\mu_p C_{ox} = 39\ \mu A/V^2$$

Example



$$g_m = \sqrt{2 \cdot \mu_n C_{ox} \frac{W}{L} \cdot I_D}$$

$$= \sqrt{2 \times 136.5 \times 10^{-6} \times \frac{10}{0.5} \times 100 \times 10^{-6}}$$

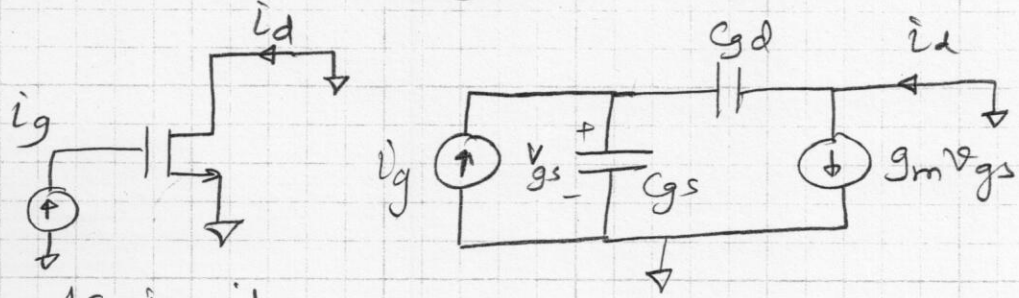
$$= 738\ \frac{\mu A}{V} = 738\ \mu S$$

$$g_{ds} = \lambda_n I_{DS} = 0.1 \times 100 \times 10^{-6} = 10\ \mu S$$

Engineer's Computation Pad

High Frequency Figure of Merit

f_T - Transition Frequency – frequency @ which current gain is unity.



AC circuit

$$i_g = s(C_{gs}+C_{gd})\,v_{gs} \Rightarrow v_{gs} = \frac{i_g}{s(C_{gs}+C_{gd})}$$

$$i_d = g_m v_{gs} = \frac{g_m\, i_g}{s(C_{gs}+C_{gd})}$$ { ignore C_{gd} contribⁿ to o/p current

For f_T (ω_T) $\left|\frac{i_d}{i_g}\right| = \frac{g_m}{\omega_T(C_{gd}+C_{gs})} = 1$

$$\omega_T = \frac{g_m}{(C_{gs}+C_{gd})} \approx \frac{g_m}{C_{gs}}$$ { $C_{gs} \gg C_{gd}$ for long-ch devices

$$f_T = \frac{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})}{2\pi\cdot\frac{2}{3}C_{ox}\,W\cdot L} = \frac{3}{4}\frac{\mu_n (V_{GS}-V_{TH})}{\pi L^2}$$

$f_T \propto (V_{GS}-V_{TH})$ $\quad v_{dsat}$

$f_T \propto \frac{1}{L^2}$ $\quad f_T$ improves with process. $L \downarrow \Rightarrow f_T \uparrow\uparrow$

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_{gs}} = \frac{\sqrt{2\mu_n C_{ox}\frac{W}{L} I_D}}{2\pi\frac{2}{3}C_{ox}\cdot W\cdot L} = \frac{1}{2\pi}\frac{3}{\sqrt{2}}\sqrt{\frac{\mu_n}{C_{ox}L^2}\left(\frac{I_D}{W}\right)}$$

($\frac{I_D}{W}$: current density)

f_T improves with current density

EE618 (Zele)

Body Effect and Sub-threshold Conduction

Body Effect

Consider the simplified NMOS shown in Fig. 1 part (A). A voltage V_{GS} is applied between gate and source whereas a voltage V_{SB} is applied between the source and bulk of the NMOS. For this explanation, we consider that the bulk is a p-well so that we can separately bias it (NMOS in a chip may lie in substrate and substrate of the whole chip will be tied to ground). We consider the following two cases -

CASE 1: $V_{GS} = V_{TH}$ **and** $V_{SB} = 0$ **V**

As shown in Fig. 1 part (B), Due to positive V_{GS} the holes in the channel region move out leaving negatively charged ions behind. The electrons that form the inversion layer comes from the n+(very high concentration) source region. The current in the device will be due to drift of these electrons when a V_{DS} is applied.

CASE 2: $V_{GS} = V_{TH}$ **and** V_{SB} **>0 V**
In this case we are increasing V_{SB} (can be achieved by decreasing the bulk voltage keeping source voltage constant). Due to a net positive voltage on the source as compared to the bulk, some of the electrons present in the channel will be attracted back in the source as shown in of Fig. 1 part (C). Hence to achieve the same charge density as in CASE1 we need a more positive charge on the gate. Therefore we can say that increasing V_{SB} increases threshold voltage.

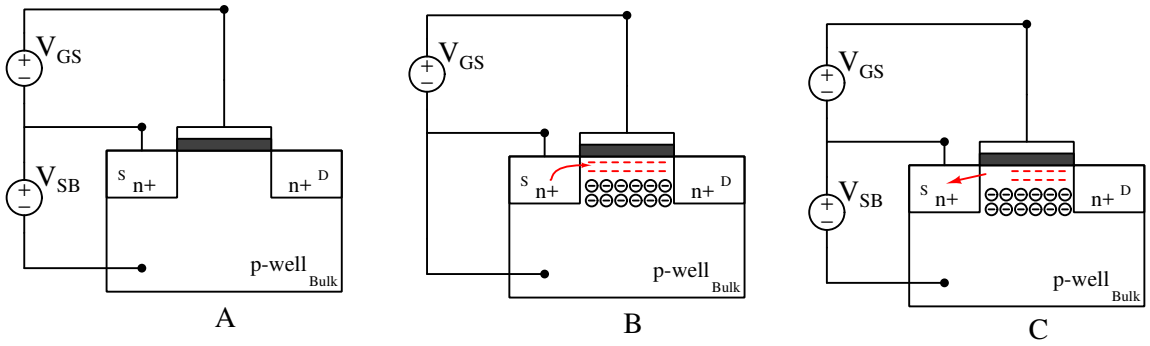


Figure 1: Body effect in MSOFETS

Effect of V_{DS} in Subthreshold Region

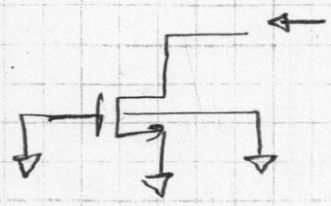
- The region where V_{GS} of the device is less than or close to V_{TH} is known as sub-threshold region.
- Due to diffusion of minority charge carrier electrons, some leakage current may flow in the device even when V_{GS} is less than V_{TH}.
- For a constant V_{DS}, the current equation in subthereshold region is given as

$$\mathrm{I}_{subth} = I_O \times \ exp(\tfrac{V_{GS}}{\zeta V_T}) \times (1 - exp(\tfrac{-V_{DS}}{V_T}))$$

  where ζ is a non-ideality factor greater than 1 and V_T = KT/q
- For $V_{DS} = 0$, the current $I_{subth} = 0$.
- For V_{DS} >$4V_{TH}$ or $5V_{TH}$ the equation reduces to

$$\mathrm{I}_{subth} = I_O \times \ exp(\tfrac{V_{GS}}{\zeta V_T})$$

Small Signal Mos terminal impedances

① 

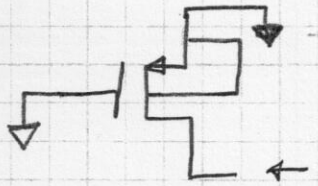
$g = g_{ds}$

$C = C_{gd} + C_{db}$

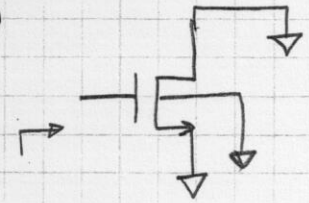
High impedance

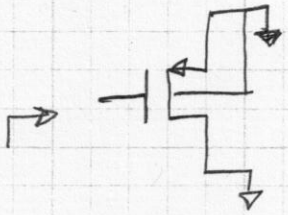
⏚ ← ac ground

DC proper biasing to keep transistor in sat.



Looking into drain

② 

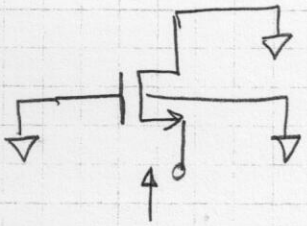


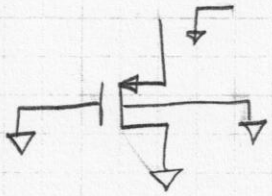
LOOKING into Gate

$g = 0$

$C = C_{gs} + C_{gd}$.

— High Impedance —

③ 



Looking into Source.

$g = g_m + g_{mbs} + g_{ds}$

$C = C_{gs} + C_{sb}$

Low impedance.

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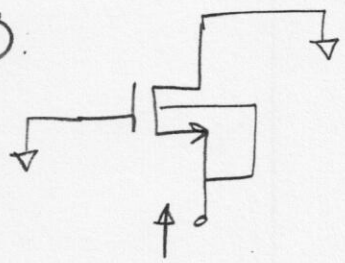
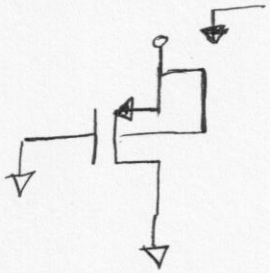
Engineer's Computation Pad

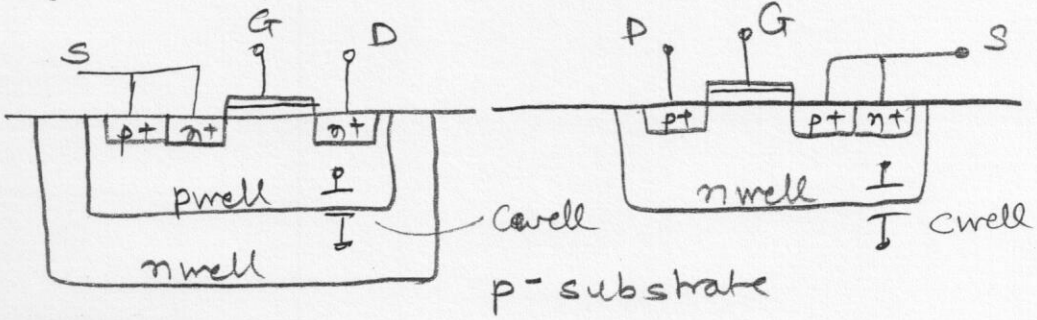
④



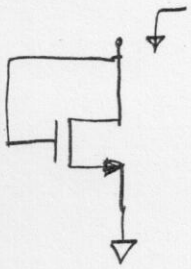


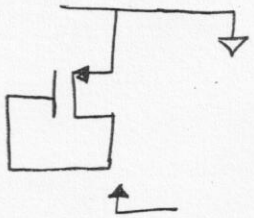
Looking into source (self biased well)

$g = g_m + g_{ds}$ $\quad C = C_{gs} + C_{gb} + C_{db} + C_{well}$



⑤





$g = g_m + g_{ds}$ $\quad C = C_{gs} + C_{db}$

Called <u>diode connected</u> device.

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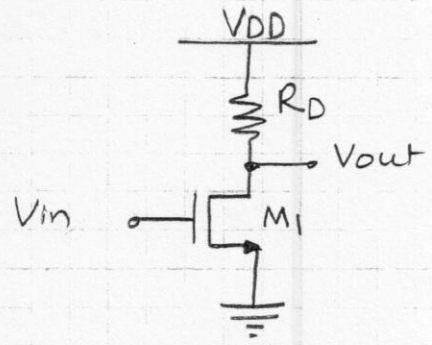
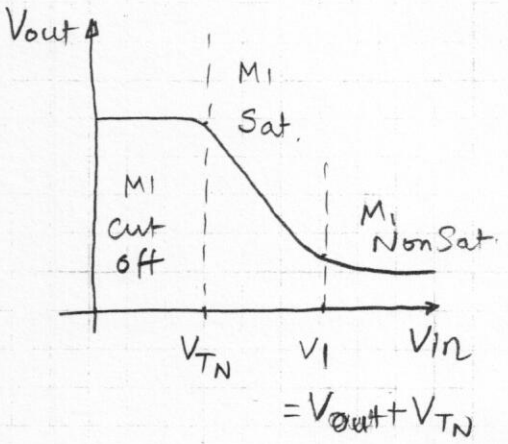
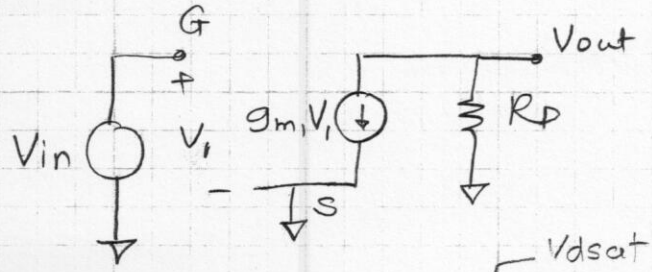
Amplifiers

1. Common-Source amplifier





Small Signal Model in sat. region (ignoring r_o)



$$V_{out} = \underbrace{-g_{m1} R_D}_{A_V \text{ voltage gain}} V_{in}$$

V_{dsat}

$$g_m = \mu_n C_{ox} \left(\frac{W}{L}\right)(V_{GS} - V_{TN}) = \frac{2 I_D}{(V_{GS} - V_{TN})} = \sqrt{2 \mu_n C_{ox} \left(\frac{W}{L}\right) I_D}$$

Small Signal Quantity

I_D, V_{GS} = Bias values

key observation

If i/p signal is large $(V_{GS} - V_{TN})$ & hence g_m & hence gain of the circuit changes a lot.

Gain varies with signal swing.

$\Rightarrow$ Distortion

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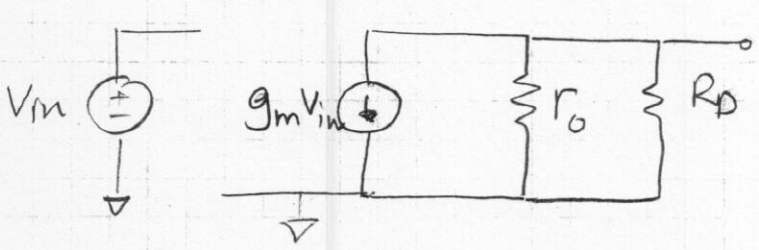
Including Channel length modulation (r_o) effect_



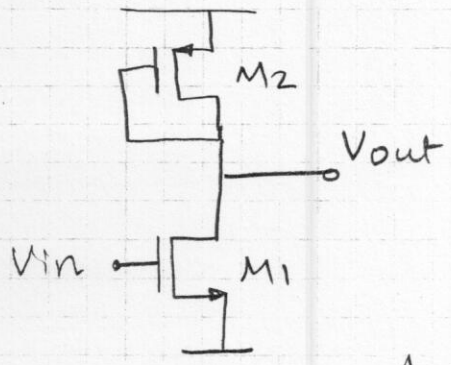
$$A_V = \frac{V_{out}}{V_{in}} = -g_m \frac{r_o R_D}{r_o + R_D}$$

$$A_V = -g_m \cdot (r_o \parallel R_D) = -\frac{g_{m(driver)}}{g_{out\uparrow} + g_{out\downarrow}}$$

g_m ↑ Driver g_m ; $(r_o \parallel R_D)$ Effective output impedance

CS Amp with diode load

①



By inspection

$$A_v = -\frac{g_{m(driver)}}{g_{out\uparrow} + g_{out\downarrow}}$$

$$A_v = -\frac{g_{m1}}{g_{m_2} + g_{ds_2} + g_{ds_1}}$$

$$\approx -\frac{g_{m1}}{g_{m2}} = -\frac{\sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_N I_D}}{\sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_p I_D}}$$

$$\approx -\sqrt{\frac{\mu_n \left(\frac{W}{L}\right)_N}{\mu_p \left(\frac{W}{L}\right)_p}}$$

→ Low voltage gain ~ 2 - 6

→ Low o/p swing $V_{omin} = V_{DSAT1}$ (0.25 V)

$$V_{OMax} = V_{DD} - |V_{GSp}| = V_{DD} - (|V_{Tp}| - |V_{DSAT_2}|)$$

$1.2V - 0.6 - 0.25V = (0.35V)$

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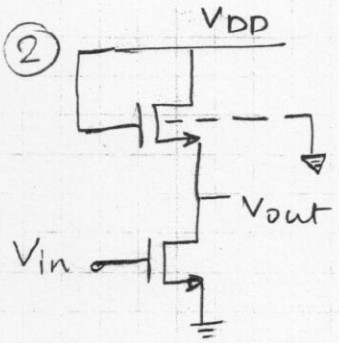
② 

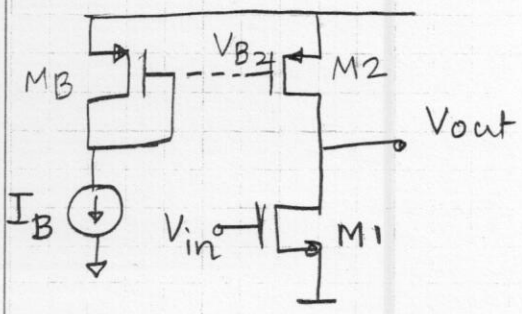
$$A_V = \frac{-g_m(\text{driver})}{g_{out\uparrow} + g_{out\downarrow}}$$

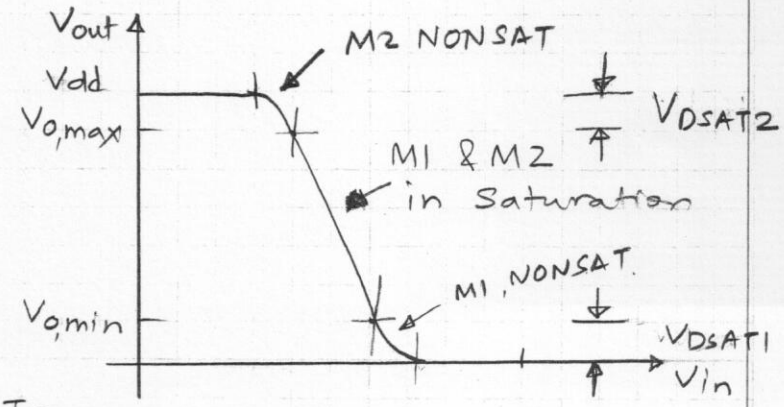
$$A_V = \frac{-g_{m1}}{g_{m2} + g_{mbs2} + \underbrace{g_{ds2} + g_{ds1}}_{\text{ignore}}}$$

$$A_V = -\frac{g_{m1}}{g_{m2} + \underbrace{g_{mbs2}}_{\text{body effect } 0.25\cdot g_{m2}}} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}} \cdot \frac{1}{1+\eta}$$

Low gain & Low swing.

C-S Amplifier with current source load.





$$(W/L)_B = (W/L)_2 \Rightarrow I_1 = I_2 = I_B$$

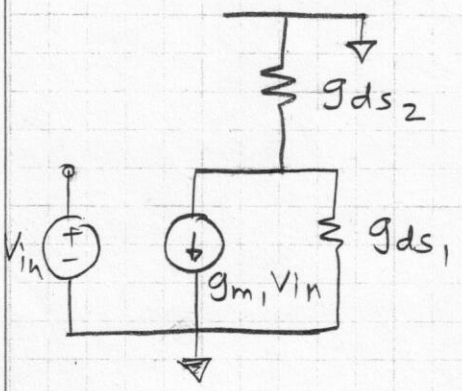
$$V_{B2} = V_{DD} - (|V_{Tp}| + V_{DSAT2})$$

$$V_{B1} = V_{TN} + V_{DSAT1}$$

$$V_{DSAT1} = \sqrt{\frac{2I_B}{\mu_n C_{ox} (W/L)_1}}$$

$$V_{DSAT2} = \sqrt{\frac{2I_B}{\mu_p C_{ox} (W/L)_2}}$$

When Both M1 & M2 are in saturation
— small signal analysis



$$A_V = -\frac{g_{m_1}}{g_{ds_1} + g_{ds_2}}$$

$$= -\frac{2I_B/(V_{GS}-V_T)_N}{\lambda_N I_B + \lambda_p I_B}$$

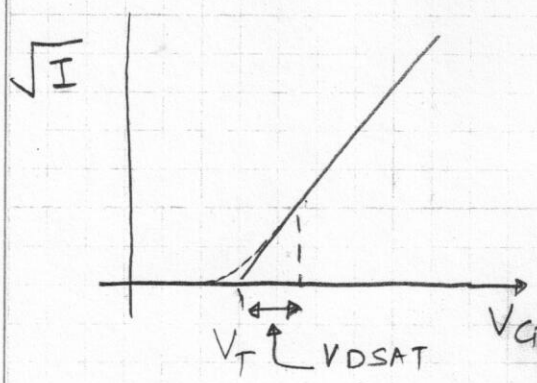
$$= -\frac{2}{V_{DSAT_1}(\lambda_N + \lambda_p)}$$

Insight To increase gain, reduce V_{DSAT_1} & increase channel length to reduce λ_N, λ_p

★ Can you keep on reducing V_{DSAT} & ↑ gain?

$$V_{DSAT_1} = V_{GS}-V_T = \sqrt{\frac{2I}{\mu C_{ox}\left(\frac{W}{L}\right)}}$$

{ for given I, as you ↑ W/L, V_{DSAT} ↓



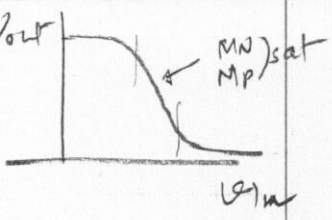
$$I = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_T)^2$$

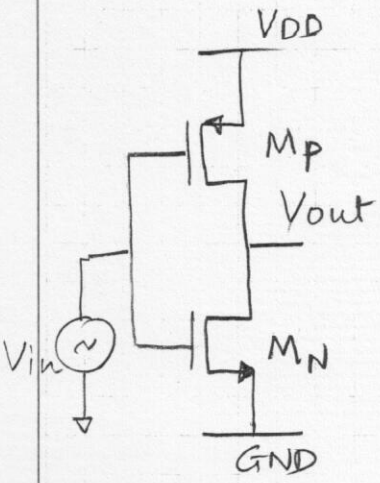
As you keep on reducing $V_{DSAT} = (V_{GS}-V_T)$, V_{GS} very close to V_T

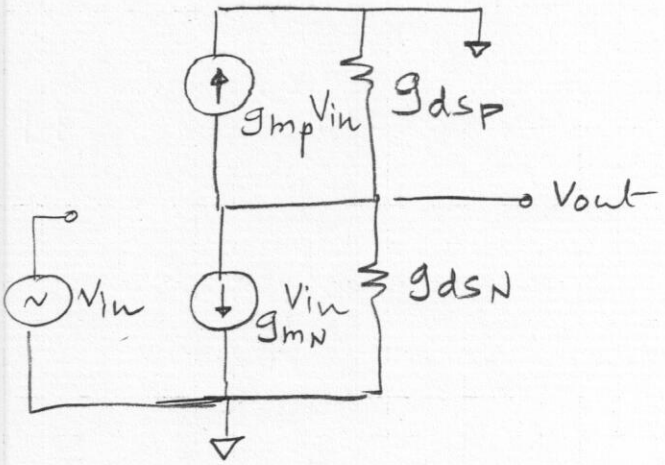
→ sub-threshold operation

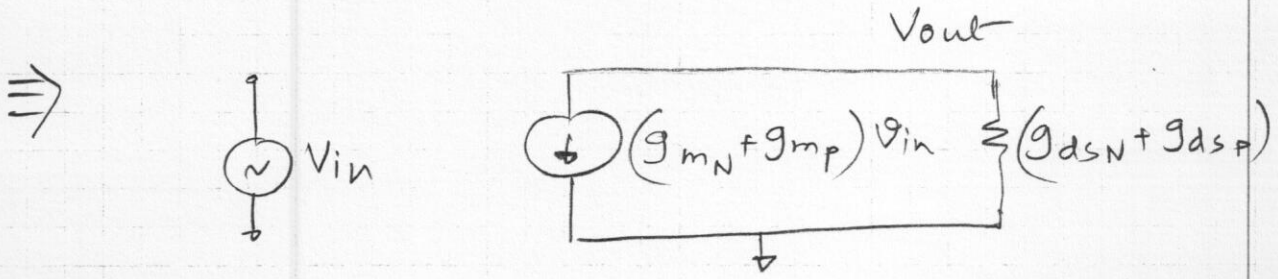
To allow for i/p signal swing & to keep out of sub.thrsh region $V_{DSAT} > 150mV$ (gen. design

CS Amp with Active Load









$$A_v = -\frac{(g_{mN} + g_{mp})}{(g_{dsN} + g_{dsp})}$$

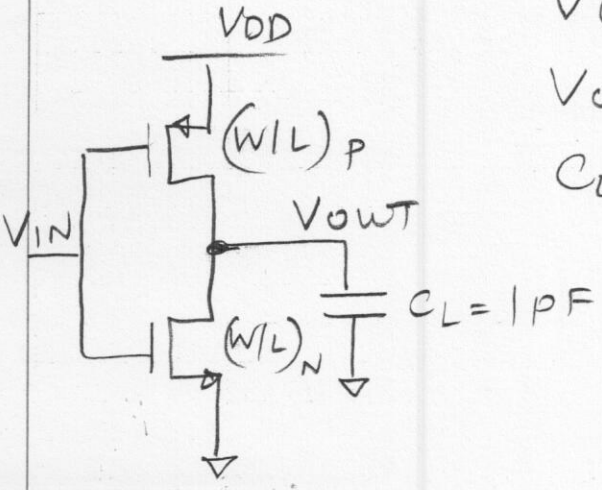
Num. Example:

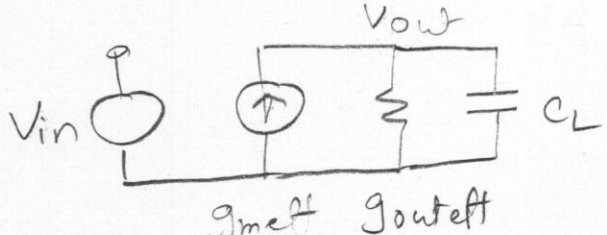
gain $A_v \geq 100$

$V_{out_{min}} = 250mV$

$V_{OUT_{max}} = Vdd - 250mV$

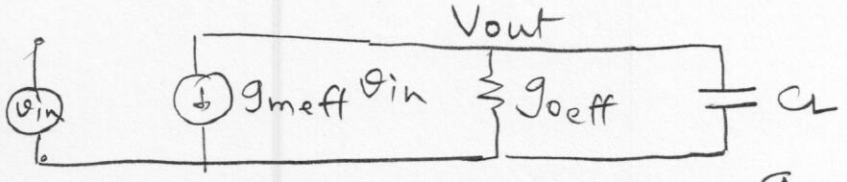
$C_L = 1pF$: $f_u = 100MHz$ unity gain frequency





ignoring transistor internal caps. ($<< 1pF$)

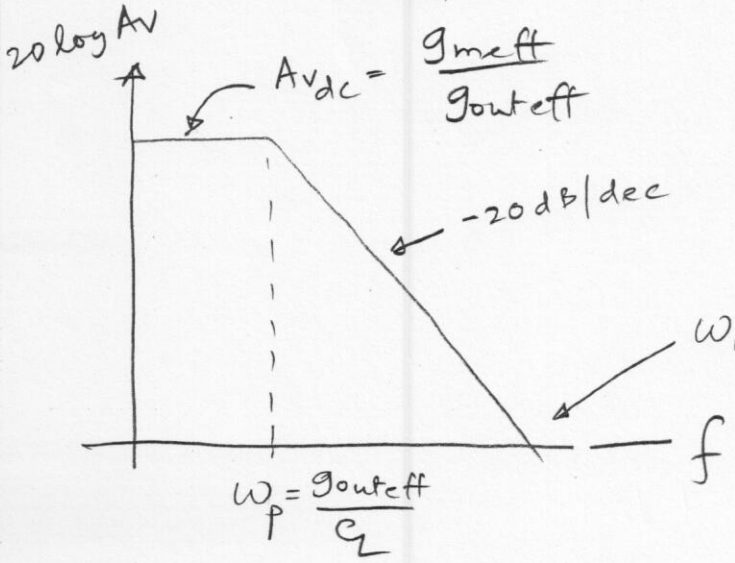
Engineer's Computation Pad



$$v_{out} = \frac{-g_{meff} v_{in}}{(g_{oeff} + sC_L)} = \frac{-\frac{g_{meff}}{g_{outeff}}}{\left(1 + \frac{s}{g_{outeff}/C_L}\right)}$$

DC gain

$\omega_p =$



$|A_v| = 1$

$$f_u = \frac{\omega_u}{2\pi} = \frac{1}{2\pi} \cdot \frac{g_{meff}}{C_L} = 100MHz$$

$$g_{meff} = 2\pi C_L * 100MHz = 2 \times \pi \times 1 \times 10^{-12} \times 10^{8} \text{ S}$$

$$= 628 \ \mu S \quad \text{—— (1)}$$

Symmetric o/p voltage swing $V_{DSATN} = V_{DSATp} = 250m$

$$\sqrt{\frac{2I}{K_N\left(\frac{W}{L}\right)_N}} = \sqrt{\frac{2I}{K_p\left(\frac{W}{L}\right)_p}} \Rightarrow \left(\frac{W}{L}\right)_p = \frac{K_N}{K_p}\left(W/L\right)_N$$

$$K_N = \mu_N C_{ox} = 136.5 \ \mu A/V^2$$

$$K_p = \mu_p C_{ox} = 39 \ \mu A/V^2$$

$$\left(\frac{W}{L}\right)_p = \frac{136.5}{39}\left(\frac{W}{L}\right)_N = 3.5\left(\frac{W}{L}\right)_N. \quad \text{—— (2)}$$

$$g_{m1} = g_{mp} = \frac{2I}{}$$

$g_{meff} = g_{mN} + g_{mp} \Rightarrow g_{mN} = g_{mp} = 314\,\mu S$

$\frac{2I}{V_{DSAT}} = 314\,\mu S \Rightarrow I = \frac{314\,\mu S \times 250\,mV}{2}$

$I = 39.25\,\mu A$ ——— (3)

To maximize voltage gain

$A_v = \frac{g_{mN} + g_{mp}}{g_{dsN} + g_{dsp}} \Rightarrow g_{dsN} = g_{dsp}$

$g_{dsN} = \lambda_N I = \frac{0.05}{L_n\,(\text{in }\mu m)} I$

$g_{dsp} = \lambda_p I = \frac{0.1}{L_p\,(\text{in }\mu m)} I$

$\Rightarrow L_p = 2 L_n$ (Channel Length)

$A_v = \frac{628\,\mu S}{2 \cdot g_{ds}} = 100 \Rightarrow g_{ds_{N,P}} = 3.14\,\mu S.$

$\frac{0.05 \times I}{L_n} = 3.14\,\mu S \Rightarrow L_n = \frac{0.05 \times 39.25\,\mu A}{3.14\,\mu S}$

(L_n in μ)

$L_N = 0.625\,\mu m.$

$L_p = 2 \cdot L_N = 1.25\,\mu m$

0.5 μm Technology → grid 0.25 μm

Round up L values to get on grid & make sure $A_v > 100$

$L_N = 0.75\,\mu m \quad L_p = 1.5\,\mu m$

Engineer's Computation Pad

$$V_{DSAT_N} = \sqrt{\frac{2I}{K_N (W/L)_N}} < 0.25\,V$$

$$\left(\frac{W}{L}\right)_N > \frac{2I}{K_N \cdot (0.25)^2} = \frac{2 \times 39.25\,\mu A}{136.5\,\mu A/V^2 \times (0.25)^2 V^2}$$

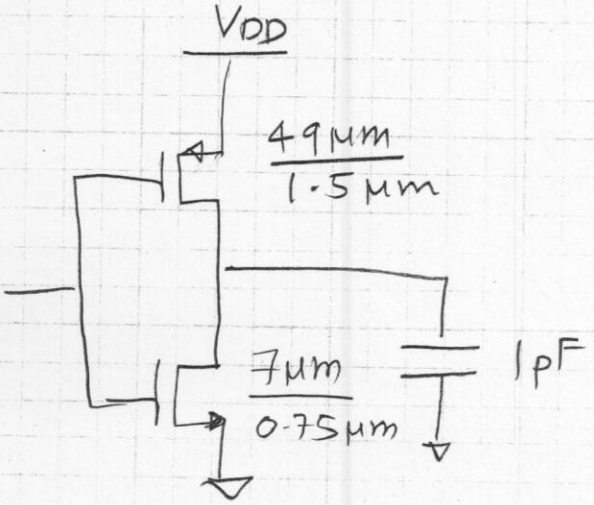
$$= 9.2$$

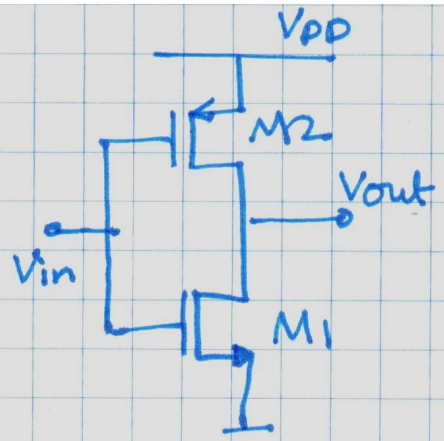
$$W_N > 9.2 \times 0.75\,\mu m = 6.9\,\mu m$$

$$W_N = 7\,\mu m$$

$$\left(\frac{W}{L}\right)_p = 3.5 \times \left(\frac{W}{L}\right)_N \Rightarrow W_p = 3.5 \times \frac{7}{0.75} \times 1.5$$

$$W_p = 49\,\mu m$$





Represents AC behavior of circuit.

DC circuit – different

$V_{Dsat_N} = V_{Dsat_P} = 0.25\,V$

$\therefore V_{GS_N} = V_{T_N} + V_{Dsat_n} = 0.5 + 0.25$

$= 0.75\,V$

$V_{SG_P} = |V_{T_P}| + V_{Dsat_P} = 0.6 + 0.25$

$= 0.85\,V$

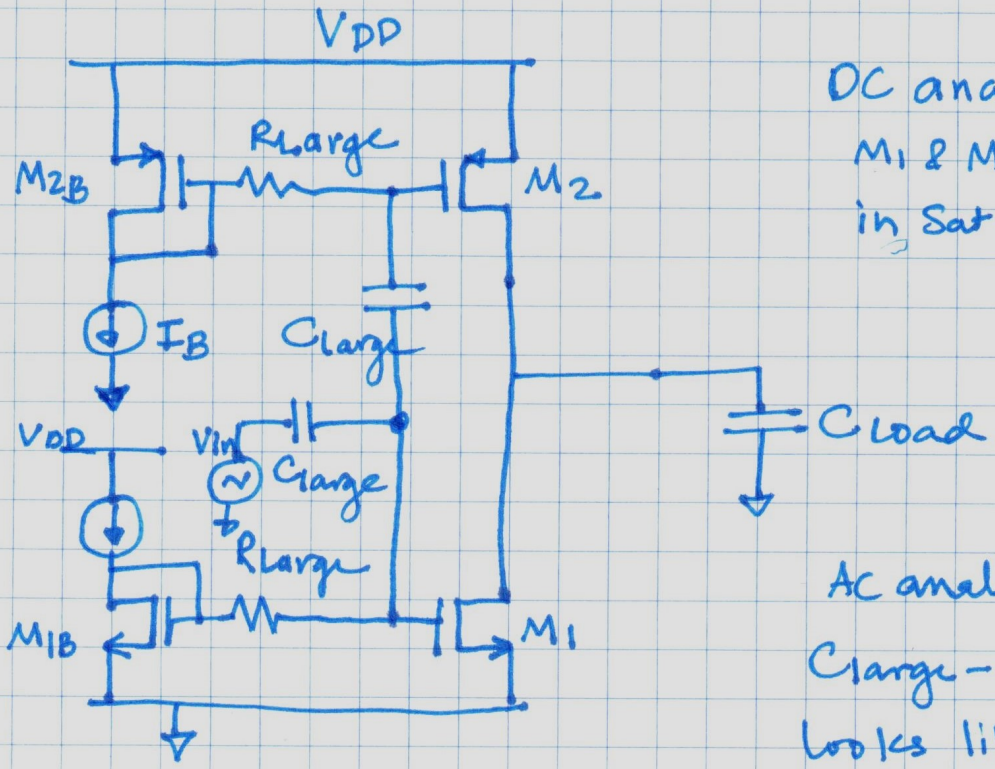
DC condition

$V_{DD} = V_{SG_P} + V_{GS_N}$

$= 0.85 + 0.75 = 1.6\,V$

Satisfied only for $V_{DD} = 1.6\,V$.

Actual circuit implementation DC & AC

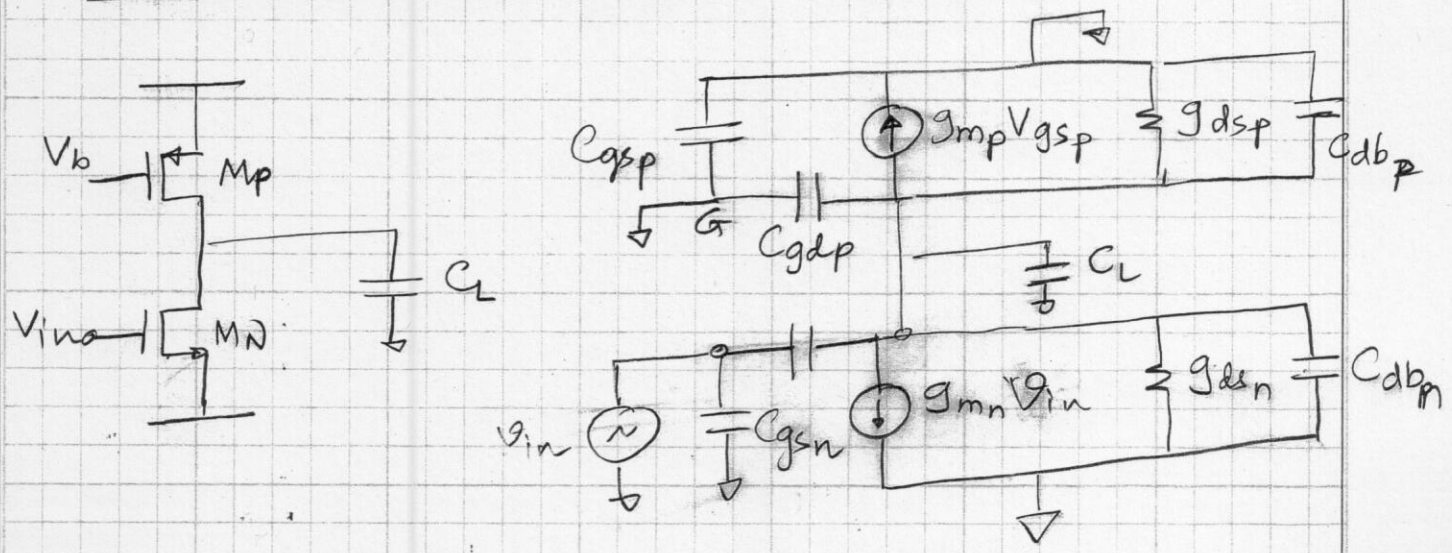


DC analysis
M1 & M2 are biased in Sat with I_B

AC analysis
CLarge – short
looks like inverter amplifier.

C-S Amplifier with Current source load.

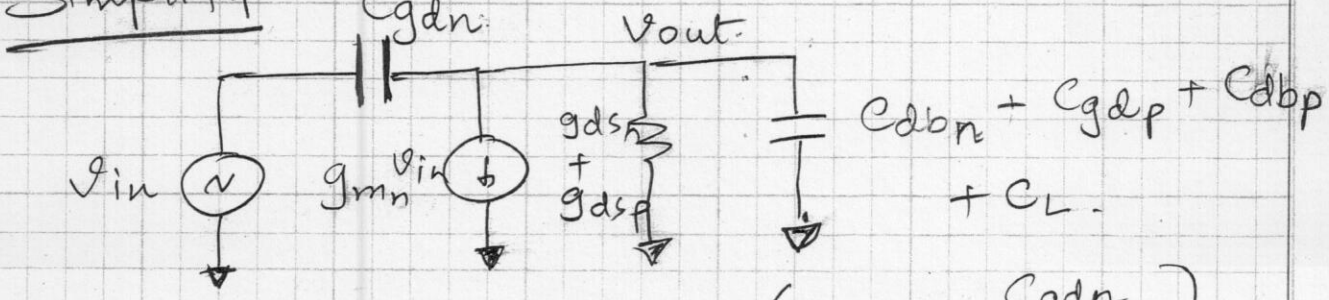
FREQUENCY RESPONSE – Detailed



Neglect g_{mp}, g_{mbsn}, g_{mbsp} – No sig.

Neglect C_{gsn}, C_{gsp} – driven by v_{in}

Simplify



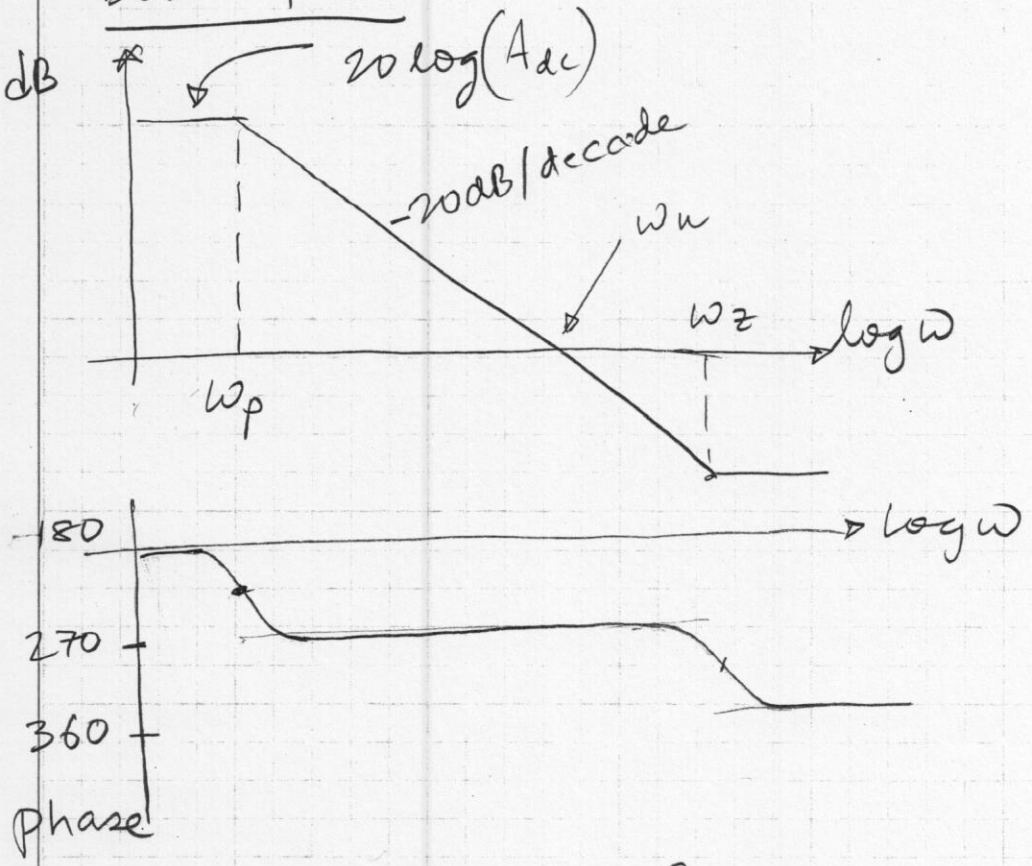
$$A_v = \frac{v_{out}}{v_{in}} = -\frac{g_{mn}}{g_{dsn}+g_{dsp}} \cdot \frac{\left(1 - s\frac{C_{gdn}}{g_{mn}}\right)}{\left(1 + s\left(\frac{C_{gdn}+C_{gdp}+C_{dbn}+C_{dbp}+C_{gdp}+C_L}{g_{dsn}+g_{dsp}}\right)\right)}$$

RHP zero $\quad \omega_z = +\frac{g_{mn}}{C_{gdn}}$

LHP pole $\quad \omega_p = -\frac{g_{out}}{C_{out}} = -\frac{g_{dsn}+g_{dsp}}{C_{gdn}+C_{gdp}+C_{dbn}+C_{dbp}+C_L}$

Engineer's Computation Pad

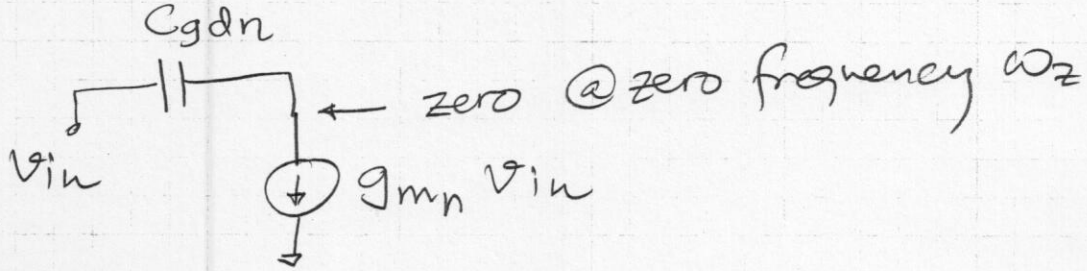
Bode Plots



In Closed-loop feedback system (Study Later)

RHP zero

- keeps gain high @ high freq.
- phase shift degrades @ high freq.



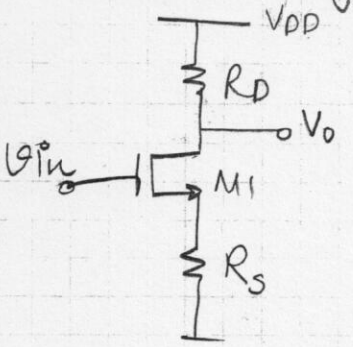
$$s_z C_{gdn} \cdot V_{in} = g_{mn} V_{in}$$

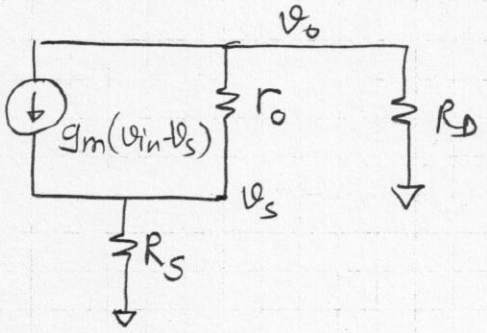
$$s_z = \frac{g_{mn}}{C_{gdn}} \leftarrow \text{Real \& +ve RHP.}$$

Quick way to analyse.

cap across inverting stage → RHP zero
cap across non inverting stage

Source degeneration





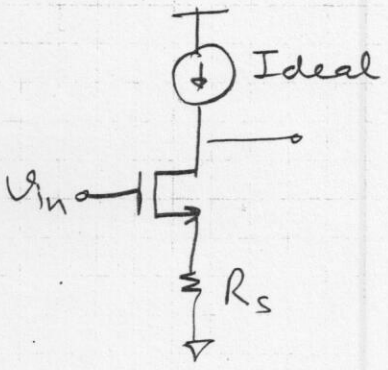
$$g_m(v_{in}-v_s)+\frac{v_o-v_s}{r_o}=\frac{v_s}{R_s} \quad \Big\| \quad \text{Also} \quad \frac{v_s}{R_s}=-\frac{v_o}{R_D} \Rightarrow v_s=-\frac{R_s}{R_D}v_o$$

$$g_m v_{in}+\left[g_m+\frac{1}{r_o}+\frac{1}{R_s}\right]v_s+\frac{v_o}{r_o}=0$$

$$g_m v_{in}+\left(g_m+\frac{1}{r_o}+\frac{1}{R_s}\right)\frac{R_s}{R_D}v_o+\frac{v_o}{r_o}=0$$

$$g_m r_o R_D v_{in}+\left[\left(g_m r_o+1+\frac{r_o}{R_s}\right)R_s+R_D\right]v_o=0$$

$$\boxed{\frac{v_{out}}{v_{in}}=\frac{-g_m r_o R_D}{R_D+r_o+R_s(g_m r_o+1)}}$$



$$\frac{v_{out}}{v_{in}}=-g_m r_o \quad \Big\{ R_D=\infty.$$

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Theorem

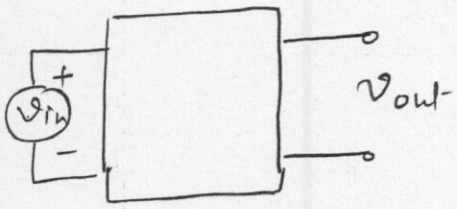
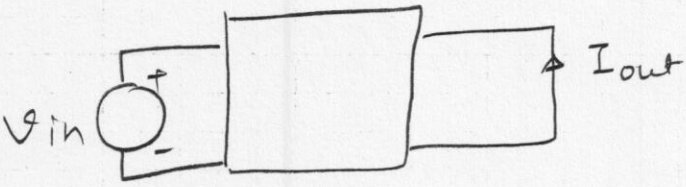


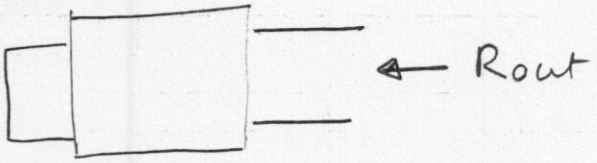
Figure out Voltage gain $\frac{v_{out}}{v_{in}}$

① Short ckt Gm.



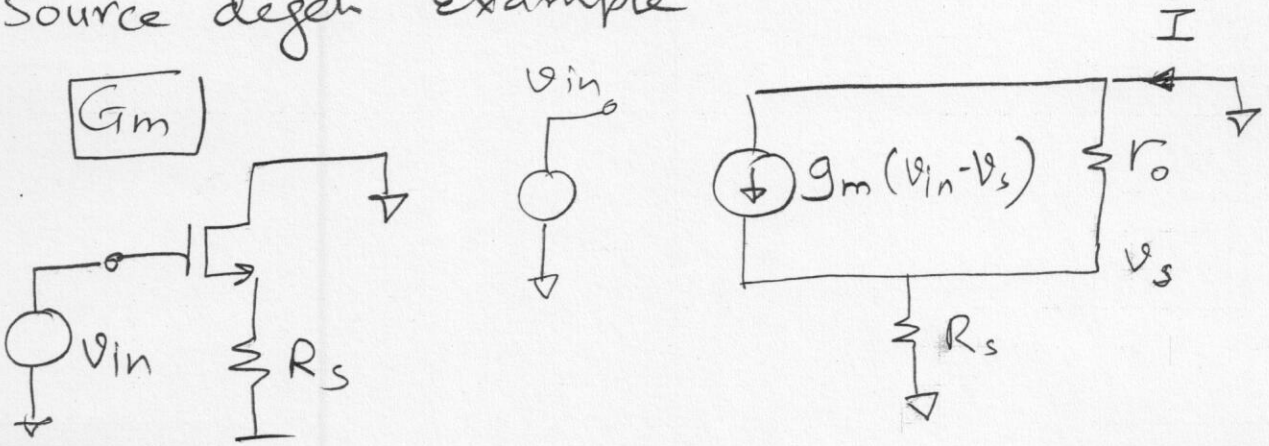
$$G_m = \frac{I_{out}}{v_{in}}$$

② Rout calculation



Voltage Gain $\frac{v_{out}}{v_{in}} = -G_m R_{out}$

Source degen Example



$$g_m(v_{in} - v_s) - \frac{v_s}{r_o} - \frac{v_s}{R_s} = 0$$

$$g_m v_{in} = \left(g_m + \frac{1}{r_o} + \frac{1}{R_s}\right) v_s$$

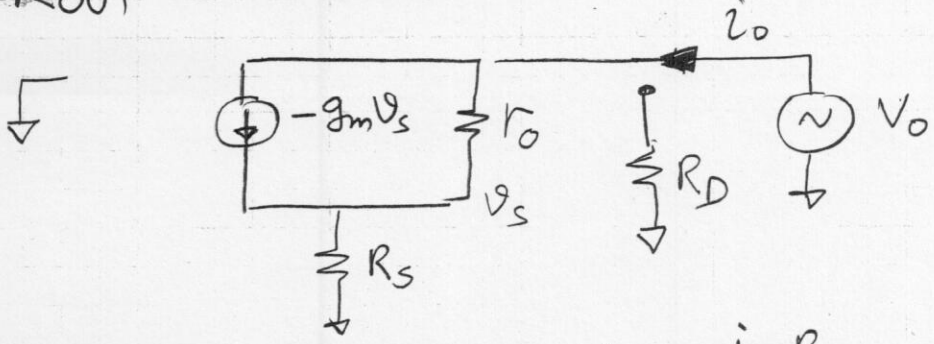
$$I = \frac{v_s}{R_s} = \frac{g_m v_{in}}{R_s\left(g_m + \frac{1}{r_o} + \frac{1}{R_s}\right)}$$

$$G_m = \frac{I}{v_{in}} = \frac{g_m}{g_m R_s + 1 + \frac{R_s}{r_o}}$$

$\Rightarrow$ if r_o is large $\quad \boxed{G_m \approx \frac{g_m}{g_m R_s + 1}}$

$$\boxed{G_m = \frac{g_m r_o}{(g_m r_o + 1) R_s + r_o}}$$

R_{OUT} Calculation



① W/o R_D.

$$v_s = i_o R_s$$

$$g_m v_s + i_o = \frac{v_o - v_s}{r_o}$$

$$\left(g_m i_o R_s + i_o\right) r_o = v_o - i_o R_s$$

$$\frac{v_o}{i_o} = \left[(1 + g_m r_o) R_s + r_o\right]$$

$$\approx g_m r_o R_s + r_o$$

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including $\| R_D$

$$R_{out} = \frac{[(1 + g_m r_o) R_s + r_o] R_D}{R_D + r_o + (1 + g_m r_o) R_s}$$

$$\frac{V_{out}}{V_{in}} = -G_m R_{out}$$

$$= -\frac{g_m r_o}{(g_m r_o + 1) R_s + r_o} \times \frac{[(g_m r_o + 1) R_s + r_o] R_D}{R_D + r_o + (1 + g_m r_o) R_s}$$

$$= -\frac{g_m r_o R_D}{R_D + r_o + (1 + g_m r_o) R_s} \leftarrow$$

Same as what we directly derived !!!

If we ignore r_o

$$G_m = \frac{g_m}{1 + g_m R_s} \quad ; \quad R_{out} = R_D$$

$$\frac{V_{out}}{V_{in}} = -\frac{g_m R_D}{1 + g_m R_s}$$

} (Quick Calculation)

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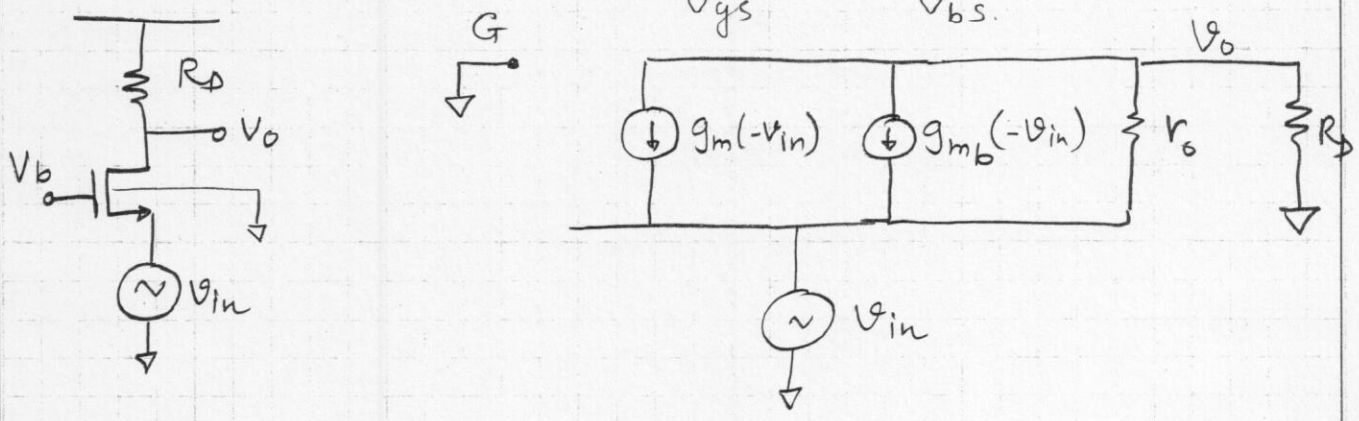
Common Gate amplifier



$$\frac{v_o}{R_D} = g_m v_{in} + g_{mb} v_{in} + \frac{v_{in} - v_o}{r_o}$$

$$\frac{v_o}{}\left(\frac{1}{R_D} + \frac{1}{r_o}\right) = (g_m + g_{mb}) v_{in} + \frac{v_{in}}{r_o}$$

$$\frac{v_o}{v_{in}} = \frac{\left((g_m + g_{mb}) r_o + 1\right)}{(r_o + R_D)} R_D$$

If we ignore body effect

$$\frac{v_o}{v_{in}} = \frac{g_m r_o + 1}{(r_o + R_D)} R_D \longrightarrow \text{✡}$$

$$Z_{in} = \frac{v_{in}}{I_{in}} = \frac{v_{in}}{V_o / R_D} = \frac{R_D \cdot (r_o + R_D)}{(g_m r_o + 1) R_D}$$

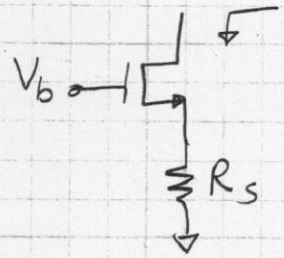
$$Z_{in} = \frac{r_o + R_D}{(g_m r_o + 1)} \simeq \frac{r_o + R_D}{g_m r_o}$$

Drain impedance div by $(g_m r_o)$ ↓

ONLY WHEN $R_D \ll r_o$

$Z_{in} \cong$ ro/(gm ro)=1/gm (low impedance)

In case of source degeneration



$$R_{out} \cong (g_m r_o) R_s + r_o$$

R_{out} ↑ by $(g_m r_o)$

Cascode from Vacuum tubes
1939 - Frederick HUNT
Cascode of two triodes instead of pentode
Iguitar amp

Cascode CS Amplifier

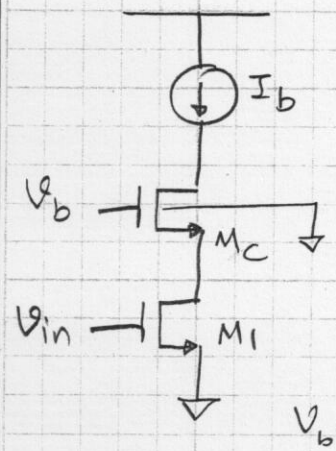
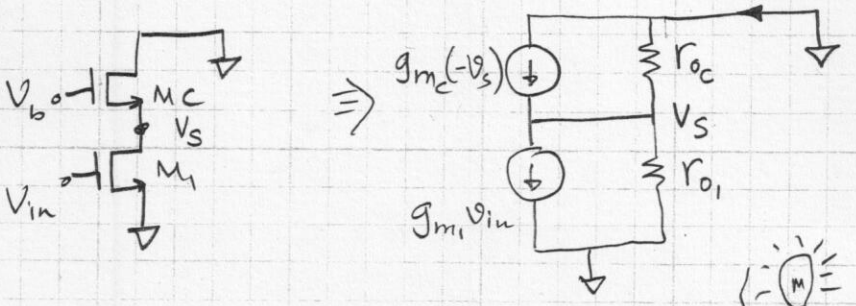


Figure out Gm & Rout

$$A_v = -G_m R_{out}$$

Gm calculation



Use g_{ds} & r_o interchan for convenien

$$g_{m_1} v_{in} + \frac{v_s}{r_{o_1}} + g_{m_c} v_s + \frac{v_s}{r_{o_c}} = 0$$

$$g_{m_1} v_{in} + v_s \left(\frac{1}{r_{o_1}} + \frac{1}{r_{o_c}} + g_{m_c} \right) = 0$$

g_{ds_1} g_{ds_c}

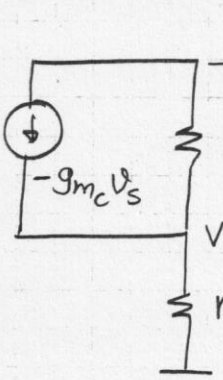
$$v_s = \frac{-g_{m_1} v_{in}}{(g_{ds_1} + g_{ds_c} + g_{m_c})}$$

$$i_{out} = g_{m_1} v_{in} + v_s g_{ds_1} = g_{m_1} v_{in} - \frac{g_{m_1} v_{in} g_{ds_1}}{(g_{ds_1} + g_{ds_c} + g_{m_c})}$$

$$\frac{i_{out}}{v_{in}} = \frac{g_{m_1}\left(g_{ds_1} + g_{ds_c} + g_{m_c} - g_{ds_1}\right)}{\left(g_{ds_1} + g_{ds_c} + g_{m_c}\right)}$$

$$\boxed{G_m \approx g_{m_1}}$$

Rout Calculation



$$v_s = i_o r_{o_1}$$

$$i_o = -g_{m_c} v_s + \frac{(v_o - v_s)}{r_{o_c}}$$

$$i_o = -g_{m_c} i_o r_{o_1} + \frac{(v_o - i_o r_{o_1})}{r_{o_c}}$$

$$i_o r_{o_c} = -g_{m_c} i_o r_{o_1} r_{o_c} + v_o - i_o r_{o_1}$$

$$R_{out} = \frac{v_o}{i_o} = \underbrace{\left(g_{m_c} r_{o_c} r_{o_1}\right)}_{\text{large}} + \underbrace{r_{o_1} + r_{o_c}}_{\text{small}}$$

$$R_{out} \approx \left(g_{m_c} r_{o_c}\right) r_{o_1}$$

Cascode self gain multiplier effect

$$\boxed{A_v = \left(g_{m_1} r_{o_1}\right)\left(g_{m_c} r_{o_c}\right) \approx \left(g_m r_o\right)^2}$$

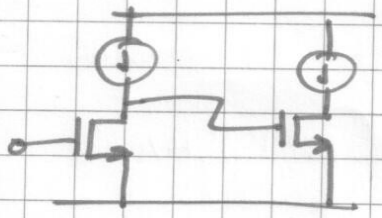
Benefits of cascoding

- (+) Rout → self gain of cascode multiplication
  - can be used for high o/p impedance current source
- (+) gain ↑ squared
- (-ve) Headroom Reduced to keep two transistors in saturation

$$V_{out_{min}} = V_{dsat_1} + V_{dsat_c}$$

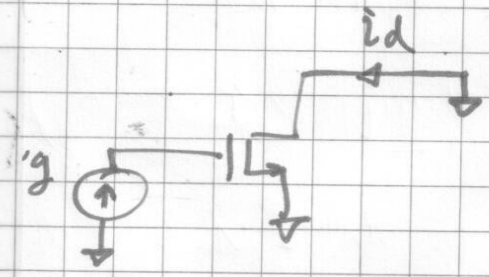
f_T discussion

Transition frequency —



voltage gain = 1

$$\omega_T = \frac{g_m}{C_{gs}}$$



Current gain = 1

$$\omega_T = \frac{g_m}{C_{gs}}$$

Give an idea of Raw speed capability of transistor

Why Transit frequency ?

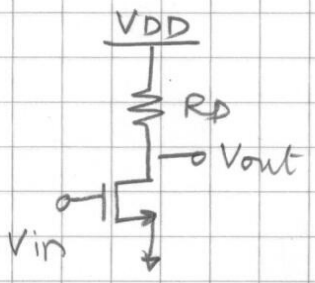
$$\omega_T f_T = \frac{g_m}{C_{gs}} = \frac{\mu_n C_{ox} \frac{W}{L}(V_{GS}-V_{TH})}{\frac{2}{3} C_{ox} W \cdot L} = \frac{\left[\frac{3}{2}(V_{GS}-V_{TH})\right]\mu_n}{L}$$

$$= \frac{\mu_n [E_{channel}]}{L} = \frac{v}{L} = \frac{1}{\tau_T}$$

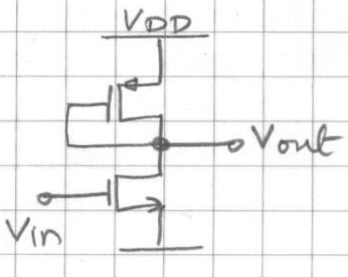
τ_T : Transit Time from source to drain

$f_T \Rightarrow$ gives an idea of intrinsic delay of device.

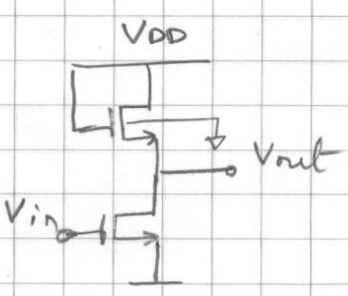
Recap f_T discussion. — Why Transit frequency



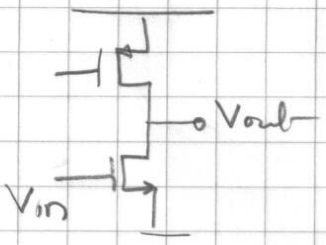
$$\frac{V_{out}}{V_{in}} \cong -g_m (r_o \| R_D)$$



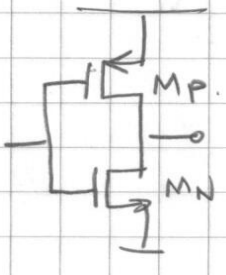
$$\frac{V_{out}}{V_{in}} \cong -\frac{g_{m_1}}{g_{m_2}}$$



$$\frac{V_{out}}{V_{in}} = \frac{-g_{m_1}}{g_{m_2} + g_{mbs_2}}$$

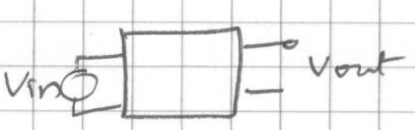


$$\frac{V_{out}}{V_{in}} = -g_{m_1} (r_{o_1} \| r_{o_2})$$



$$\frac{V_{out}}{V_{in}} = -\frac{(g_{mN} + g_{mP})}{(g_{dsN} + g_{dsP})}$$

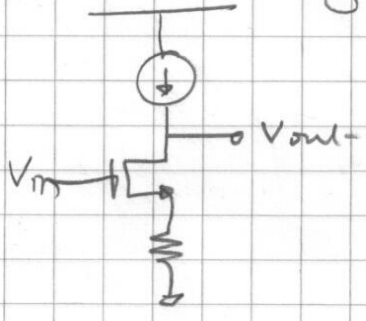
XF Theorem



Short Ckt G_m & R_{out}

$$\frac{V_{out}}{V_{in}} = -G_m R_{out}$$

Source degeneration

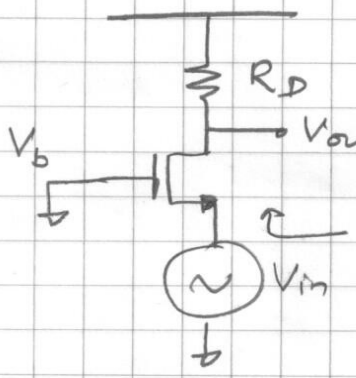


$$G_m \cong \frac{g_m}{1+g_m R_s}$$

$$R_{out} = g_m r_o R_s + r_o$$

$$\frac{V_{out}}{V_{in}} \approx -G_m R_{out} = -g_m r_o$$

Common Gate Amplifier

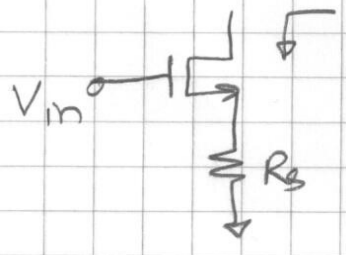


$$\frac{V_{out}}{V_{in}} = \frac{g_m r_o}{(r_o + R_D)} R_D$$

(Body effect ignored)

$$Z_{in} = \frac{r_o + R_D}{(g_m r_o + 1)} \approx \frac{r_o + R_D}{(g_m r_o)} \approx \frac{1}{g_m}$$

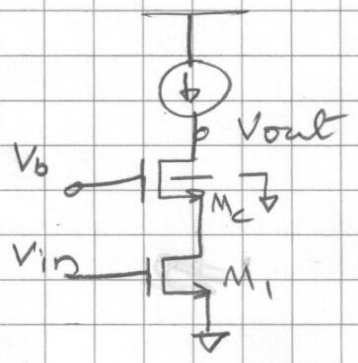
($R_D >>$



$$R_{out} = (g_m r_o) R_s + r_o$$

R_{out} ↑ $(g_m r_o)$ factor

Cascode Common Source Amplifier

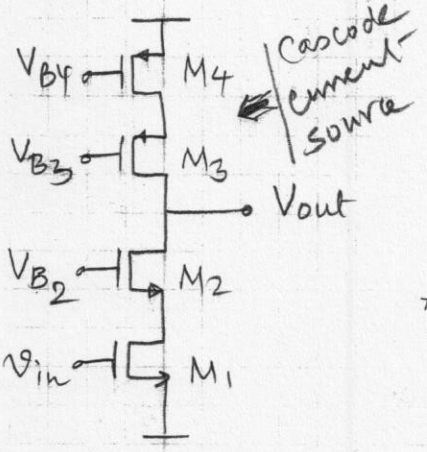


$$A_v = -G_m \cdot R_{out}$$

$$\cong -g_{m_1}\left(g_{m_c} r_{o_c} \cdot r_{o_1}\right)$$

$$\approx -\left(g_{m_1} r_{o_1}\right)\left(g_{m_c} r_{o_c}\right)$$

Cascode Stage with current source



$$G_m = g_{m_1}$$

$$R_{out} = (g_{m_2} r_{o_2}) r_{o_1} \parallel (g_{m_3} r_{o_3}) r_{o_4}$$

Assuming $r_{o_1} = r_{o_2} = r_{o_3} = r_{o_4} = r_o$

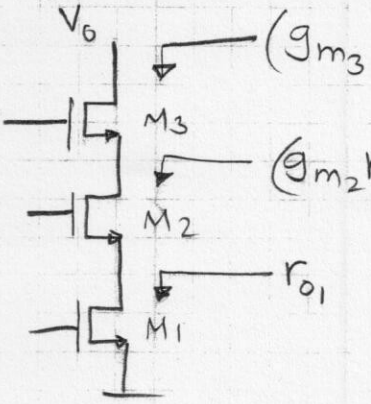
$$g_{m_1} = g_{m_2} = g_{m_3} = g_{m_4} = g_m$$

$$A_v = -\frac{1}{2}(g_m r_o)^2$$

$$V_{out\,min} = V_{dsat_1} + V_{dsat_2}$$

$$V_{out\,max} = V_{dd} - (|V_{dsat_3}| + |V_{dsat_4}|)$$

Tripple Cascode



$(g_{m_3} r_{o_3})(g_{m_2} r_{o_2}) r_{o_1}$ ← Really high o/p impedance

$(g_{m_2} r_{o_2}) r_{o_1}$

r_{o_1}

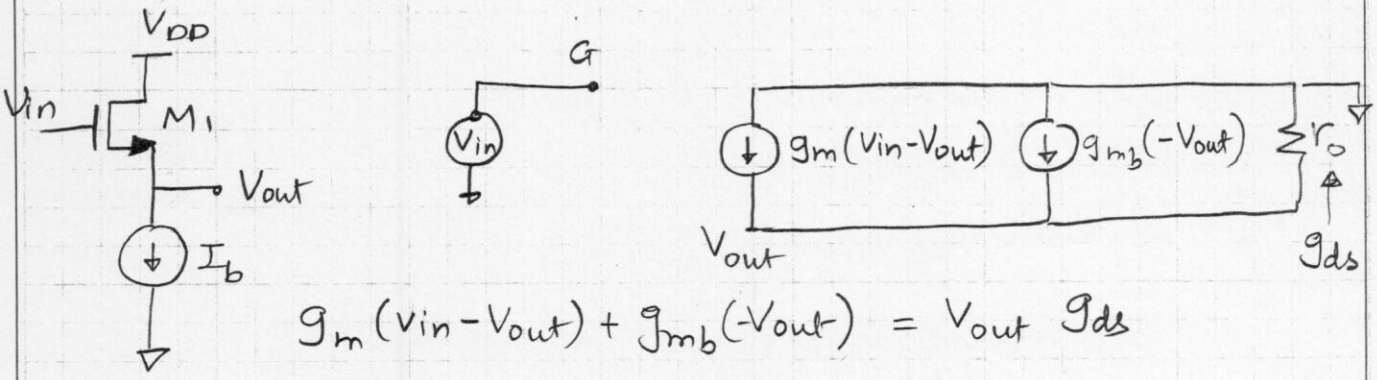
$$V_{o\,min} = V_{dsat_1} + V_{dsat_2} + V_{dsat_3}$$

(with proper biasing.)

Also called

Telescopic Cascode

Common drain Amplifier (Source follower)



$$g_m(V_{in}-V_{out}) + g_{mb}(-V_{out}) = V_{out}\, g_{ds}$$

$$(g_m + g_{mb} + g_{ds})V_{out} = g_m V_{in}$$

$$\frac{V_{out}}{V_{in}} = \frac{g_m}{g_m + g_{mb} + g_{ds}} \approx \frac{g_m}{g_m + g_{mb}} = \frac{1}{1+\eta} \approx 1$$

→ Non-inverting unity gain. amplifier

$r_{in} = \infty$ $\quad r_{out} = \dfrac{1}{g_m + g_{mb} + g_{ds}} \approx \dfrac{1}{g_m}$ Low imp.

→ O/P DC range

$$V_{out} = V_{in} - (V_{T_1} + V_{dsat_1})$$

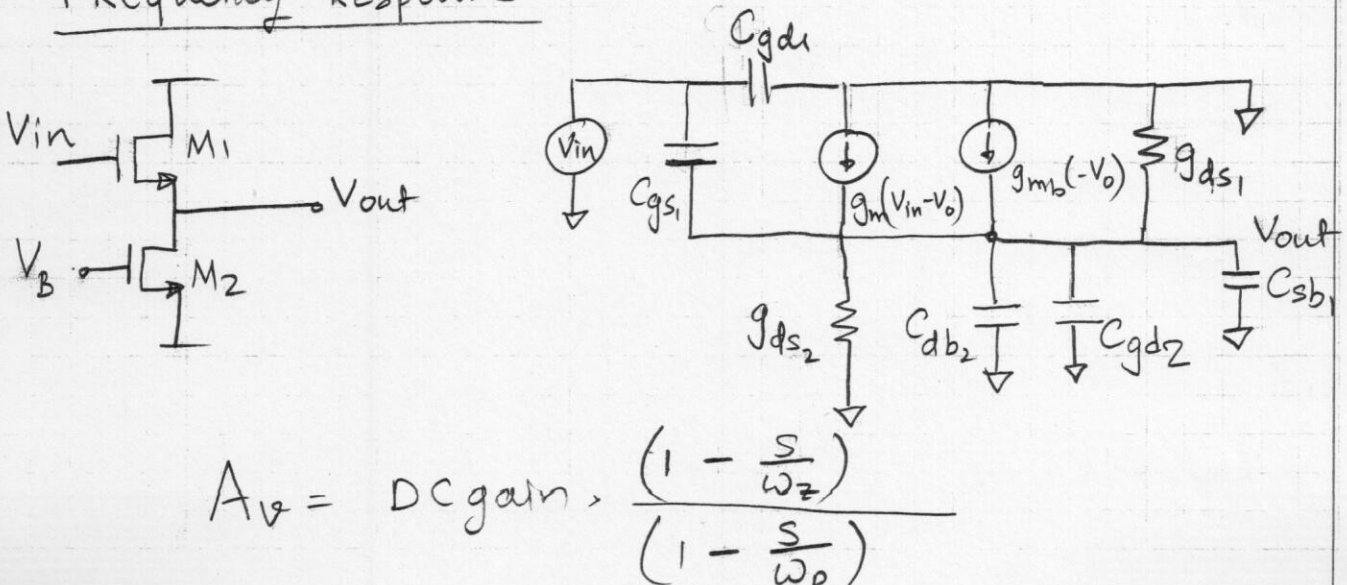
$$V_{out\,max} = V_{DD} - (V_T + V_{dsat})$$

$$V_{in\,max} = V_{DD}$$

$$V_{in\,min} = V_T + V_{dsat} + \underbrace{V_{dsat}}_{cs}$$

→ DC-level shifter & Buffer. (low O/P imp)

Frequency Response



$$A_v = \text{DC gain} \cdot \frac{\left(1 - \frac{s}{\omega_z}\right)}{\left(1 - \frac{s}{\omega_p}\right)}$$

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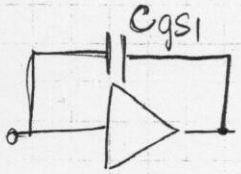
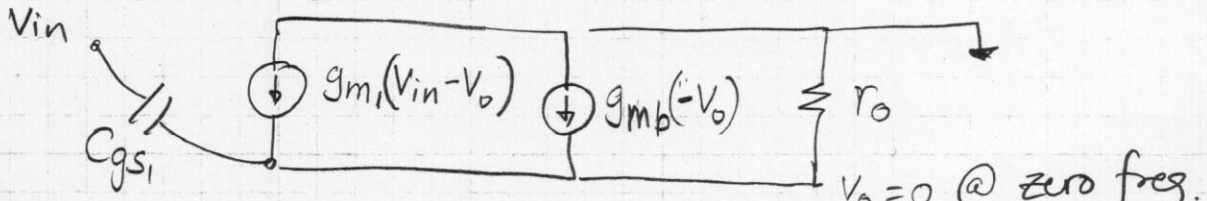
LHP $\omega_p = -\frac{g_{out}}{C_{out}} = -\frac{g_{m_1} + g_{mbs_1} + g_{ds_1} + g_{ds_2}}{C_{gs_1} + C_{sb_1} + C_{db_2} + C_{gd_2}}$



$\Rightarrow$ LHP zero.

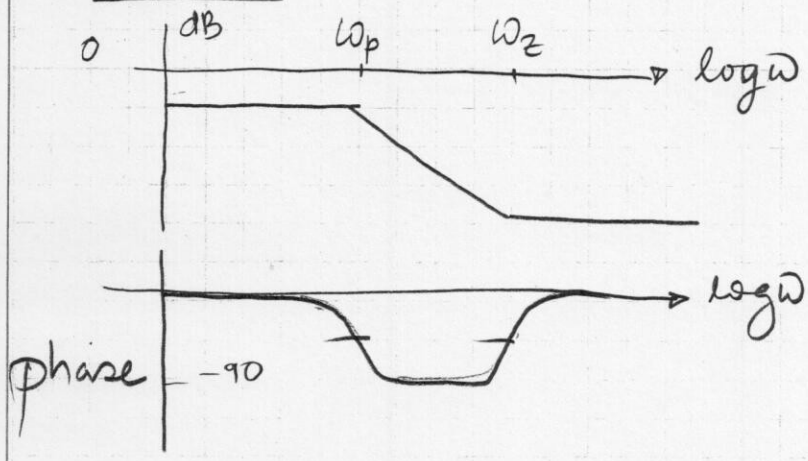


@ Zero frequency ω_z

$$\omega_z C_{gs_1} \cdot v_{in} = -g_{m_1} V_{in} \Rightarrow \boxed{\omega_z = -\frac{g_{m_1}}{C_{gs_1}}}$$

$$A_V = \frac{g_{m_1}}{g_{m_1} + g_{mbs_1} + g_{ds_1} + g_{ds_2}} \cdot \frac{\left(1 + \frac{s}{g_{m_1}/C_{gs_1}}\right)}{\left(1 + \frac{s}{\left(\frac{g_{m_1} + g_{mbs_1} + g_{ds_1} + g_{ds_2}}{C_{gs_1} + C_{sb_1} + C_{db_2} + C_{gd_2}}\right)}\right)}$$

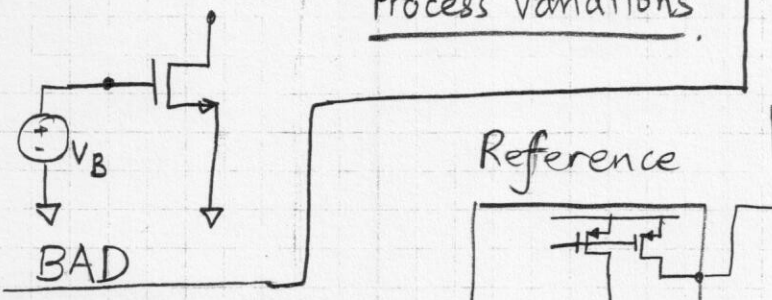
Bode Plot



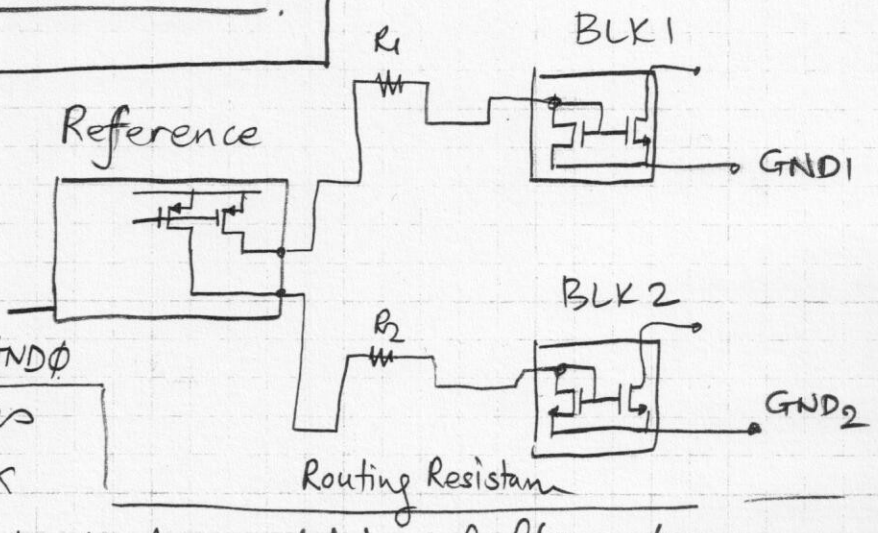
New Topic MOS Current Mirrors / Sources

Novice Biasing

Process variations.



ON CHIP CURRENT DISTRIBUTION



sending voltage as reference XXX

→ Gnd / Vdd potentials could be different

→ transistor properties across the chip change.

Current Sources used for DC biasing,
Active load to get max gain without IR drop.

Specs →
- → Output Resistance
- → voltage compliance (min or max voltage)
- → Accuracy & process independance.
- → DC balance (for mirrors)
- → i/p Resistance (for mirrors)

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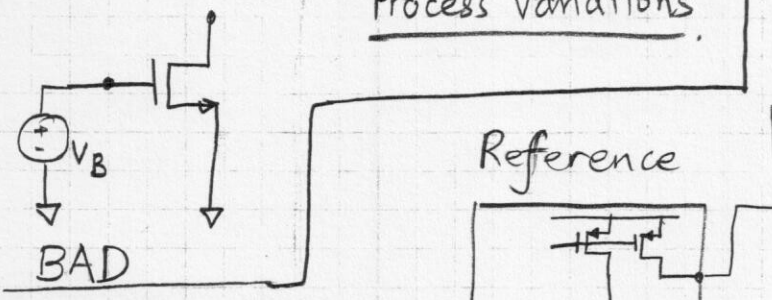
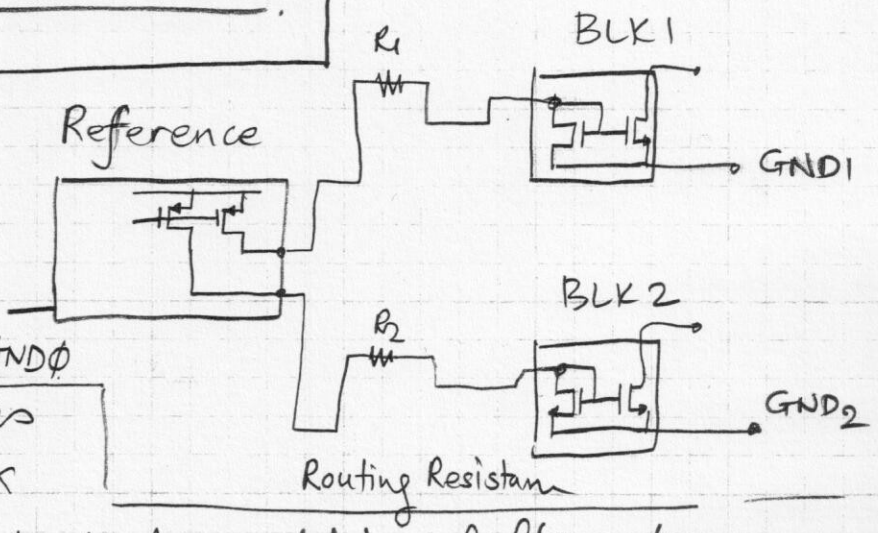
New Topic MOS Current Mirrors / Sources

Novice Biasing

Process variations.



ON CHIP CURRENT DISTRIBUTION



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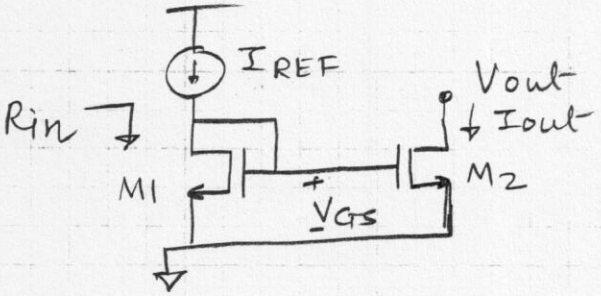
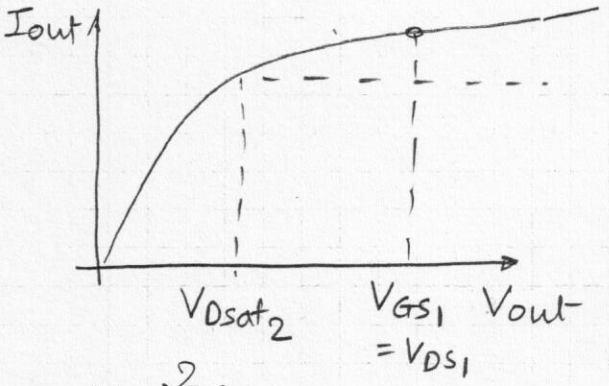
Simple Current mirror



$$R_{in} = \frac{1}{g_{m_1} + g_{ds_1}} \approx \frac{1}{g_{m_1}}$$



$$I_{REF} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{T_1})^2 (1 + \lambda_1 V_{GS_1})$$

$$I_{OUT} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{T_2})^2 (1 + \lambda_2 V_{out})$$

Assume $V_{T_1} = V_{T_2}$

$$\frac{I_{OUT}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1} \frac{(1 + \lambda_2 V_{OUT})}{(1 + \lambda_1 V_{GS})}$$

small

For accurate mirroring, keep L same $\Rightarrow \lambda_1 = \lambda_2$

$$\frac{I_{OUT}}{I_{REF}} = \frac{W_2}{W_1}\left(1 + \lambda (V_{out} - V_{GS})\right)$$

To keep λ small → use long channel device
L large $\gg L_{min}$

$$I_{OUT} = \frac{W_2}{W_1} I_{RFF}$$

For accurate mirroring $W_2 = N W_1$ (N: Integer)

DO NOT SCALE THE TRANSISTOR SIZE.

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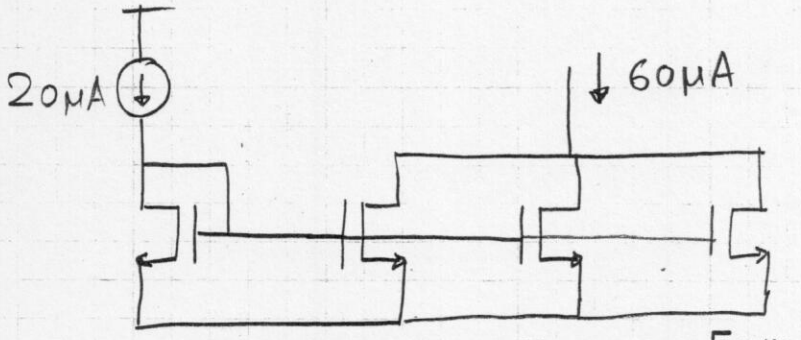
STAEDTLER® No. 937 811L Engineer's Computation Pad

Example

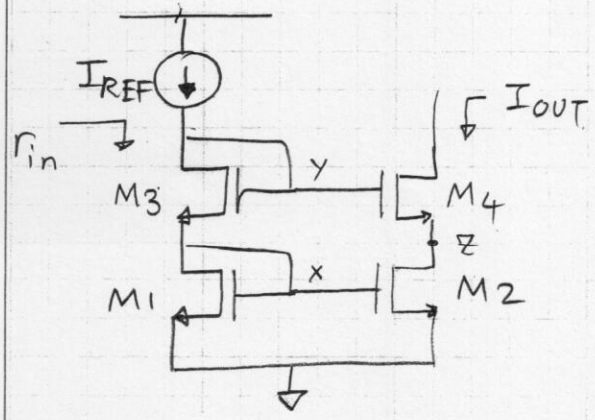


$\frac{W}{L}$	$\frac{5\mu m}{1\mu m}$	$\frac{5\mu m}{1\mu m}$	$\frac{5\mu m}{1\mu m}$	$\frac{5\mu m}{1\mu m}$ ← Large L, $\lambda\downarrow$

$$V_{out\,min} = V_{dsat_2}$$

$$R_{out} = \frac{1}{g_{ds_2}}$$

CASCODE CURRENT MIRROR



$$r_{in} = \frac{2}{g_m}$$

$$r_{out} \cong (g_{m_4} r_{o_4})\, r_{o_2}$$

$$V_y = V_{GS_3} + V_{GS_1}$$

$$V_z = V_{GS_3} + V_{GS_1} - V_{GS_4} = V_{GS_1}$$

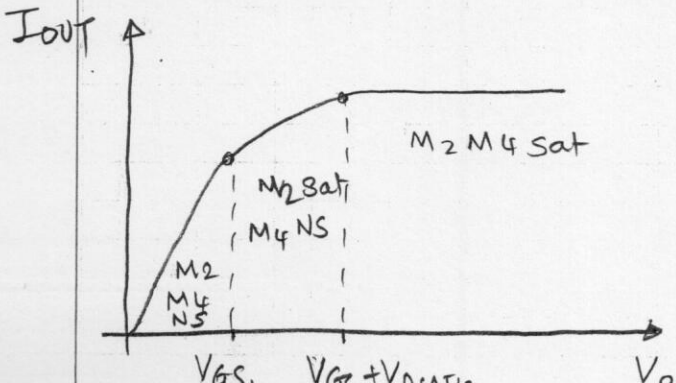
$$V_{OUT\,min} = V_z + V_{dsat_4}$$

$$= V_{GS_1} + V_{dsat_4}$$

$$\cong V_T + 2V_{dsat}$$

$$0.5V + 0.4V = 0.9V$$

NOT SUITABLE for low voltage



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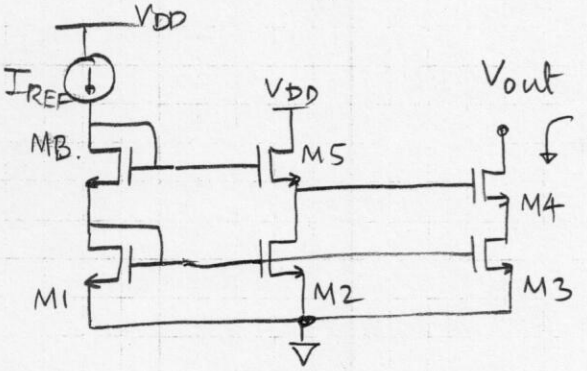
High Swing Cascode CM



DC imbalance M1 ↔ M3 different V_{DS}.

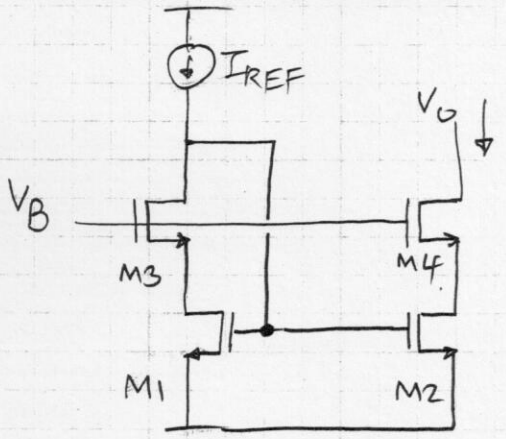
$M_1 - M_5$ identical.

$$\left(\frac{W}{L}\right)_B = \frac{1}{4}\left(\frac{W}{L}\right)_{1\text{-}5}$$

$$\Rightarrow V_{GS_B} = V_T + 2V_{dsat_1}$$

$$V_{OUT\,min} = 2V_{Dsat_1}$$

Low-voltage High swing Cascode CM.



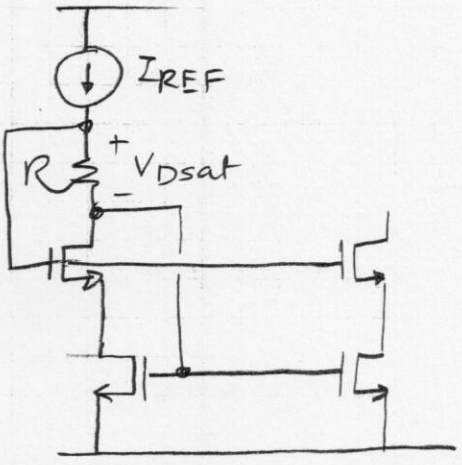
DC balance ✓

$$V_{DS_1} = V_{DS_2} = V_{Dsat}$$

$$V_B = V_T + 2V_{Dsat}$$

$$V_{omin} = 2V_{Dsat}$$

Smart Biasing



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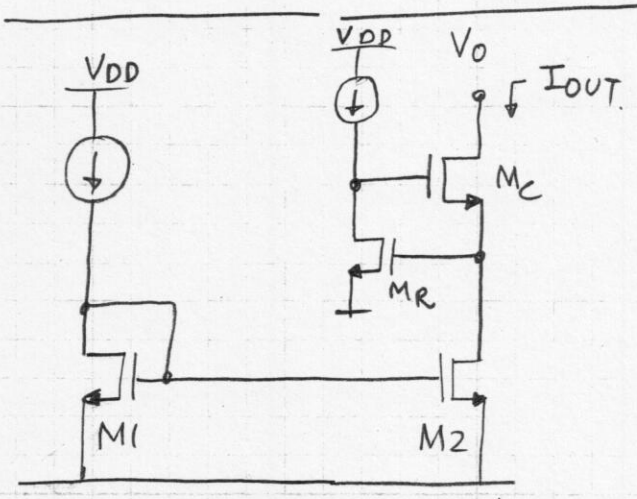
REGULATED CASCODE CM

YANG - ALLSTOT 1990 - CAS Tran



Series feedback

$V_{O_{min}} = V_{GS_R} + V_{Dsat_C}$

$= V_T + 2V_{dsat}$

Feedback loop $M_R - M_C$ - Loop gain $= (g_{m_R} r_{O_R}) \cdot 1$

r_{out} (without feedback) $= r_{O_2} \cdot (g_{m_C} r_{O_C})$

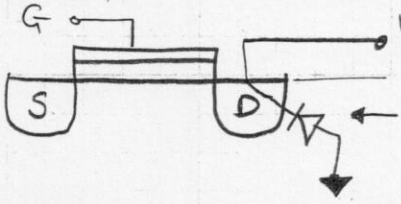
r_{out} (with feedback) $= r_{O_2} (g_{m_C} r_{O_C}) \cdot (g_{m_R} r_{O_R})$

$= (g_m r_O)^2 r_O$

$= (25)^2 \times 10K \approx 6.25\ M\Omega$

Really large

→ In reality r_{out} limited by leakage current due to Drain - Bulk diode of M_C.



← Diode leakage at high temperature

1.5V 500nA → 3MΩ

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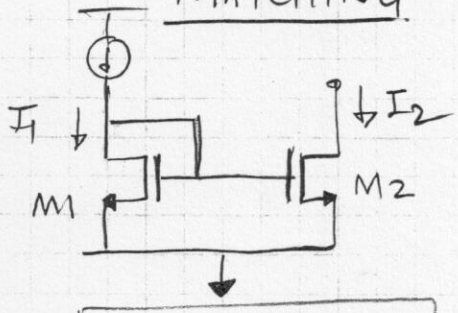
MATCHING CONSIDERATIONS



$$\beta = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)$$

$$I_1 = \beta_1 (V_{GS} - V_{T_1})^2 (1 + \lambda V_{DS_1})$$

$$I_2 = \beta_2 (V_{GS} - V_{T_2})^2 (1 + \lambda V_{DS_2})$$

Variat^n μ_n, C_{ox}, W, L, V_T

$$\frac{I_2}{I_1} = \frac{\beta_2}{\beta_1}$$

(assume all else equal)

Incremental analysis

$$\Delta\beta = \beta_2 - \beta_1$$

$$\beta = \frac{\beta_1 + \beta_2}{2}$$

$$\beta_1 = \beta - \frac{\Delta\beta}{2}$$

$$\beta_2 = \beta + \frac{\Delta\beta}{2}$$

$$I_2 = \frac{\left(\beta + \frac{\Delta\beta}{2}\right)}{\left(\beta - \frac{\Delta\beta}{2}\right)} I_1 = \frac{\left(1 + \frac{\Delta\beta}{2\beta}\right)}{\left(1 - \frac{\Delta\beta}{2\beta}\right)} I_1 \simeq \left(1 + \frac{\Delta\beta}{\beta}\right) I$$

Large β → large $\frac{W}{L}$ → smaller mismatch

V_T variations

$$V_{T_1} = V_T\left(1 + \frac{\Delta V_T}{2V_T}\right); \quad V_{T_2} = V_T\left(1 - \frac{\Delta V_T}{2V_T}\right)$$

$$\frac{I_2}{I_1} = \frac{(V_{GS} - V_{T_2})^2}{(V_{GS} - V_{T_1})^2} = \frac{\left(V_{GS} - V_T + \frac{\Delta V_T}{2}\right)^2}{\left(V_{GS} - V_T - \frac{\Delta V_T}{2}\right)^2}$$

$$= \frac{\left(1 + \frac{\Delta V_T}{2(V_{GS} - V_T)}\right)^2}{\left(1 - \frac{\Delta V_T}{2(V_{GS} - V_T)}\right)^2} = \left(1 + \frac{\Delta V_T}{(V_{GS} - V_T)}\right)\left(1 + \frac{\Delta V_T}{(V_{GS} - V_T)}\right)$$

$$= \left[1 + \frac{2\Delta V_T}{(V_{GS} - V_T)}\right]$$

To reduce mismatches increase $(V_{GS} - V_T)$ or Vdsat

Tradeoff with o/p swing

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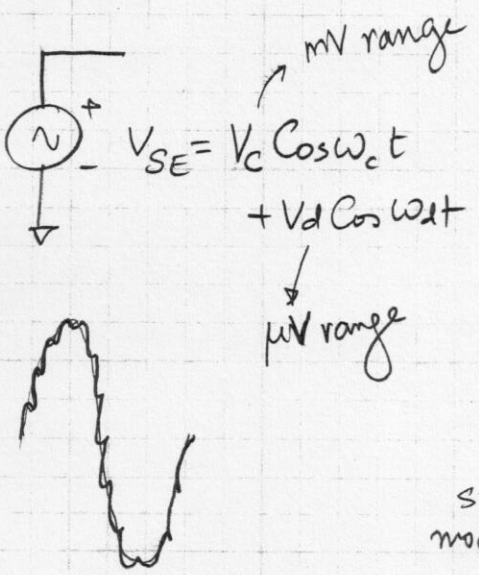
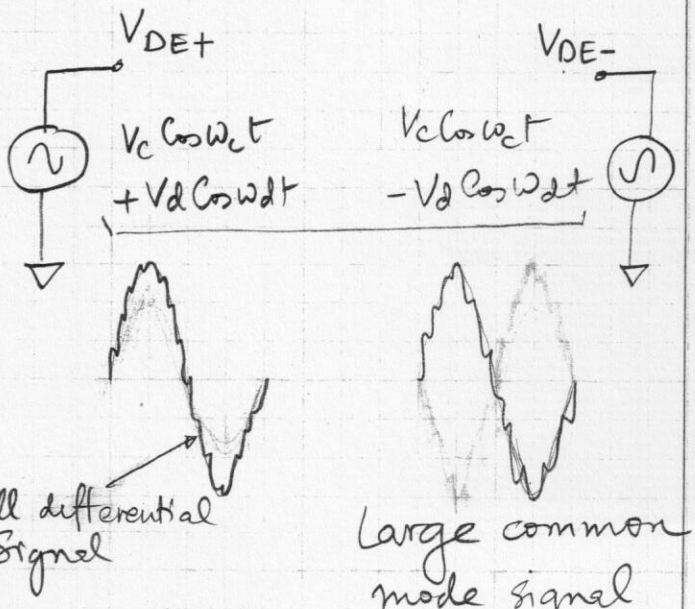
NEW TOPIC DIFFERENTIAL AMPLIFIERS

Why differential amplifier ?

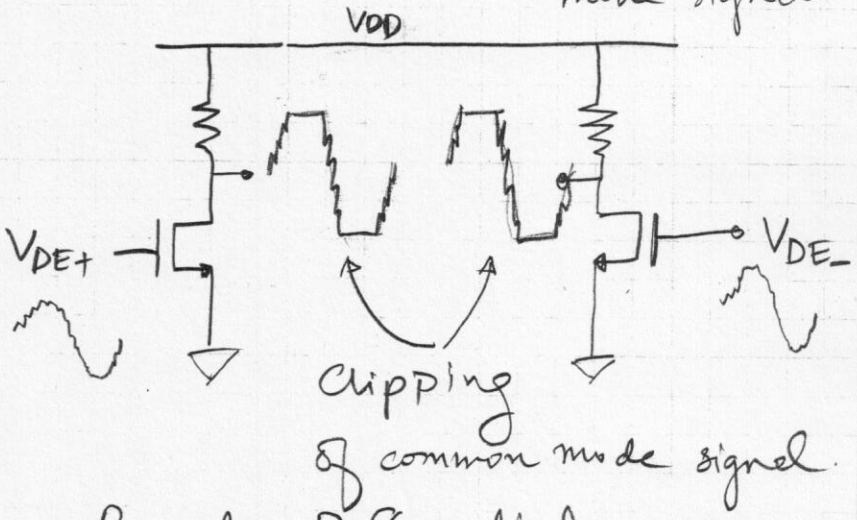
- Example – ECG
  - Detecting very small signal in presence of very large signal
  - Understanding whisper in presence of screaming voice
  - Difference Amplifier

Single Ended & Differential Signal




V_{DE+}
V_{DE-}
$V_c \cos\omega_c t + V_d \cos\omega_d t$
$V_c \cos\omega_c t - V_d \cos\omega_d t$
small differential mode signal
Large common mode signal

Large common mode signal could be 50 Hz Supply hum, – common mode coupling



VDD – Noise

Psuedo – Differential

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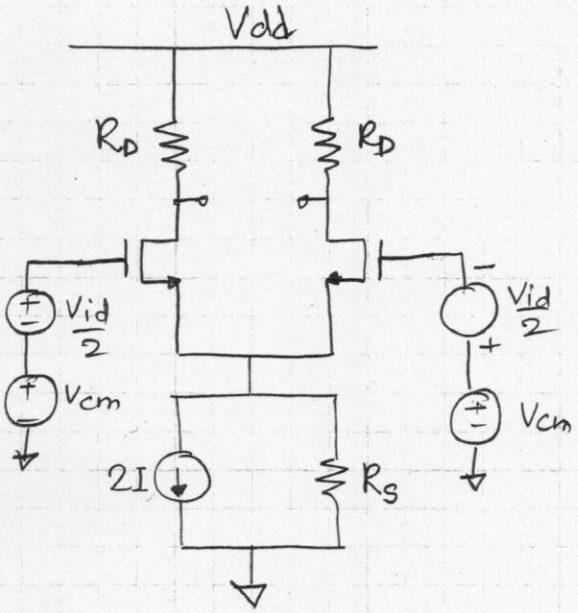
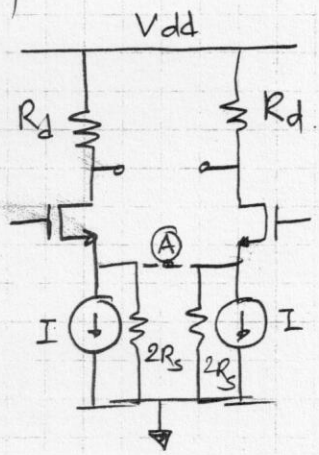


Goal

Large Differential gain
A_{dm}

Small Common-mode gain
A_{cm}
(over large range of V_{cm})

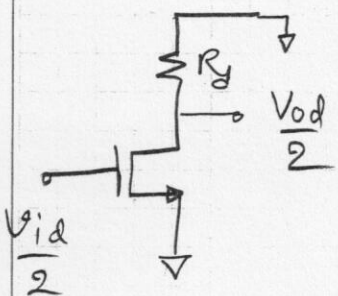
Symmetric Half Ckt



For differential i/p, — NO ac small signal V_{cm} is applied
(only DC V_{cm} bias)

(A) → Virtual ground

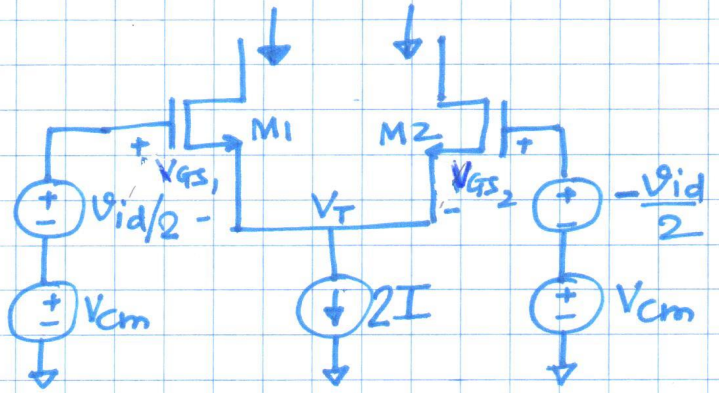
Half ckt analysis



$$A_{dm} = \frac{-g_{m_1}}{g_{ds_1} + \frac{1}{R_d}} = \frac{-g_m R_d}{1 + g_{ds} R_d}$$

Differential Pair Virtual Ground Concept

$I+\Delta i$ $\quad$ $I-\Delta i$ $\quad\leftrightarrow\quad (I+\Delta i)+(I-\Delta i)=2I$ (KCL)



Valid only for differential inputs

Assume V_{GS_1} & V_{GS_2} have equilibrium value of V_{eq}. They change by ΔV_{GS_1} & ΔV_{GS_2} on application of differential signal v_{id}.

Since the circuit is linearized around operating pt.

$(I+\Delta i)+(I-\Delta i)=2I \;\rightarrow\; I_1+I_2=2I$

$g_m\Delta V_{GS_1}+g_m\Delta V_{GS_2}=0 \;\leftarrow$

$$\Rightarrow \Delta V_{GS_1}=-\Delta V_{GS_2} \qquad \text{—①}$$

KVL $\quad V_{cm}+\frac{v_{id}}{2}-\Delta V_{GS_1}-V_{eq}=V_T=V_{cm}-\frac{v_{id}}{2}-\Delta V_{GS_2}-V_{eq}$

$$\Rightarrow \Delta V_{GS_1}-\Delta V_{GS_2}=v_{id} \qquad \text{—②}$$

FROM ① & ② V_T doesn't change.

Differential signal v_{id} is consumed by V_{GS_1} & V_{GS_2}. V_T doesn't change.

Hence Virtual Ground.

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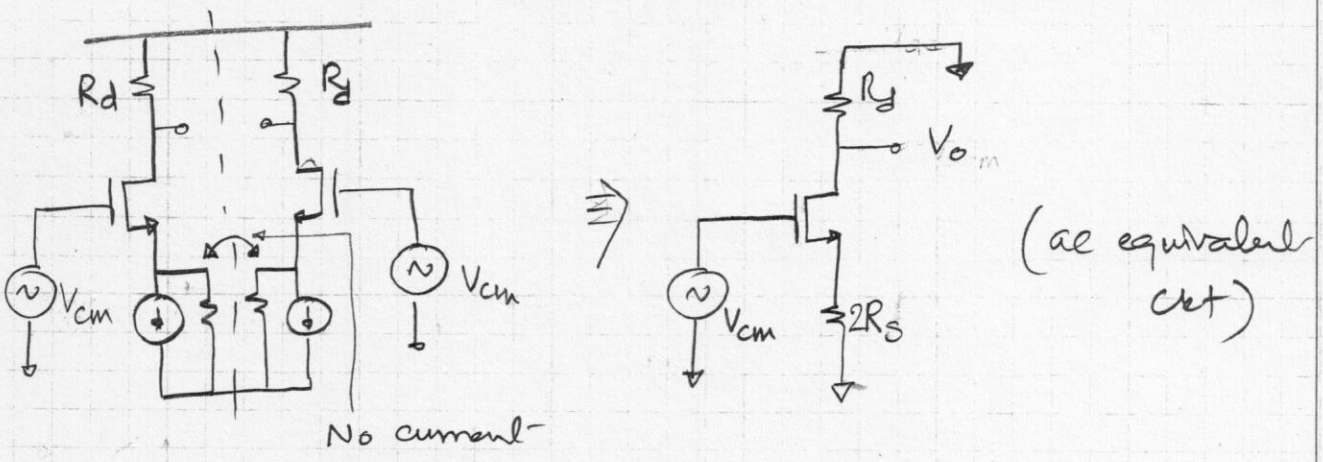
For common mode i/p $v_{id} = 0$, AC current @ V_{cm}



PROVE: $$A_{cm} = \frac{-g_m r_o R_d}{R_d + r_o + 2R_s\left(1 + (g_m + g_{mbs}) r_o\right)}$$

approximating

$$A_{cm} \cong -\frac{g_m r_o R_d}{2R_s g_m r_o} = -\frac{R_d}{2R_s}$$

CMMR - common mode rejection ratio

$$= 20 \log \left| \frac{A_{dm}}{A_{cm}} \right| = 20 \log \left| \frac{g_m R_d r_o \cdot 2R_s}{(r_o + R_d) R_d} \right|$$

$$= 20 \log \left(\frac{2(g_m r_o) R_s}{(r_o + R_d)} \right)$$

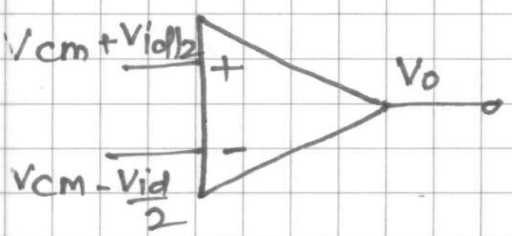
In CMOS implementation $R_d = r_o$ (PMOS)

$$= 20 \log (g_m R_s)$$ ← current source o/p resistance as high as possible

$$g_m R_s = \frac{2I}{(V_{GS} - V_T)} \cdot \frac{V_A}{I} = \frac{2V_A}{(V_{dsat})}$$ ← Early voltage, current src, diff pair.

Current source quality → CMRR

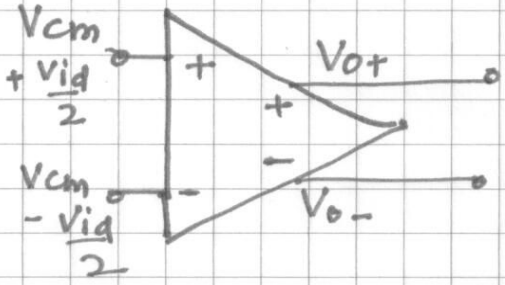
About COMMON-MODE REJECTION.



$$\underbrace{A_{cm} \cdot V_{cm}}_{\text{undesired}} + \underbrace{A_{dm} \cdot V_{id}}_{\text{Desired}}$$

$$CMRR = 20 \log \left| \frac{A_{dm}}{A_{cm}} \right|.$$

Consider amplifier with differential outputs



$$A_{cm} \cdot V_{cm} + A_{dm} \frac{V_{id}}{2} + A_{CMDM}(V_{cm})$$

$$A_{cm} \cdot V_{cm} + A_{dm}\left(-\frac{V_{id}}{2}\right) + A_{CMDM}(-V_{cm})$$

Desired.

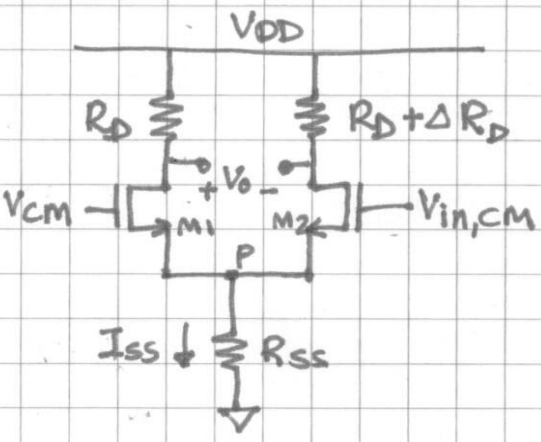
* Will be rejected by Next Diff Amp
* Only changes bias points
  → may alter small signal gain
* Can limit output voltage swing

Common-Mode to Diff. mode conversion

* Corrupts desired differential signal
* Due to ~~Asst~~ Asymmetry due to Mismatches
* Frequency dependent effects.

  Example: High frequency CM → Modifies tail current source ← parasitic cap across tail current.

Example ACM-DM. due to mismatch.



SF concept

$$\Delta V_p = \frac{R_{ss}}{R_{ss} + 1/2g_m}\Delta V_{in,cm} = \frac{2g_m R_{ss}}{1+2g_m R_{ss}}\Delta V_{in,cm}$$

$$\Delta I_{ss} = \frac{2g_m R_{ss}}{1+2g_m R_{ss}} \cdot \frac{\Delta V_{in,cm}}{R_{ss}}$$

↑ Splits equally on both sides

$$\Delta I_{D_1} = \Delta I_{D_2} = \frac{g_m}{1+2g_m R_{ss}}\Delta V_{in,cm}$$

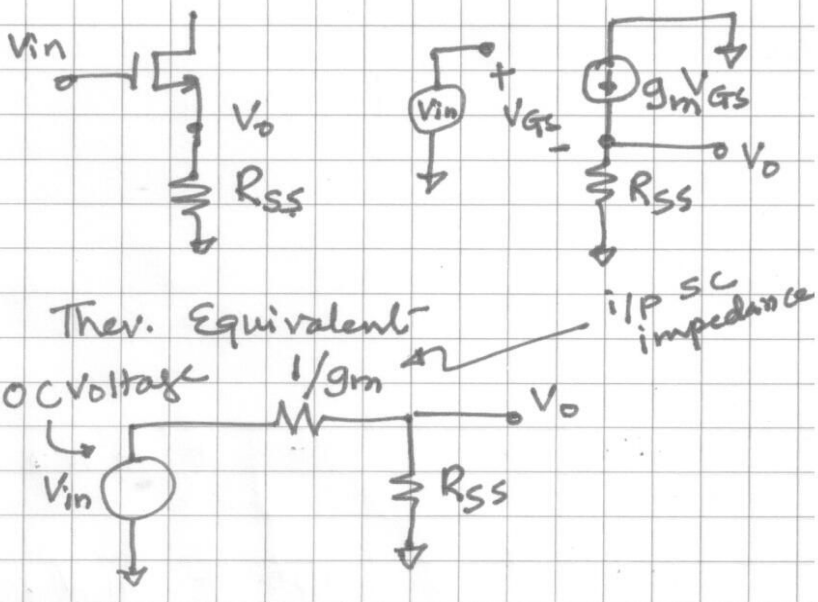
$$\Delta V_{out_{CM-DM}} = -\Delta I_{D_1} R_D - \left[-\Delta I_{D_2}(R_D+\Delta R_D)\right]$$

$$= \Delta I_D \cdot \Delta R_D = \frac{g_m \Delta R_D}{1+2g_m R_{ss}}\Delta V_{in,CM}.$$

$$\therefore A_{CM-DM} = \frac{g_m \Delta R_D}{1+2g_m R_{ss}}.$$

Side Note

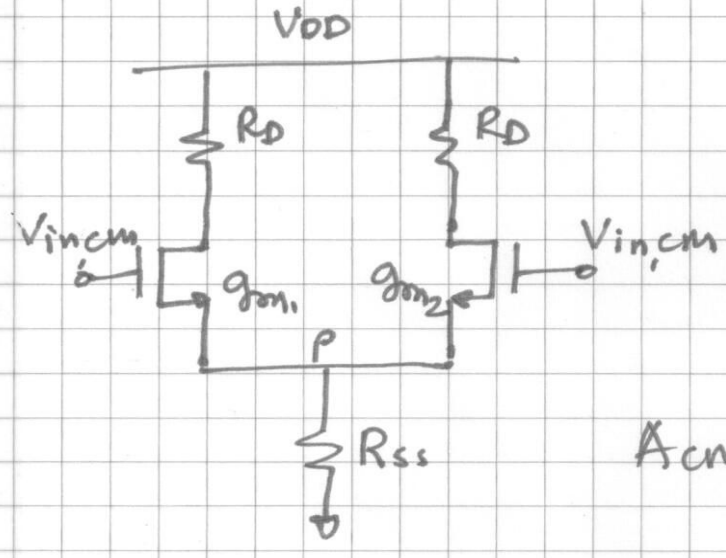
Source Follower



$$\frac{V_o}{V_{in}} = \frac{R_{ss}}{R_{ss} + 1/g_m}.$$

Insight. R_{SS} → Current Source output impedance

R_{SS} should be large to achieve good CMRR.



$g_{m_1} \neq g_{m_2}$ (mismatches)

↪ HW prove.

$$A_{CM-DM} = -\frac{\Delta g_m R_D}{1 + (g_{m_1} + g_{m_2}) R_{SS}}$$

R_{SS} - current source o/p impedance.

For a fully differential circuit:
Input and output both are differential

$$CMRR = \left| \frac{A_{DM}}{A_{CM-DM}} \right|$$

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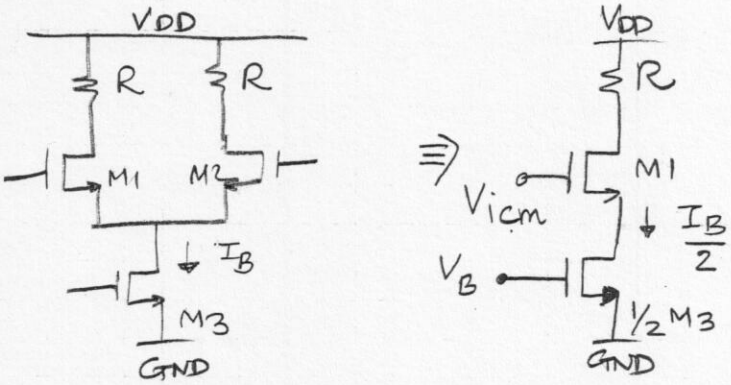
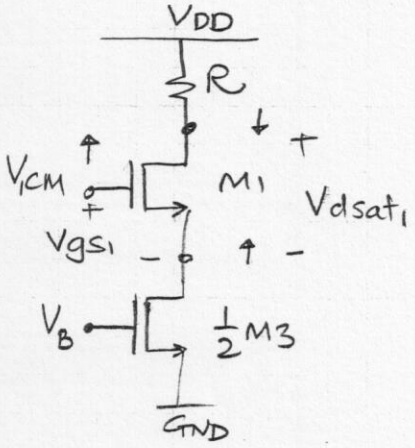
Common-mode Range CMR

– Range of common-mode input voltages for which all devices are in saturation.



Calculating $V_{icm}(max)$



$V_{icm}(max)$ when M1 enters non-sat

$$V_{icm}(max) - V_{gs1} = V_{DD} - \frac{I_B R}{2} - V_{dsat1}$$

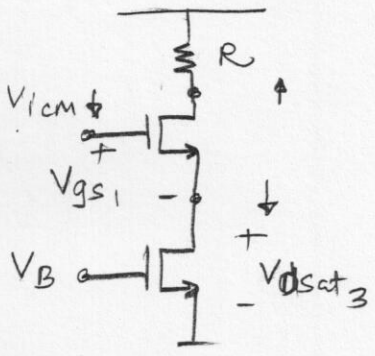
$$V_{icm}(max) = V_{DD} - \frac{I_B R}{2} + V_{gs1} - V_{dsat1}$$

$$= V_{DD} - \frac{I_B R}{2} + V_{T1}$$

DC drop across R.

Typ $V_{icm}(max) = (V_{DD} - V_{dsat})$ [↑ can be larger than V_{DD}]

Calculating $V_{icm}(min)$



$V_{icm}(max)$ – when M3 enters non-sat

$$V_{icm}(min) = V_{gs1} + V_{dsat3}$$

$$= V_{T1} + V_{dsat1} + V_{dsat3}$$

$$\approx V_T + 2V_{dsat}$$

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Example $V_{DD} = 1.8V$ $V_{TN} = 0.5V$ $V_{Tp} = -0.6V$

$V_{dsat} \approx 150mV$

For nmos diff pair – amplifier

$V_{icm(max)} = V_{DD} - V_{dsat} \cong 1.8V - 0.15 = 1.65V$

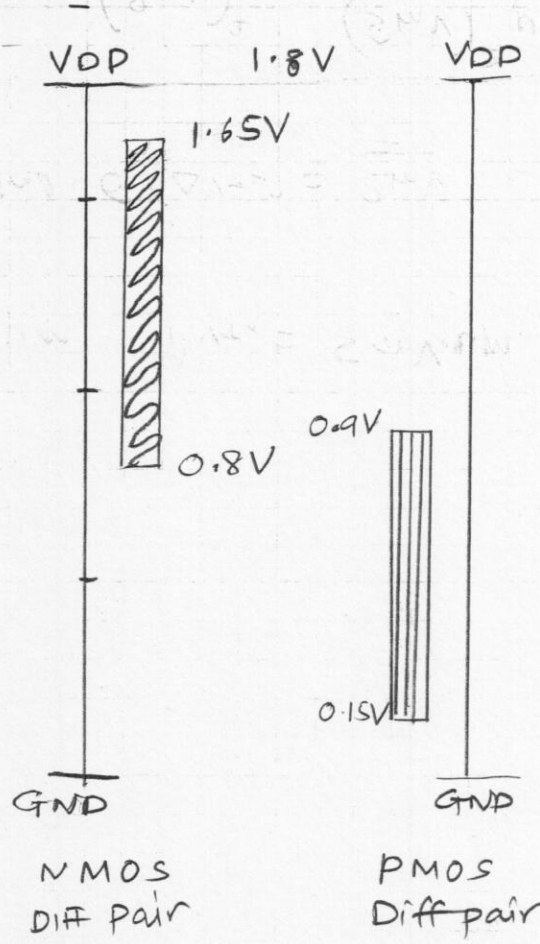
$V_{icm(min)} = V_T + 2V_{dsat} = 0.5V + 0.3V = 0.8V$

For pmos diff pair – amplifier

(-ve dirⁿ) $V_{icm(max)} = 0 + 0.15V = 0.15V$

$V_{icm(min)} = V_{DD} - (V_T + 2V_{dsat}) = 1.8 - (0.6 + 0.3V)$

$= 0.9V.$



For Rail-to-Rail (V_{DD} – GND) V_{ICM}, smart combination of NMOS – PMOS diff pair is used.

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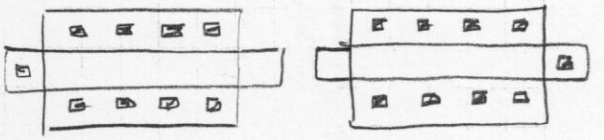
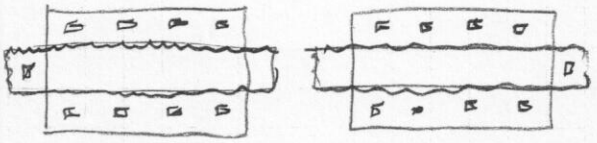
INTRODUCTION TO MISMATCHES



Diff pair transistors (layout tool)



After processing

jagged edges

Random variations. ΔW, ΔL

Intuitively as W & L ↑ Relative mismatch $\frac{\Delta W}{W}, \frac{\Delta L}{L}$ ↓

Mismatches decrease as area of transistor (WL) increases

— example — Breakup transistor in small pieces

→ averaging effect

→ Can be extended to other device parameters also.

$$\sigma(\Delta V_{TH}) = \frac{A_{VTH}}{\sqrt{WL}}$$

$$\sigma^2(\Delta V_{TH}) = \frac{A_{VTH}^2}{WL}$$

(variance)

A_{VTH} (mV μm)

$\cong 5$ (0.18μm process)

[=30 → 2.5μm]

$$\sigma\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta}{\sqrt{WL}}$$

$$\sigma^2\left(\frac{\Delta\beta}{\beta}\right)^2 = \frac{A_\beta}{WL}$$

(variance)

$A_\beta \Rightarrow$ (% μm)

$\cong 1$ (0.18μm proces)

[2.5 → 2.5μm]

good references

- measured values.
- Theory in Pelgrom – JSSC OCT 89
- Lakshmi kumar – JSSC Dec 86
- Kinget – JSSC June 2005

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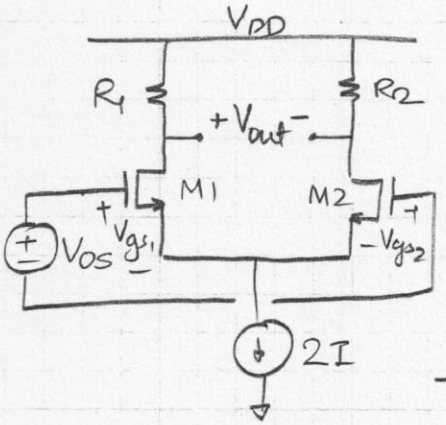
Effect of Mismatches

Allstot Razavi 14.2.1



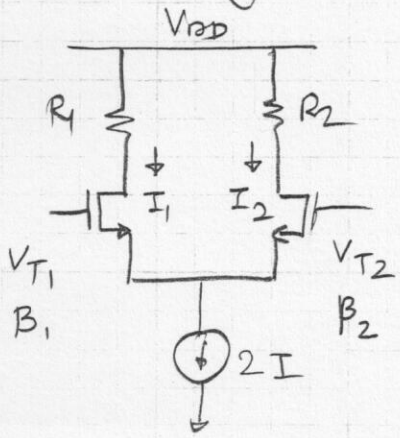
Input referred offset voltage

V_{os} = i/p DC voltage required to make $V_{out} = 0$

→ Systematic offset – Bad design practices → $\left(\frac{W}{L}\right)_1 \neq \left(\frac{W}{L}\right)_2$ or $R_1 \neq R_2$

→ Random offsets — process variations

Calculating Offset voltage



$$I_1 R_1 = I_2 R_2$$

$$V_{os} = V_{GS_1} - V_{GS_2}$$

$$= V_{T_1} + \sqrt{\frac{I_1}{\beta_1}} - V_{T_2} - \sqrt{\frac{I_2}{\beta_2}}$$

Incremental analysis

avg quantity $X = \frac{X_1 + X_2}{2}$

$X_1 = X + \frac{\Delta X}{2}$

$X_2 = X - \frac{\Delta X}{2}$

apply this to I, R, V_T, β

$$V_{T_1} = V_T + \frac{\Delta V_T}{2} \qquad \beta_1 = \beta + \frac{\Delta\beta}{2} \qquad R_1 = R + \frac{\Delta R}{2}$$

$$V_{T_2} = V_T - \frac{\Delta V_T}{2} \qquad \beta_2 = \beta - \frac{\Delta\beta}{2} \qquad R_2 = R - \frac{\Delta R}{2}$$

$$I_1 = I + \frac{\Delta I}{2}$$

$$I_2 = I - \frac{\Delta I}{2}$$

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$$V_{OS} = V_{T1} - V_{T2} + \sqrt{\frac{I_1}{\beta_1}} - \sqrt{\frac{I_2}{\beta_2}}$$

$$= \Delta V_T + \sqrt{\frac{I}{\beta}}\sqrt{\frac{1+\Delta I/2I}{1+\Delta\beta/2\beta}} - \sqrt{\frac{I}{\beta}}\sqrt{\frac{1-\Delta I/2I}{1-\Delta\beta/2\beta}}$$

$$= \Delta V_T + \sqrt{\frac{I}{\beta}}\left[\left(1+\frac{\Delta I}{4I}-\frac{\Delta\beta}{4\beta}\cdots\right)-\left(1-\frac{\Delta I}{4I}+\frac{\Delta\beta}{4\beta}\cdots\right)\right]$$

$$= \Delta V_T + \sqrt{\frac{I}{\beta}}\left(\frac{\Delta I}{2I}-\frac{\Delta\beta}{2\beta}\right)$$

Random quantities - Rms sum all (+)

$$V_{OS} \simeq \Delta V_T + \sqrt{\frac{I}{\beta}}\left(\frac{\Delta I}{2I}+\frac{\Delta\beta}{2\beta}\right) = \Delta V_T + \frac{2I}{g_m}\left(\frac{\Delta I}{2I}+\frac{\Delta\beta}{\beta}\right)$$

$$= \Delta V_T + (V_{GS}-V_T)\left(\frac{\Delta I}{2I}+\frac{\Delta\beta}{2\beta}\right)$$

$$I_1R_1 = I_2R_2 \Rightarrow \left(I+\frac{\Delta I}{2}\right)\left(R+\frac{\Delta R}{2}\right) = \left(I-\frac{\Delta I}{2}\right)\left(R-\frac{\Delta R}{2}\right)$$

$$IR\left(1+\frac{\Delta I}{2I}\right)\left(1+\frac{\Delta R}{2R}\right) = IR\left(1-\frac{\Delta I}{2I}\right)\left(1-\frac{\Delta R}{2R}\right)$$

$$1+\frac{\Delta I}{2I}+\frac{\Delta R}{2R} \simeq 1-\frac{\Delta I}{2I}-\frac{\Delta R}{2R} \Rightarrow \frac{\Delta I}{I} = \frac{\Delta R}{R}$$

$$V_{OS} \simeq \Delta V_T + \frac{2I}{g_m}\left(\frac{\Delta R}{R}+\frac{\Delta\beta}{\beta}\right)$$

$\sigma(V_{OS})^2 = (\ )^2 + (\ )^2 + (\ )^2$

Taking to the next level $\frac{\Delta\beta}{\beta} = \frac{\Delta K'}{K'} + \frac{\Delta W}{W} + \frac{\Delta L}{L}$

$$\frac{\Delta R}{R} = \frac{\Delta\rho_\square}{\rho_\square} + \frac{\Delta L}{L} + \frac{\Delta W}{W}$$

W & L of Resistor

sheet R

→ Many terms contribute to offsets.

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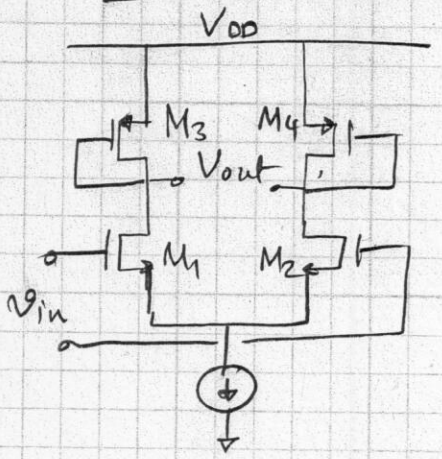
Back to Diff Pair

MOS Load instead of R load.

Diode PMOS load



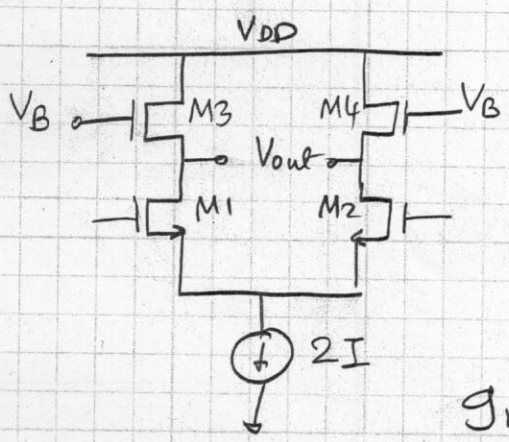
Voltage gain

$$A_v = -\frac{g_{mN}}{g_{mp} + g_{dsN} + g_{dsp}}$$

$$A_v \cong -\frac{g_{mN}}{g_{mp}}$$

$$A_v = -\sqrt{\frac{\mu_n (W/L)_N}{\mu_p (W/L)_P}}$$ (Low value)

Current Source PMOS LOAD



Voltage Gain

$$A_v = \frac{-g_{mN}}{(g_{dsN} + g_{dsp})}$$ High

$$g_{mN} = \frac{2I}{(V_{GS} - V_T)_N}$$

$$g_{dsN} = \lambda_N I$$

$$g_{dsp} = \lambda_P I$$

$$A_v = \frac{2}{(V_{GS} - V_T)_N} \cdot \frac{1}{(\lambda_N + \lambda_P)}$$ ← decided by channel length for NMOS PMOS

$(V_{GS} - V_T)_N$ ↓ 0.15V

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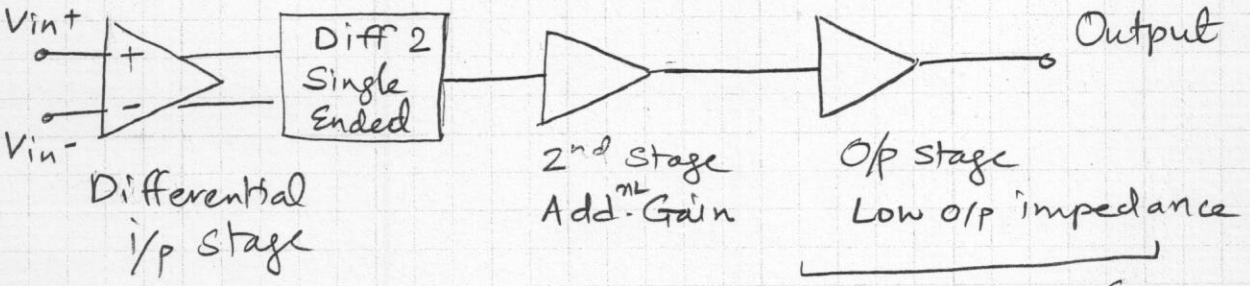
OPERATIONAL AMPLIFIERS

- Basic building block
- High gain differential Amplifier
- A very high V. (Voltage) gain (need not be accurate)
- High input impedance
- Low output impedance

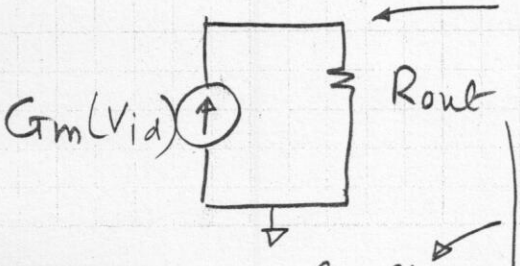
Generic Topology



OPAMP — Low o/p impedance includes final buffer stage

OTA - Operational Transconductance Amplifier
- high o/p impedance
- Current o/p

$V_{out} = [G_m R_{out}]\, V_{id}$



Most Common On-Chip

→ Can be used as voltage amplifier when driving high impedance loads.

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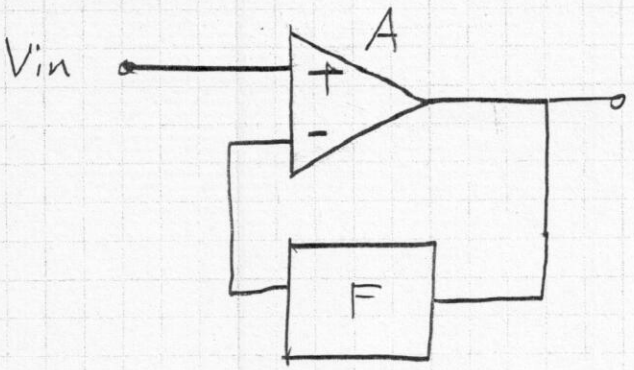
OPAMP/OTA performance Parameters

★ **Voltage Gain** — Determines precision of feedback System.

Example:



$$\frac{V_{out}}{V_{in}} = \frac{A}{1+AF} = \frac{1}{\frac{1}{A}+F} \approx \frac{1}{F}$$

A needs to be Larger than Spec.

↑ driven by desired accuracy

↓ Does not need to be accurate

F can be decided by ratio of R or Cs, — accurate vs. process, temp, voltage variations.

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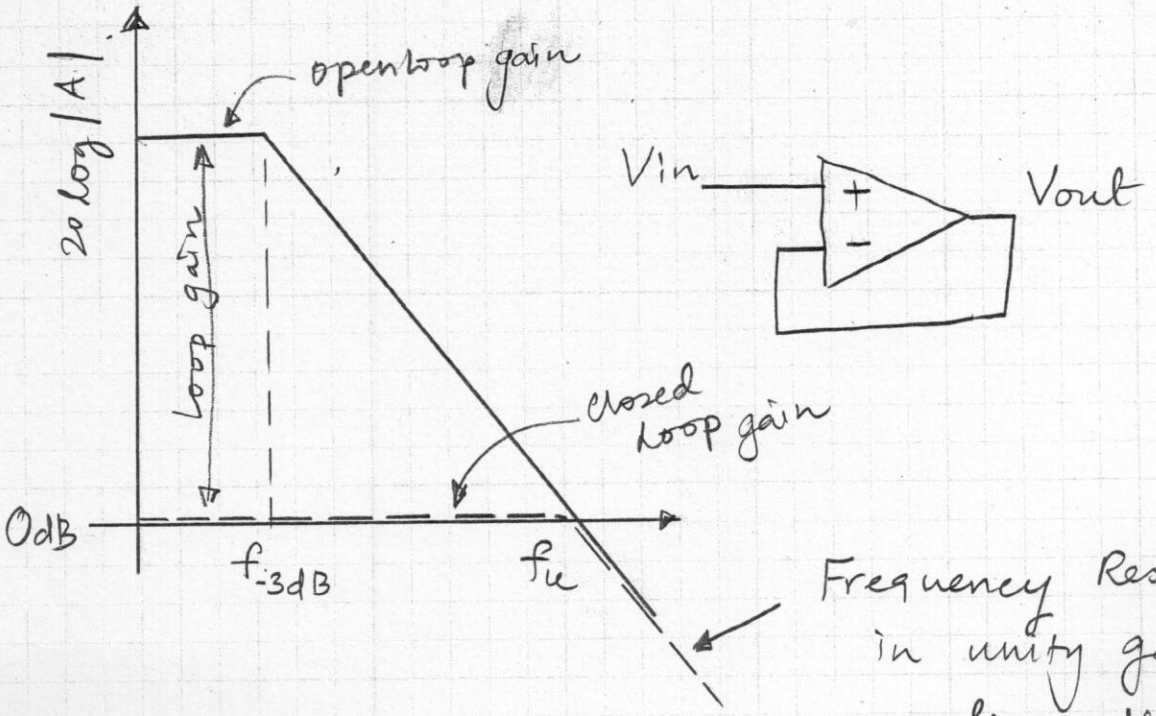
★ Small Signal BW

Open loop frequency response



→ Decides closed loop freq. response after feedback

→ Gain Margin / Phase Margin
(we will be discussing this extensively later)

→ Stability important.

★ Output swing – Large – keeping all transistors in Saturation (maintaing high ac gain)

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★ Input Common-Mode range

- i/p CMR for which all transistors are in saturation.
- NMOS - $(V_{DD} - V_{DSAT}) \leftrightarrow V_T + 2V_{DSAT}$
- PMOS - $[V_{DD} - (V_T + 2V_{DSAT})] \leftrightarrow V_{DSAT}$
- To handle Rail 2 Rail i/p
  - Combo of NMOS & PMOS. Diff i/p pair

★ Input Referred Offset

- Dominated by i/p Diff pair & load
- First Stage high gain
- Avoid systematic mismatches
- Large Device sizes to reduce random mismatches.

★ Noise - Determines minimum signal that can be accurately processed

- Similar treatment like offsets
- We will be studying this extensively.

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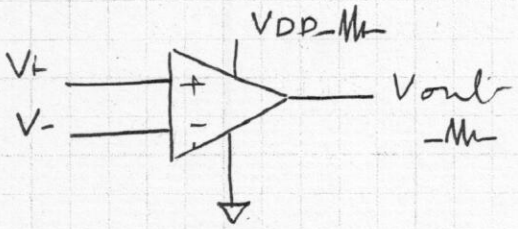
CMRR – Common-mode rejection ratio (already discussed)

PSRR – Power Supply Rejection Ratio

– How much of supply noise shows up @ o/p.

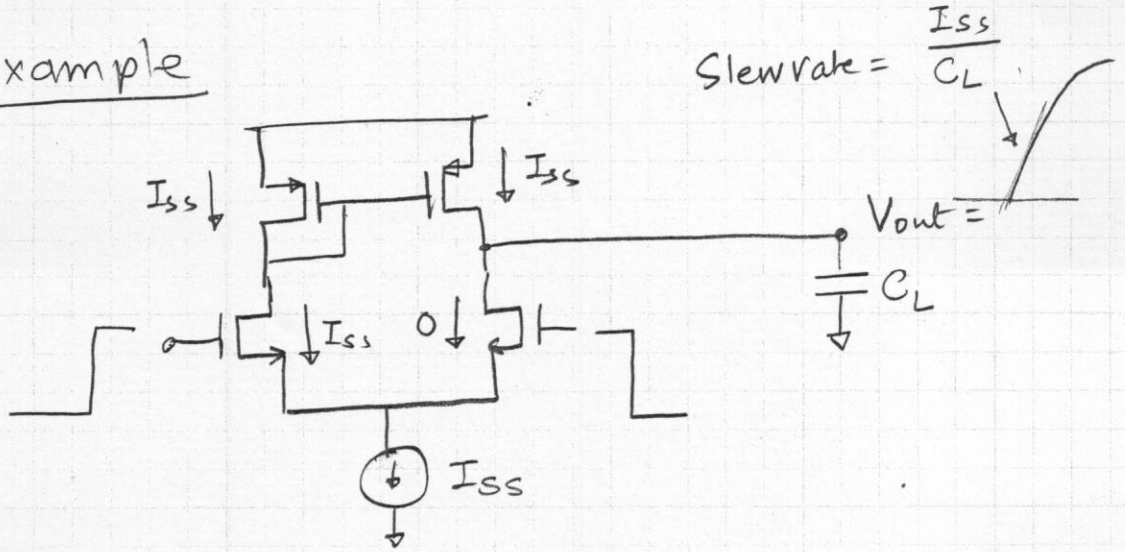


Large Signal Behavior – Slew rate

Slewing – Fastest change in the node voltage. Generally decided by

$$I/C = \frac{dV}{dt}$$

Example



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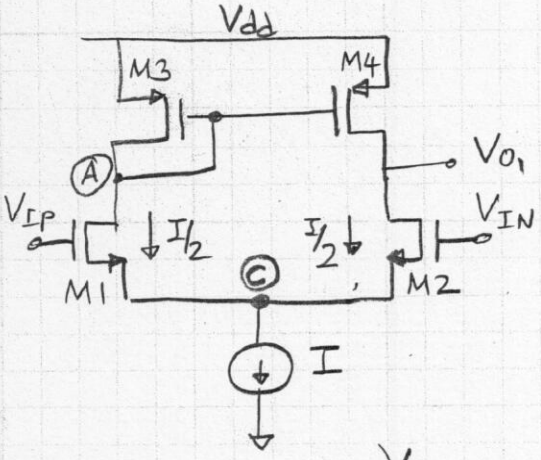
OTA Topologies

(— Allstot)



Single Stage OTA

Common-mode

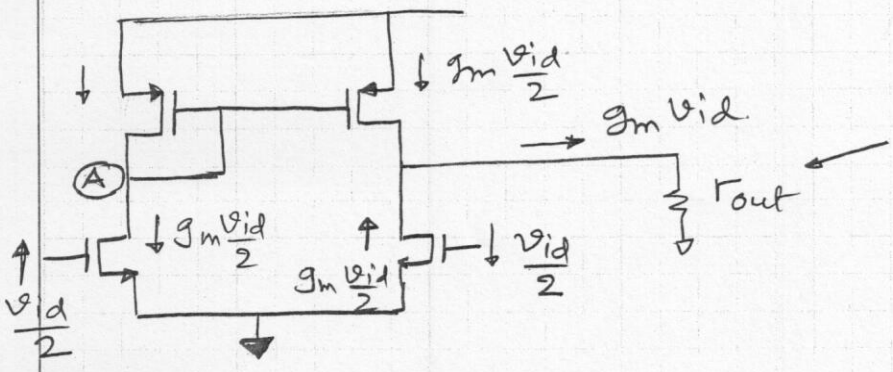
$V_{IP} = V_{IN} = V_{CM}.$ $\left(\frac{V_{dd}}{2}\right)$

Assume Feedback sets $V_{SD_3} = V_{SD_4}$

$$V_{SD_3} = V_{SD_4} = |V_{Tp}| + \sqrt{\frac{2(I/2)}{\mu_p C_{ox}\left(\frac{W}{L}\right)_p}}$$

$$V_{O_1} = V_{dd} - |V_{Tp}| - |V_{DSATp}|$$

Ac analysis — Node © — virtual ground node. for differential signal.



small signal O/P resistance $= \frac{1}{(g_{ds_2} + g_{ds_4})}$

$$V_{O_1} = \frac{g_{m_1} v_{id}}{g_{ds_2} + g_{ds_4}}$$

$$A_V = \frac{g_{m_1}}{g_{ds_2} + g_{ds_4}}$$ 25-100

$$g_{out_A} = g_{m_3} + g_{ds_3} + g_{ds_1} \approx g_{m_3}$$ — low imp. wide Bandwidth node.

Limited gain (one stage only)

D2SE included.

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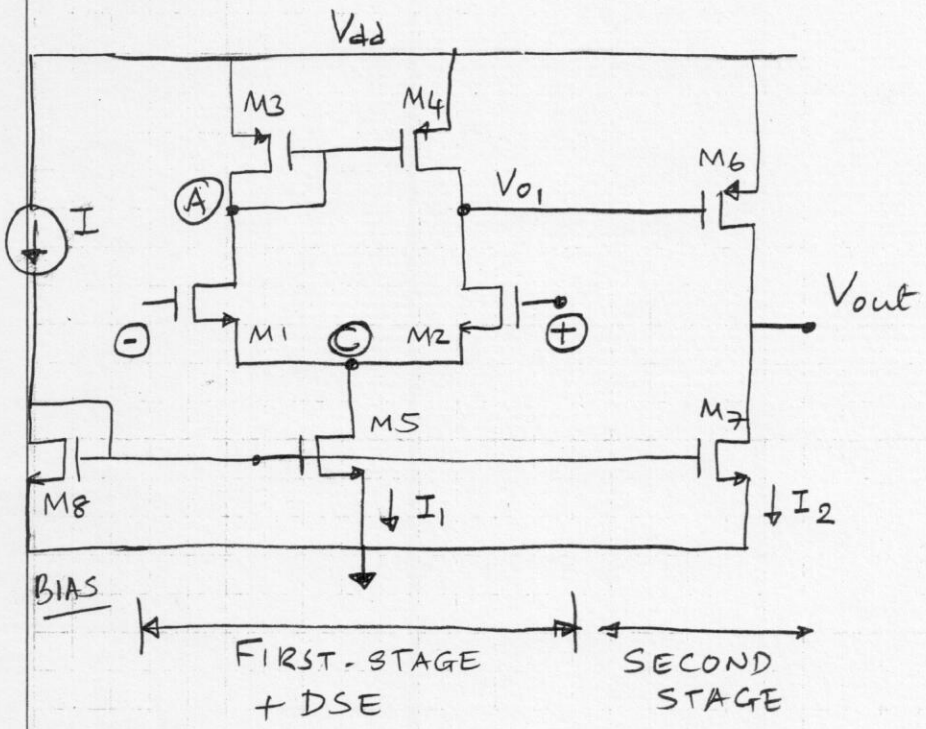
Two Stage OTA



BIASING — To avoid systematic offsets

(DC) $V_A = V_{o_1}$ $\left\{ \begin{array}{l} \text{Else} \\ V_{os} = \dfrac{V_{o_1} - V_A}{A} \end{array} \right.$ ← FIRST STAGE GAIN.

$$V_A = V_{dd} - V_{SG_3} = V_{o_1} = V_{dd} - V_{SG_6}$$

$$V_{SG_3} = V_{SG_6} \Rightarrow \text{Same } V_{dsat}.$$

$$|V_{T_3}| + \sqrt{\frac{2(I_1/2)}{\mu_p C_{ox}\left(\frac{W}{L}\right)_3}} = |V_{T_6}| + \sqrt{\frac{2(I_2)}{\mu_p C_{ox}\left(\frac{W}{L}\right)_6}}$$

Assuming $V_{T_3} = V_{T_6}$ (process matching)

$$\left(\frac{W}{L}\right)_6 = 2\left(\frac{I_2}{I_1}\right)\cdot\left(\frac{W}{L}\right)_3$$

Good design practice

Also use unit cell design – keep W same

M_3, M_4, M_6 – same L

$M_1 - M_2$ same W & L.

M_8, M_5, M_7 – same L.

$$V_{o1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} v_{id} \quad \& \quad V_{out} = \frac{g_{m6} V_{o1}}{g_{ds6} + g_{ds7}}$$

$$\text{Total gain} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} \cdot \frac{g_{m6}}{g_{ds6} + g_{ds7}}$$

↑ ↑

Each high impedance node contributes a low freq pole in frequency response

Each pole → 90° phase shift

Two poles → 180° phase shift → +ve feedback

– Limit Two gain Stages. for Stability.

– <u>Need for frequency compensation</u>

Motivation to Study Feedback & Stability

→ Then comeback & figure out frequency compensation of opamps.

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STAEDTLER Engineer's Computation Pad

Feedback & Stability

1927: Harold Black (Bell labs) — -ve feedback.

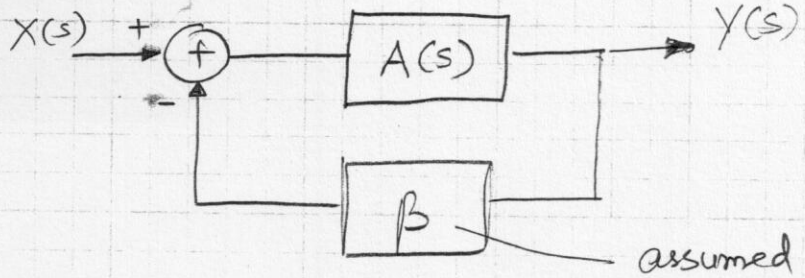
Advantages

1. Gain desensitization
2. Terminal impedance Modification
   - Shunt FB ↓ impedance
   - Series FB ↑ impedance
3. Bandwidth Modification. (increase in BW)
4. Nonlinearity reduction.

Disadvantages

1. Gain Reduction
2. Potential Instability.

Negative feedback example



$$\frac{Y(s)}{X(s)} = \frac{A(s)}{1+\beta A(s)}$$

Closed loop gain.

T = loop gain = $\beta A(s)$.

Closed loop gain goes to ∞ when $\beta A(s) = -1$

$\rightarrow |\beta A(s)| = 1$

$\rightarrow \angle \beta A(s) = -180°$.

Barkhausen's criteria for oscillation.

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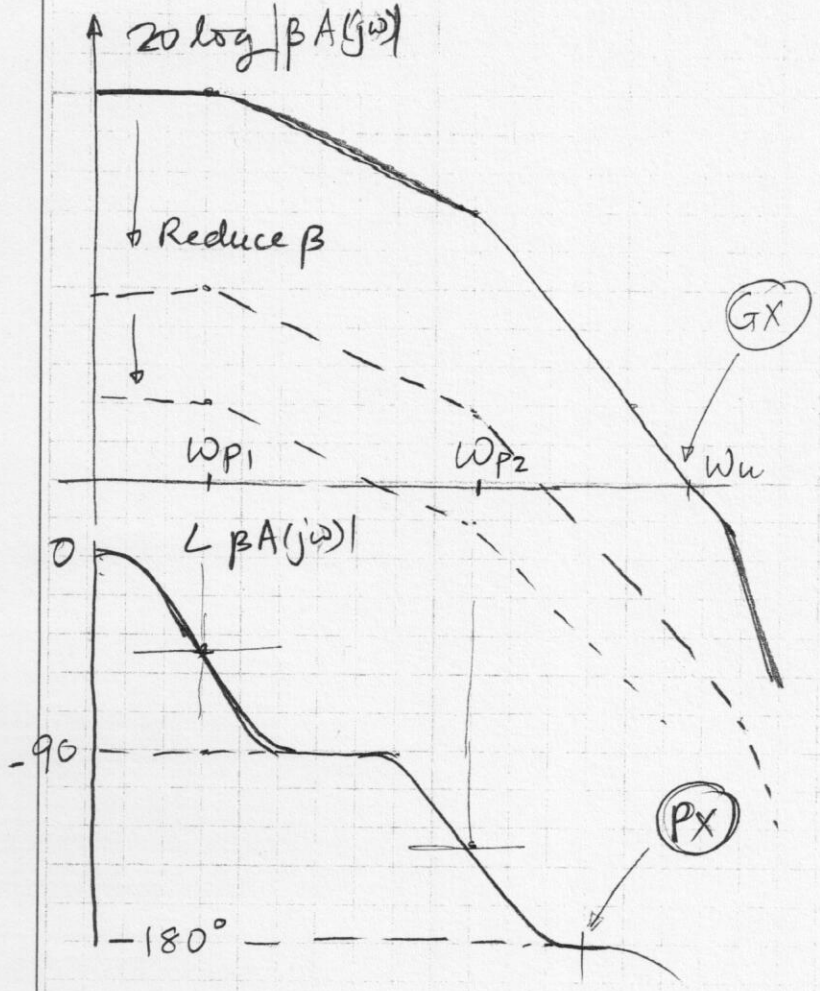
Consider Two-pole frequency response.

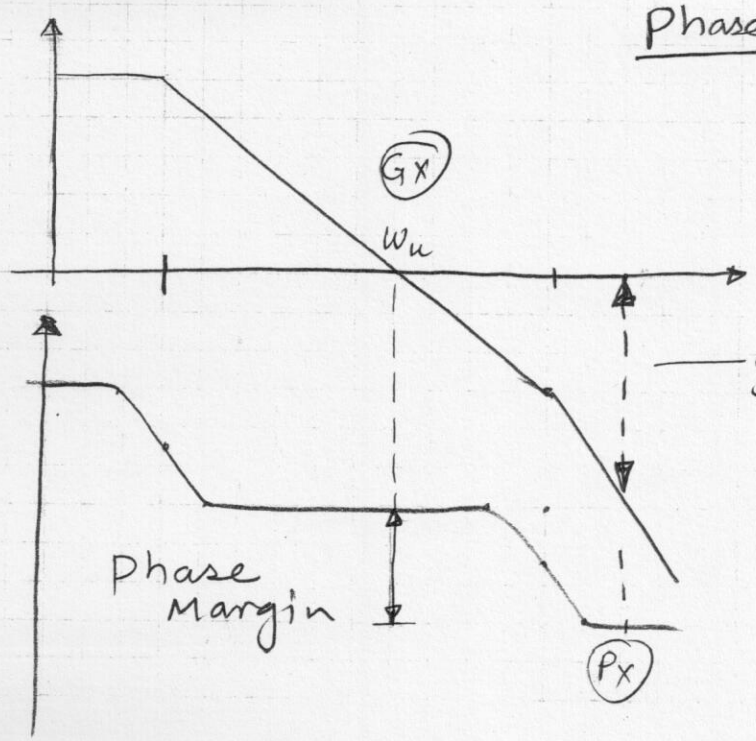


GX
Gain Crossover freq.
- Loop gain unity

PX
Phase Crossover freq.
- Loop phase shift 180°

For Stability
GX must occur before PX

Measure of Stability

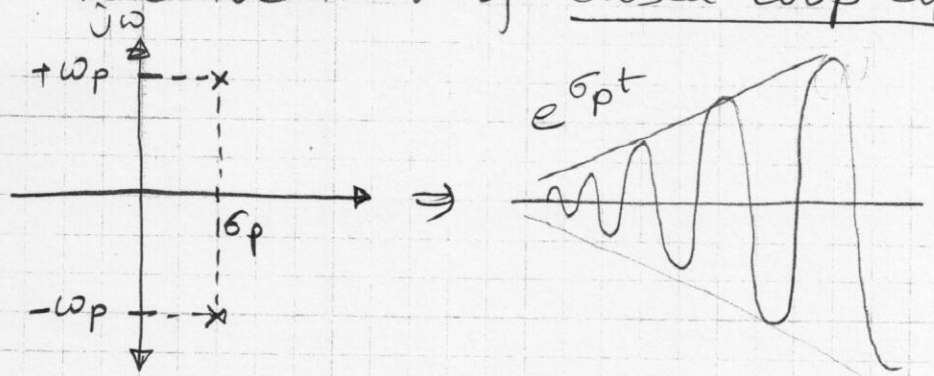


Phase Margin PM
$= 180° - \angle T(\omega_u)$
$= 60°$ (max. flat gain)
$= 70°$ (fast settling)

— Gain Margin GM

$GM = -20 \log |T(\omega_{-180°})|$
$= 12$ dB (typ).

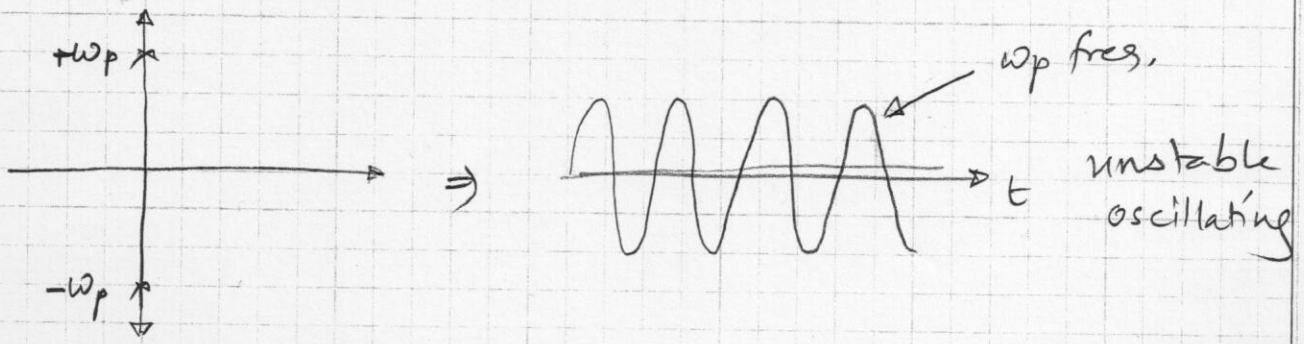
Pole location of Closed Loop System $\frac{Y(s)}{X(s)}$

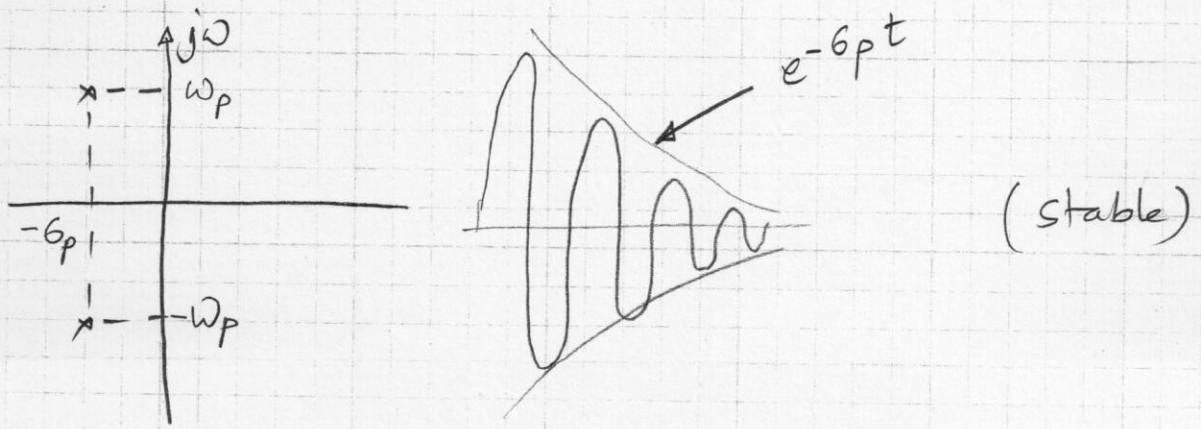


Not T(s) Loop Gain

Freq domain

Time domain





(stable)

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Example One pole amplifier

$$A(s) = \frac{A_0}{\left(1 + \frac{s}{\omega_{p_1}}\right)}$$

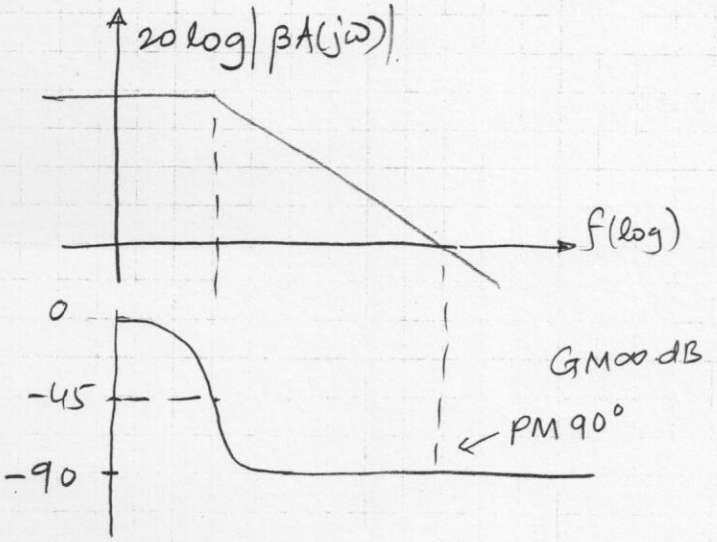
β constant

Loop Gain $T(s) = \dfrac{\beta A_0}{\left(1 + \frac{s}{\omega_{p_1}}\right)}$

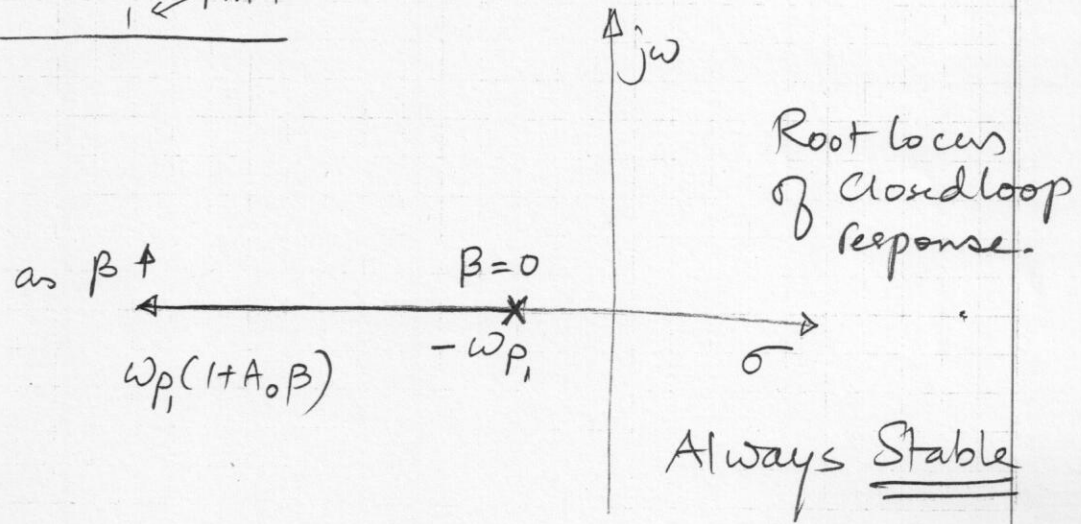
Closed loop gain

$$\frac{Y(s)}{X(s)} = \frac{\frac{A_0}{\left(1 + \frac{s}{\omega_{p_1}}\right)}}{1 + \frac{A_0\beta}{\left(1 + \frac{s}{\omega_{p_1}}\right)}} = \frac{A_0}{\left(1 + \frac{s}{\omega_{p_1}} + A_0\beta\right)}$$

$$\frac{Y(s)}{X(s)} = \frac{A_0/(1 + A_0\beta)}{1 + \frac{s}{\omega_{p_1}(1 + A_0\beta)}}$$ ← used for Root locus.



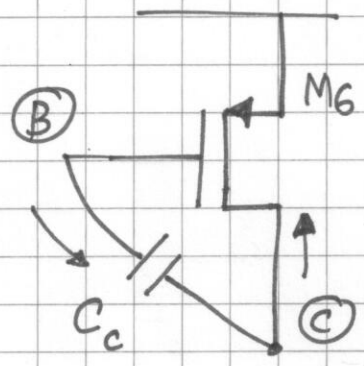
Unconditionally Stable



Root locus of closed loop response.

Always Stable

Cause of RHP Zero



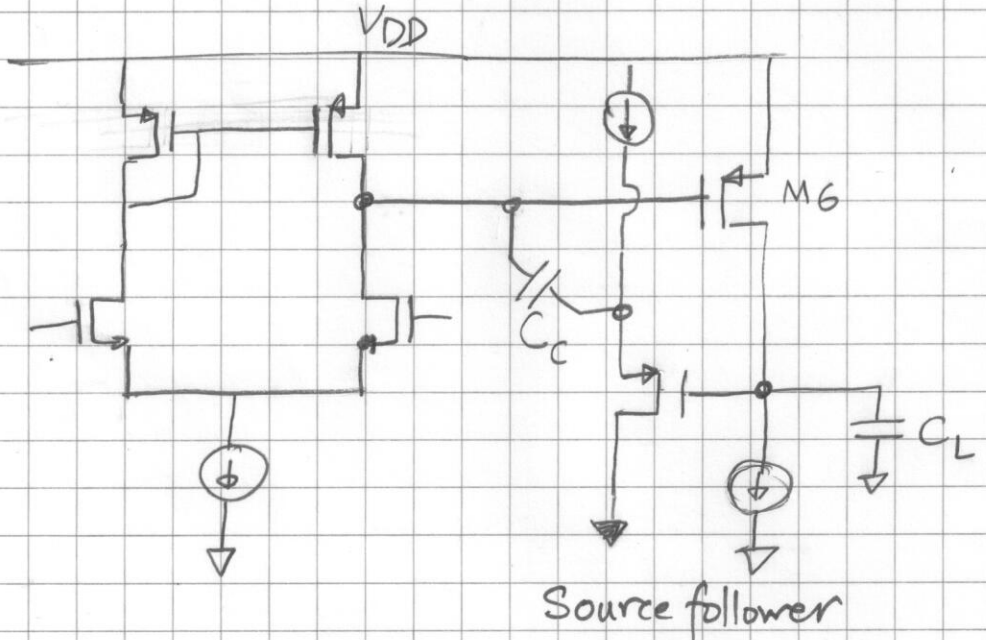
C_c around inverting stage

$\rightarrow \omega_z C_c V_B = g_{m_6} V_B$ @ zero freq.

$s \Rightarrow \omega_z = \frac{g_{m_6}}{C_c}$

→ Due to feedforward path.

Soln Remove feedforward path.

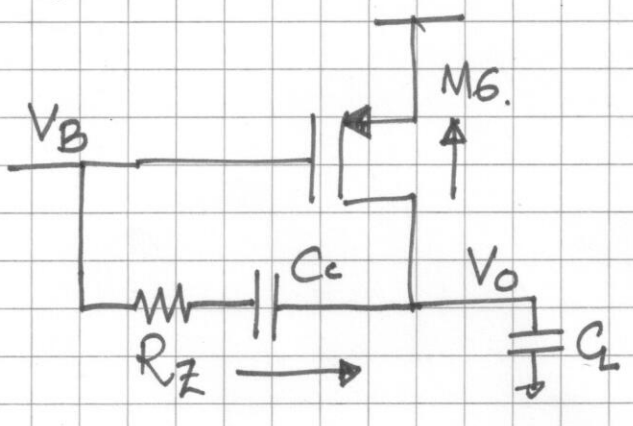


→ P_D & P_{ND} remain same as before.

⊖⊖ Power dissipation of SF.

⊖ SF frequency response. (must make sure that it doesn't deteriorate PM).

Another idea



Location of zero.

At zero freq. ω_z

$$\frac{V_B}{\left(R_z + \frac{1}{\omega_z C_c}\right)} = V_B g_{m6}$$

$$g_{m6}\left(R_z + \frac{1}{\omega_z C_c}\right) = 1$$

$$\frac{g_{m6}}{\omega_z C_c} = (1 - g_{m6} R_z) \Rightarrow \omega_z = \frac{g_{m6}/C_c}{(1 - g_{m6} R_z)}$$

When $g_{m6} R_z = 1 \Rightarrow R_z = \frac{1}{g_{m6}}$

Zero moves to ∞.

Better yet. When $g_m R_z > 1$ $\omega_z \rightarrow$ LHP zero. (-ve)

$\rightarrow$ cancel out Non-dominant pole..

$$\omega_z = \frac{g_{m6}/C_c}{(1 - g_{m6} R_z)} = -\frac{g_{m6}}{C_L}$$

(LHP Pole -ve sign.)

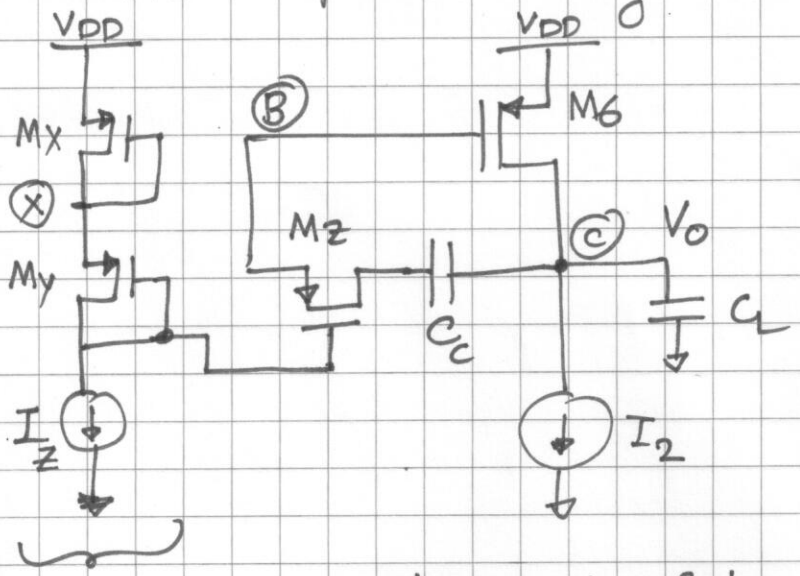
$$\frac{C_L}{C_c} = g_m R_z - 1 \Rightarrow R_z = \frac{1}{g_{m6}}\left(1 + \frac{C_L}{C_c}\right)$$

Really Cool idea!!

How do you achieve this. over PVT ?

R_z - resistor. — to track $\frac{1}{g_m}$.

R_Z → Implement using triode MOSFET.



M_Z – Non Sat.

$$I = \left[(V_{SG}-|V_{Tp}|)V_{SD} - \frac{1}{2}V_{SD}^2\right]\mu_p C_{ox}\left(\frac{W}{L}\right)_Z$$

$$R_Z = \left.\frac{1}{\partial I/\partial V_{SD}}\right|_{V_{SD}=0} = \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_Z (V_{SG}-|V_{Tp}|)_Z}$$

↖ Looks like g_m form.

By design (X) tracks (B) (DC bias)

$\Rightarrow V_{SG_X} = V_{SG_6}$ → choose I_Z & $\left(\frac{W}{L}\right)_X$

$$R_Z = \frac{1}{g_{m_6}}\left(1+\frac{C_L}{C_C}\right) = \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_Z \underbrace{(V_{SG}-|V_{Tp}|)_Z}}$$

↳ $= (V_{SG}-|V_{Tp}|)_Y$

$$\frac{\left(1+\frac{C_L}{C_C}\right)}{\mu_p C_{ox}\left(\frac{W}{L}\right)_6 (V_{SG}-|V_{Tp}|)_6} = \text{"}$$

$$\left(\frac{W}{L}\right)_Z = \left(\frac{W}{L}\right)_6 \cdot \frac{(V_{SG}-|V_{Tp}|)_6}{(V_{SG}-|V_{Tp}|)_Y} \cdot \left(\frac{C_C}{C_C+C_L}\right)$$

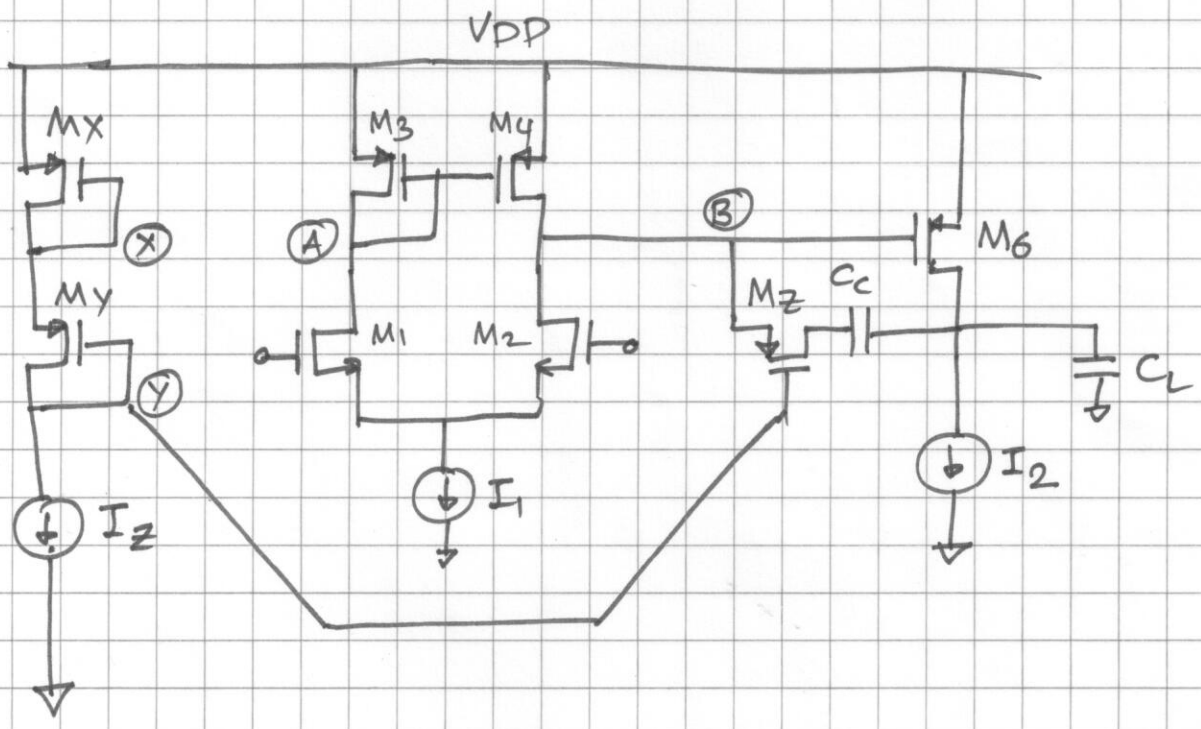
$$\left(\frac{W}{L}\right)_Z = \left(\frac{W}{L}\right)_6 \sqrt{\frac{2I_{6Q}}{\left(W/L\right)_6 \cdot \mu_p C_{ox}}} \times \sqrt{\frac{\left(\frac{W}{L}\right)_y \mu_p C_{ox}}{2I_Z}} \cdot \left(\frac{C_c}{C_c + C_L}\right)$$

$$= \sqrt{\frac{I_{6Q}}{I_Z}} \cdot \sqrt{\left(\frac{W}{L}\right)_6 \cdot \left(\frac{W}{L}\right)_y} \cdot \left(\frac{C_c}{C_c + C_L}\right)$$

→ All dependent on ratios – Not abs values

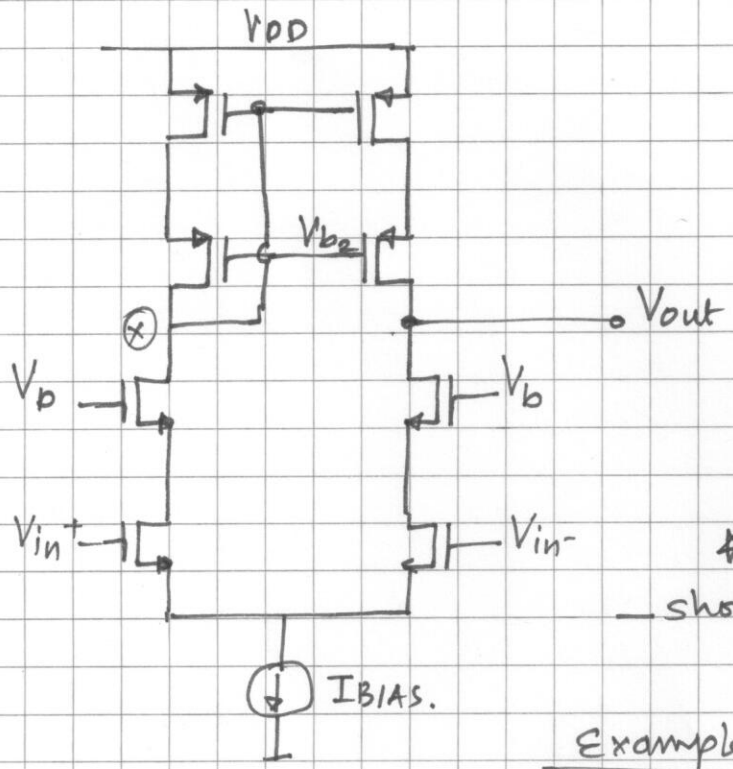
→ Tracking compensation.

* Black, Allstot, Reed. – JSSC Dec 83



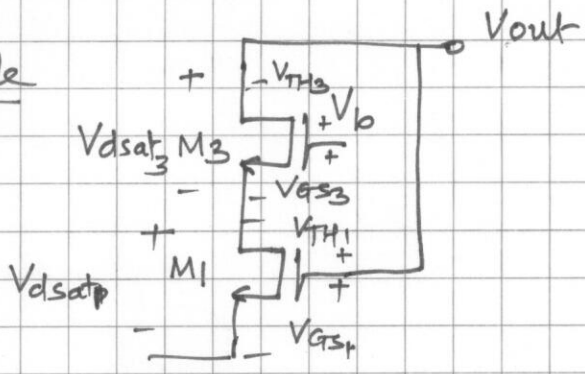
OPAMP ARCHITECTURES

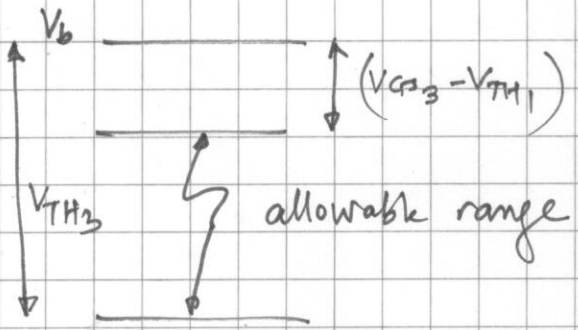
Telescopic Cascode Opamp.



* Single Stage.
  Low power - current reuse
* Limited output swing.
  $(V_{DD} - 2V_{dsat_n} - 2|V_{dsat_p}| - V_{IBIAS})$
* unity gain buffer difficult
  - shorting -ve i/p to o/p.

Example

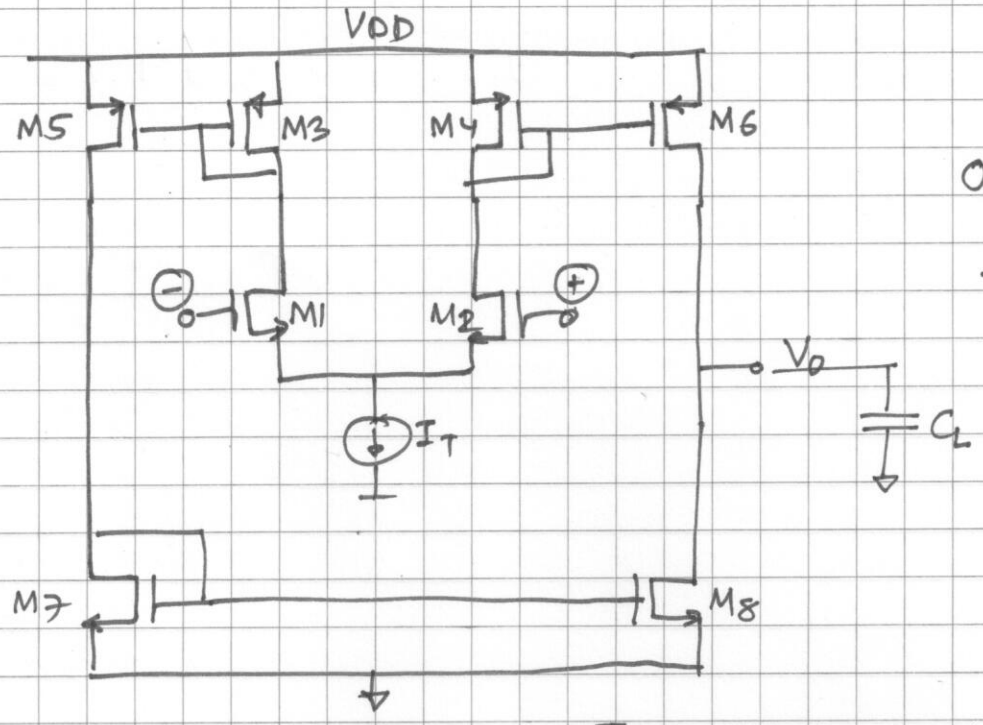




$$\text{Gain} = g_{m_N}\left[g_{m_N} r_{o_N}^2 \,\|\, g_{m_P} r_{o_P}^2\right]$$

* Mirror pole @ x

OPAMP using current mirrors



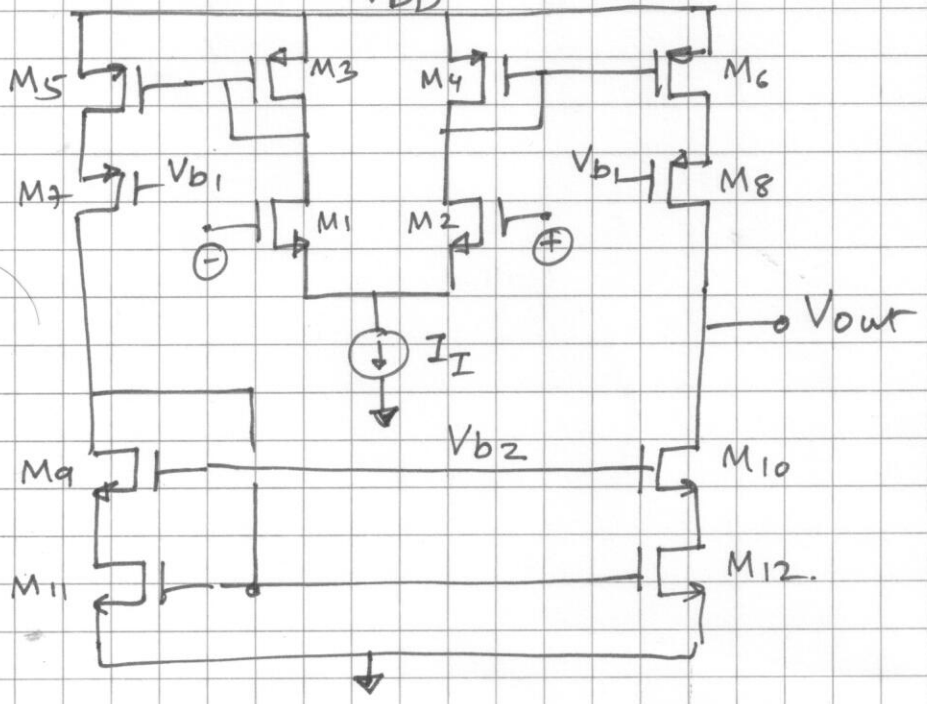
Output pole dominant - unloaded may become unstable.

Slew rate $= \frac{I_T}{C_L}$ (if all mirrors are unity gain)

$= M \frac{I_T}{C_L}$ (Mirror gain = M)

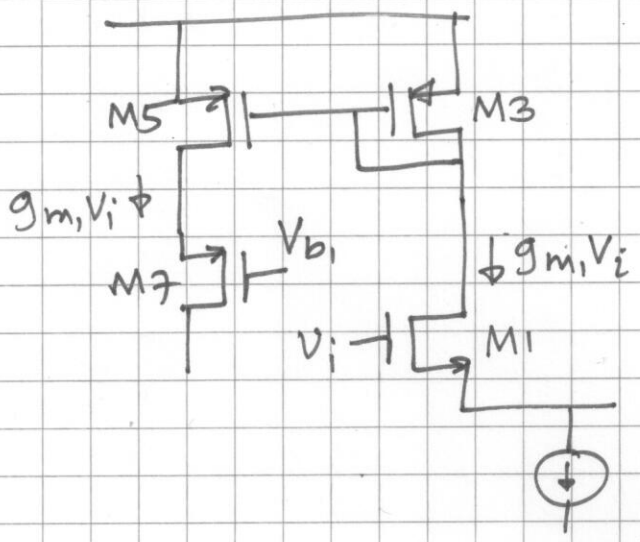
Low gain $\frac{g_m r_o}{2}$

Gain Improvement using cascodes.

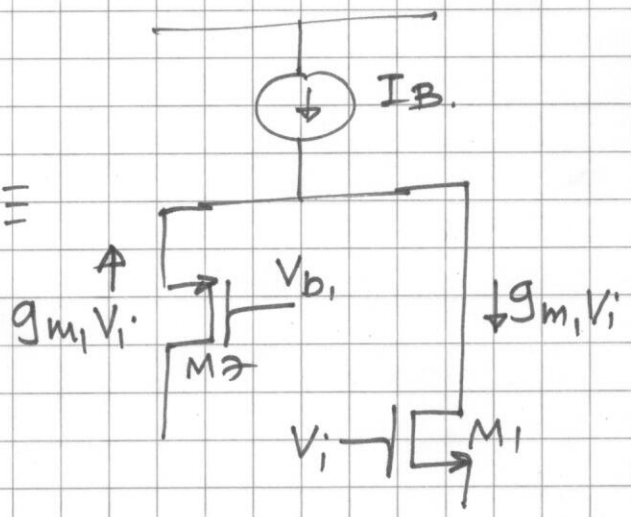


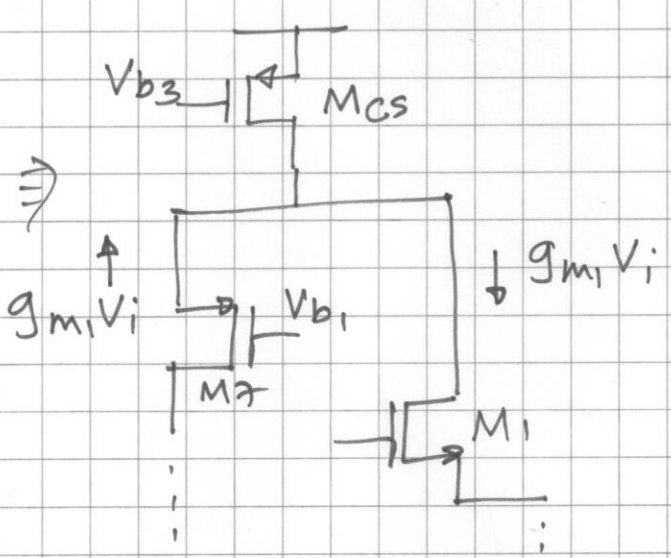
Gain $\frac{(g_m r_o)^2}{2}$.

Consider PMOS mirror



≡



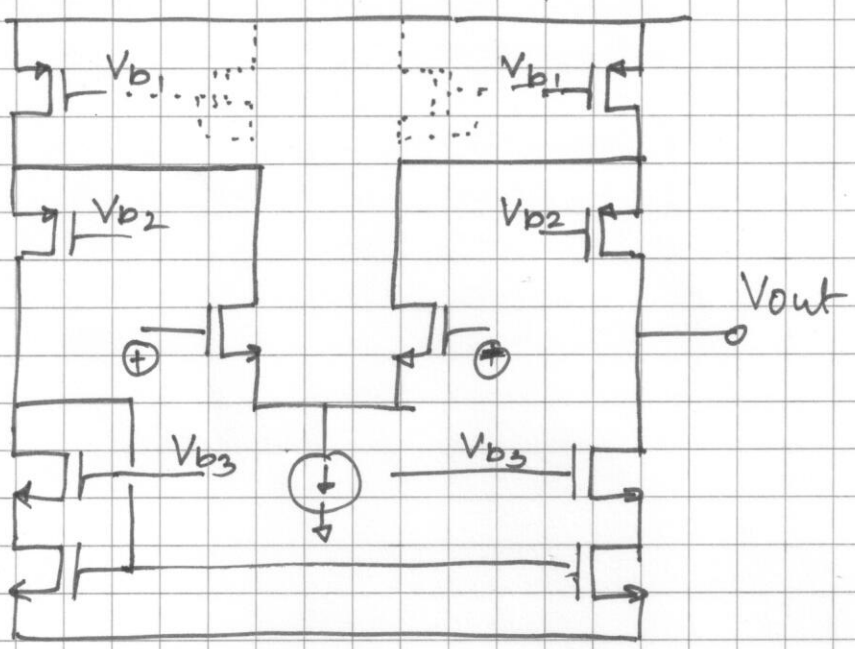


Signal Current flows to o/p. only sign change

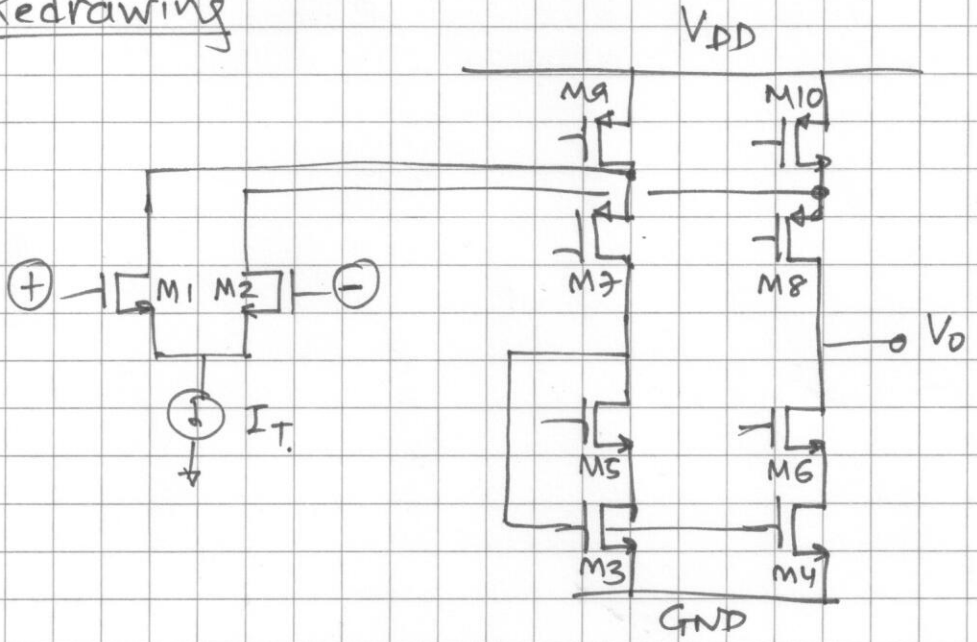
Key Concept of folded Cascode opamp

Avoid Mirror pole. M3/M5 & M4/M6

Folded Cascode OPAMP



Redrawing



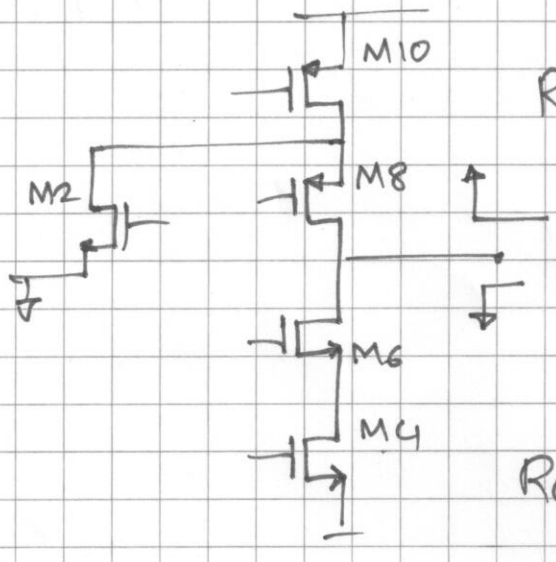
Advantage – No stacking of cascode on top of i/p. devices.

Large o/p swing ($V_{DD} - 4V_{dsat}$)

Calculate gain How?

Short o/p to DC ⇒ $G_m = g_m$,

Output impedance $\underline{R_{out}}$.



$$R_{out\uparrow} = g_{m8} r_{o8} \left[r_{o10} \parallel r_{o2} \right]$$

$$R_{out\downarrow} = (g_{m6} \cdot r_{o6}) r_{o4}$$

$$R_{out} = R_{out\uparrow} \parallel R_{out\downarrow}$$

$\parallel$ impedances Lets use g.

$$g_{out\uparrow} = \frac{(g_{ds2} + g_{ds10})}{g_{m8} \cdot r_{o8}}$$

$$g_{out\downarrow} = \frac{g_{ds4}}{g_{m6} \cdot r_{o6}}$$

diff pair

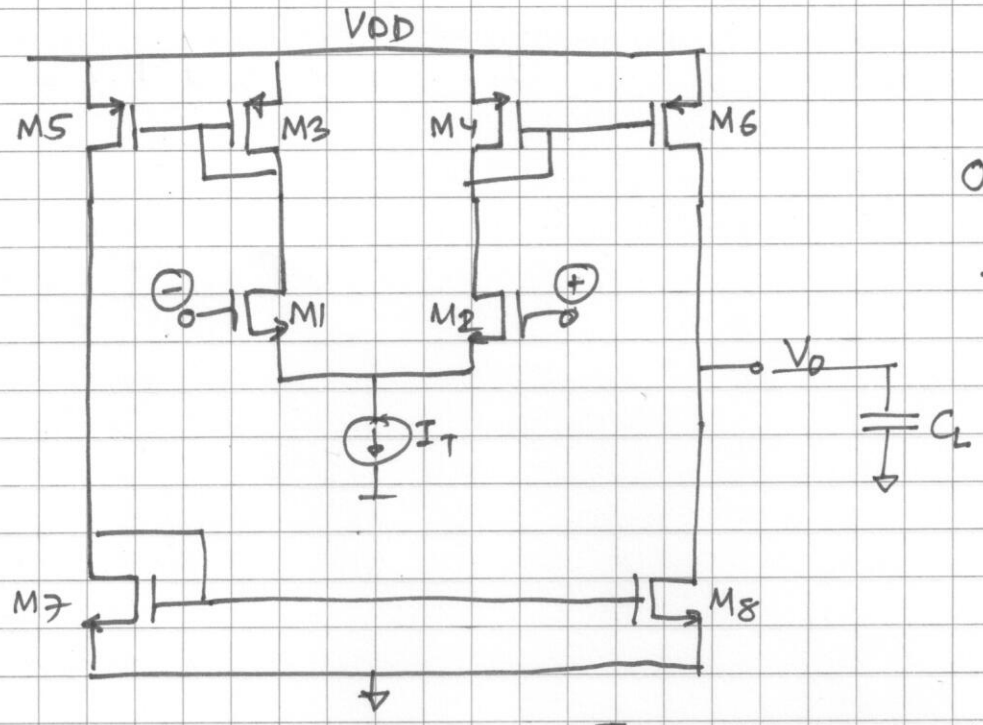
$$Gain = \frac{G_m}{g_{out}} = \frac{g_{m1} \cdot}{\frac{(g_{ds2} + g_{ds10})}{g_{m8} r_{o8}} + \frac{g_{ds4}}{g_{m6} \cdot r_{o6}}}$$

Extreme Simplification all g_ms equal. all g_{ds} equal.

$$Gain = \frac{g_m}{\frac{2g_{ds}}{g_m r_o} + \frac{g_{ds}}{g_m r_o}} = \frac{g_m}{3g_{ds}} \cdot g_m r_o$$

$$= \frac{1}{3} (g_m r_o)^2.$$

OPAMP using current mirrors



Output pole dominant - unloaded may become unstable.

Slew rate $= \frac{I_T}{C_L}$ (if all mirrors are unity gain)

$= M \frac{I_T}{C_L}$ (Mirror gain = M)

Low gain $\frac{g_m r_o}{2}$

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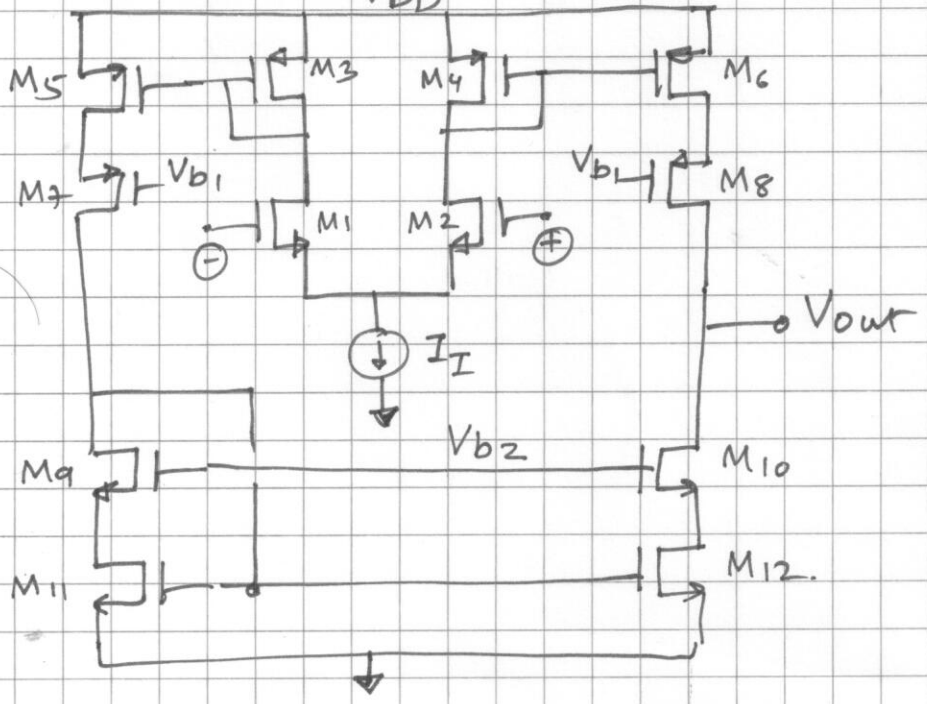
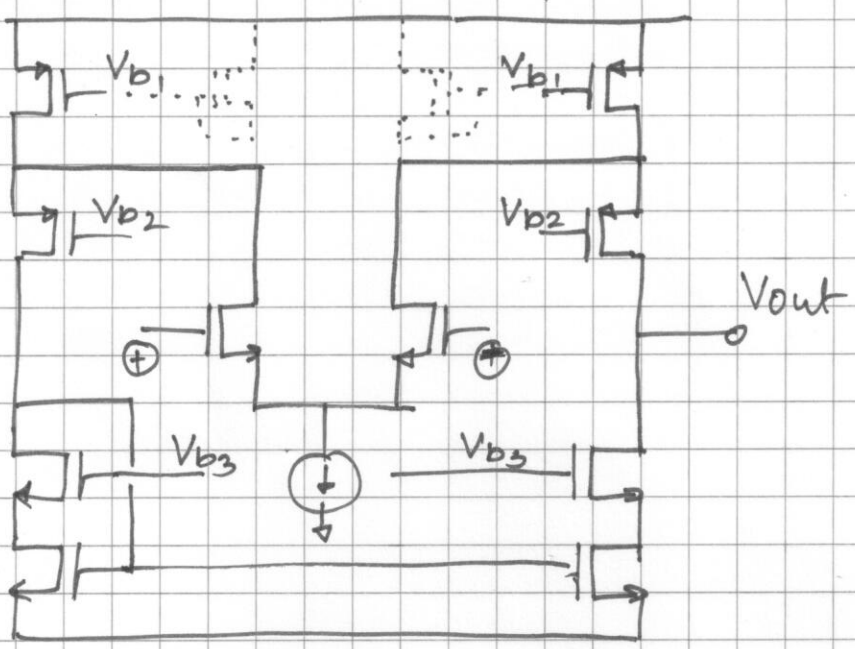
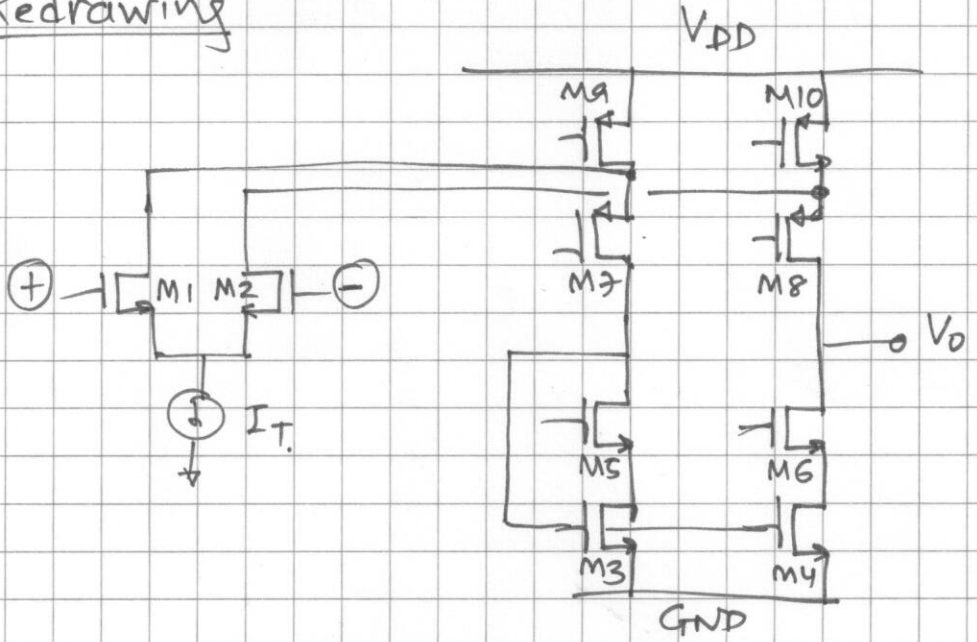


Gain $\frac{(g_m r_o)^2}{2}$.

Folded Cascode OPAMP



Redrawing



Advantage – No stacking of cascode on top of i/p. devices.

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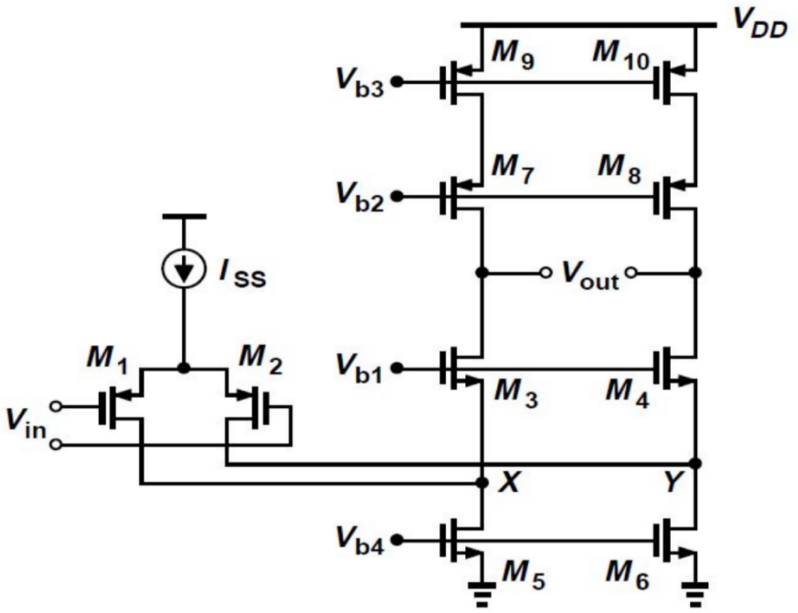
Calculate gain How?

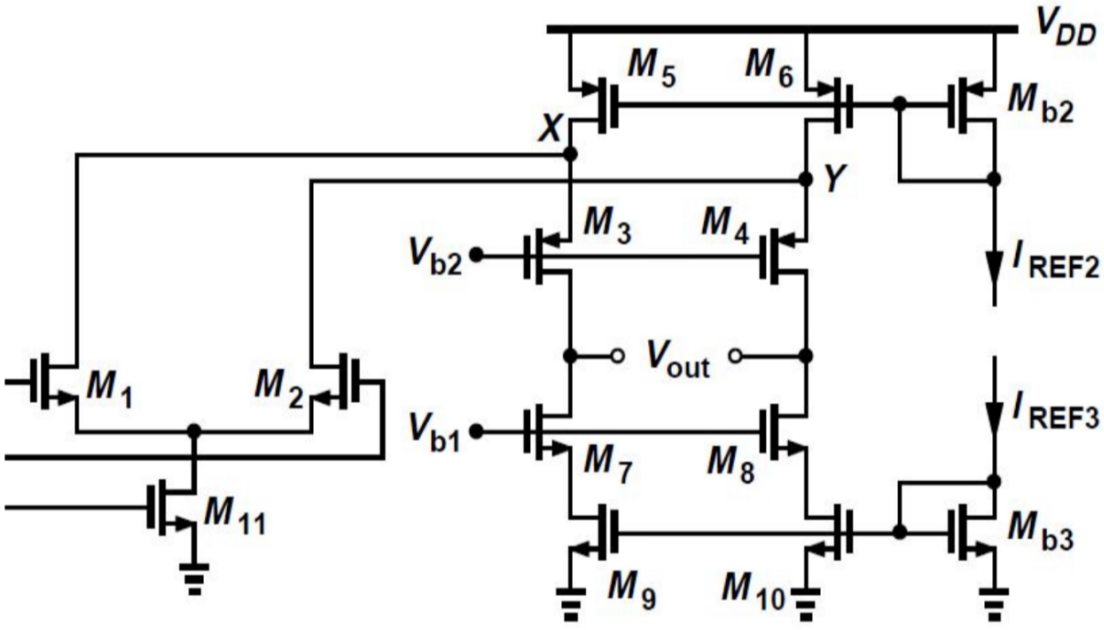
Short o/p to DC ⇒ $G_m = g_m$,

Folded cascode op amp with cascode PMOS load:



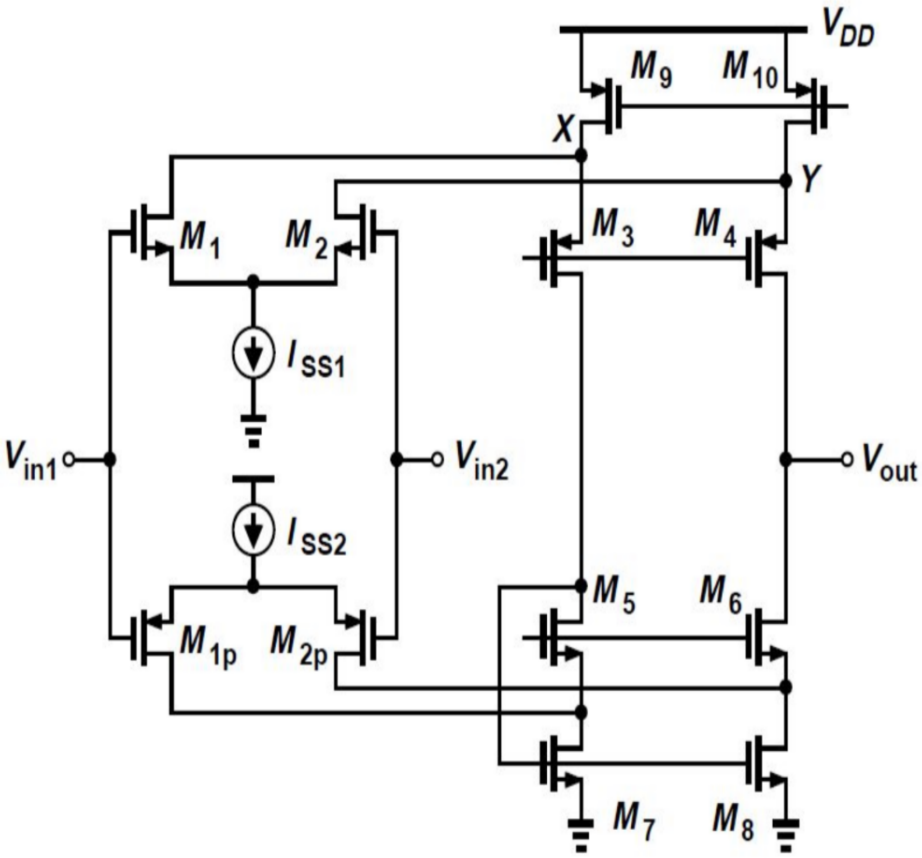
$V_{in,cm\ -\ range} => V_{DD}-(V_{Tp}+2V_{dsatp})$ to $V_{dsatn\ (previous\ stage)}$

Folded cascode op amp with cascode NMOS load:

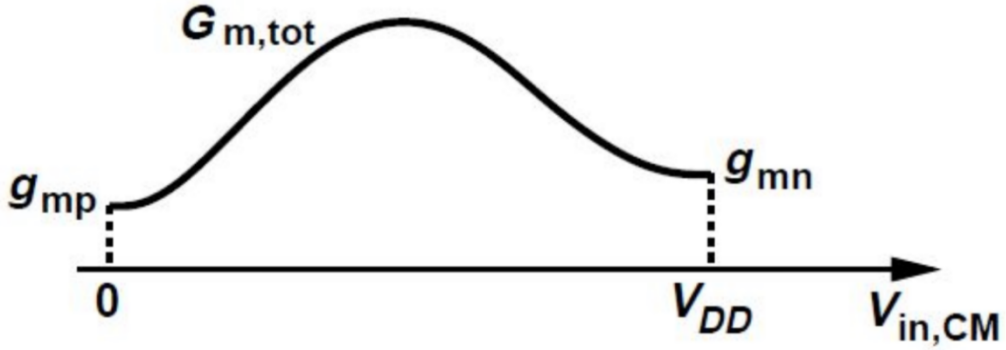


$V_{in,cm\ -\ range} => (V_{DD}- V_{dsatp\ (previous\ stage)})$ to $(V_{Tn}+2V_{dsatn})$

Extension of input common mode range:

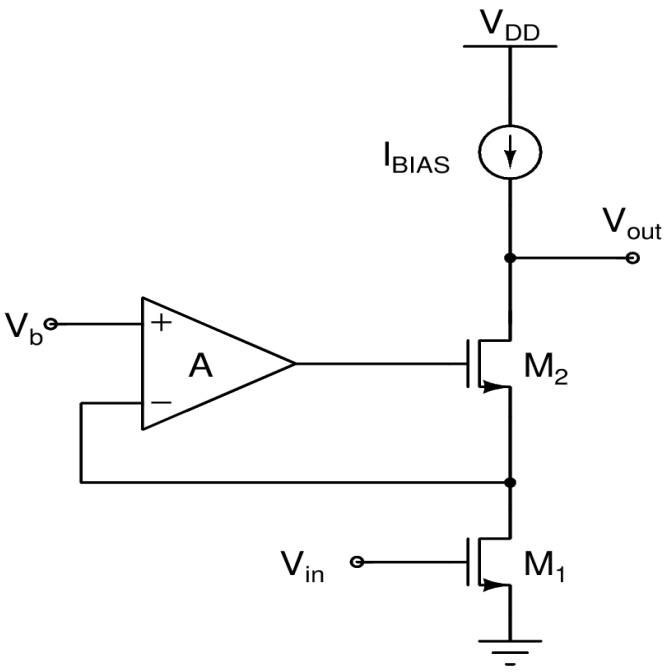


$$V_{\text{in, cm range}} = \sim V_{DD}$$



Reference: Design of Analog CMOS Integrated Circuits- B. Razavi. Chapter 9

Gain Boosting



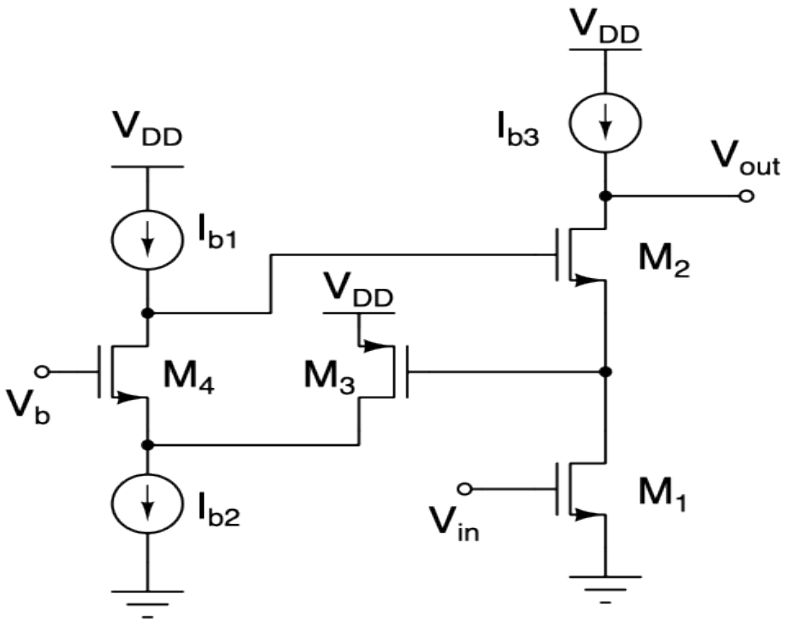
$$G_m = g_{m1}$$

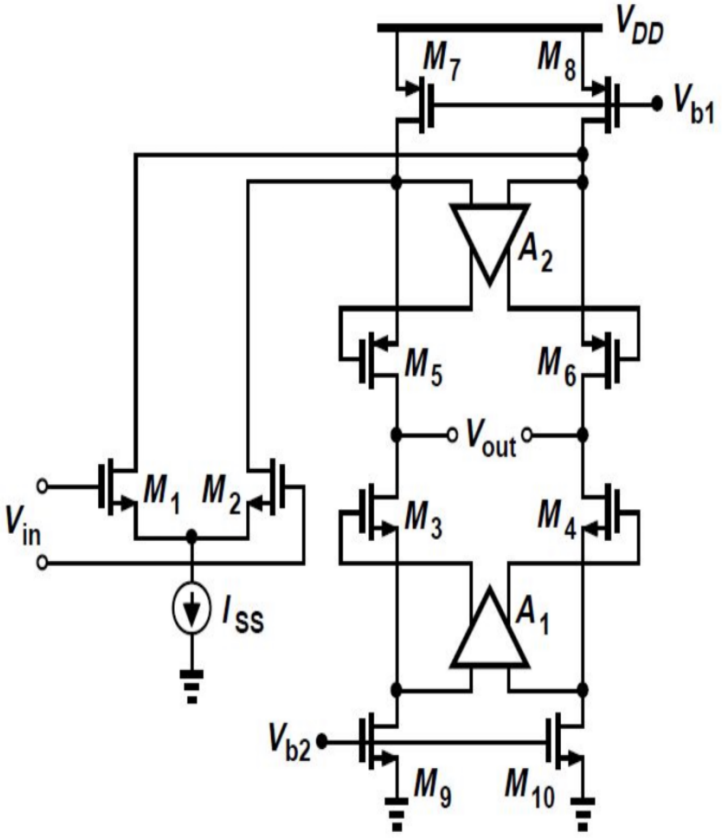
$$R_{out} = r_{o1} g_{m2} r_{o2} .(A+1)$$

$$\text{Gain} = g_{m1} r_{o1} g_{m2} r_{o2} .(A+1)$$

Reference: Klaas Bult JSSC – Dec 1990 pp. 1379 : Gain Boosting with Fast Settling

Implementation:





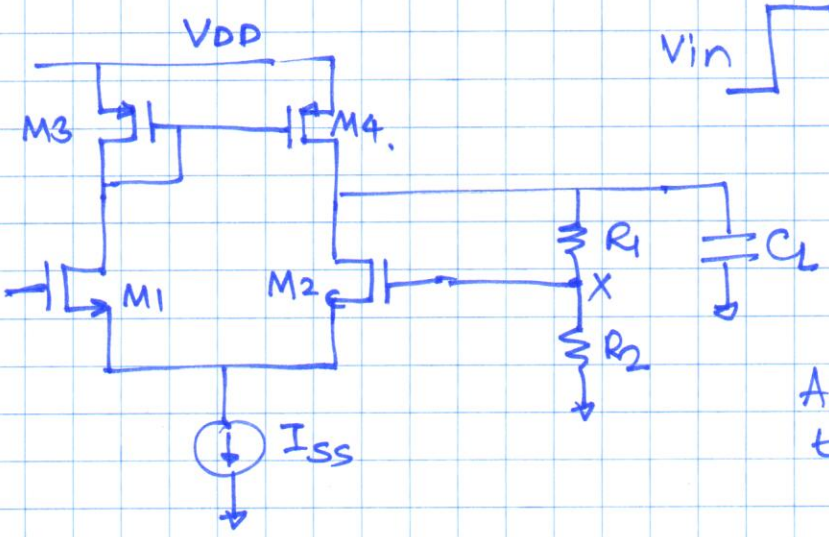
$$A = g_{m3} r_{o3} \frac{g_{m4} r_{o4}}{3}$$

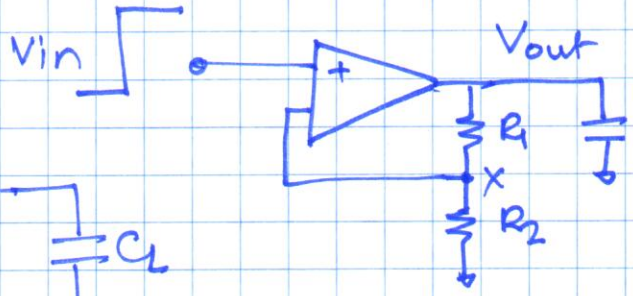
Slew Rate – Revisited

— large signal behavior Non-Linear

— fastest change in the node voltage.
decided by $\frac{I}{C} = \frac{dV}{dt}$

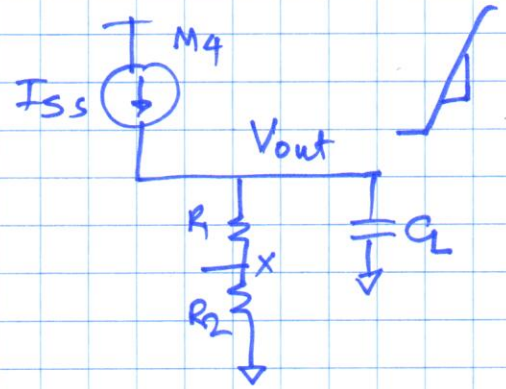
Consider single stage OTA





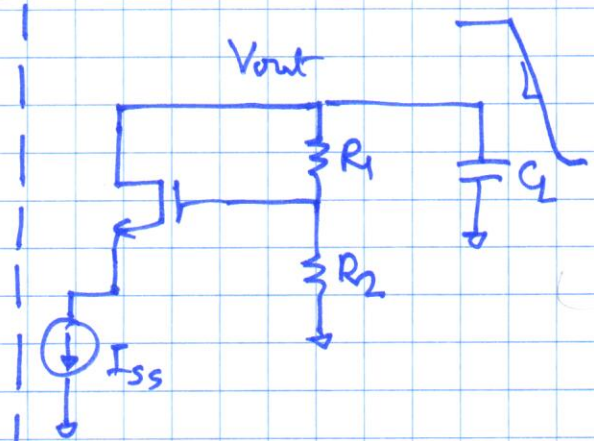
Assume $R_1 + R_2$ large to neglect current through

When ⌐ Vin step is applied,



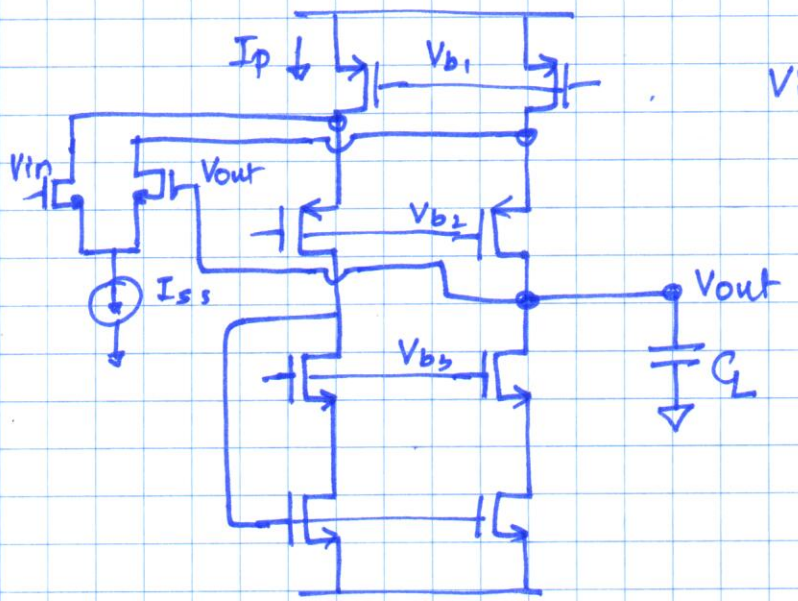
+ve slew rate = $\frac{I_{ss}}{C_L}$

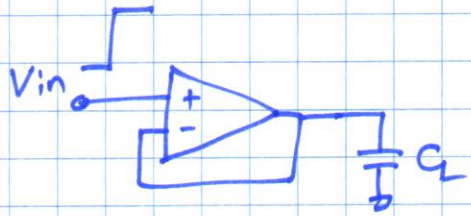
When ⌐ vin applied,



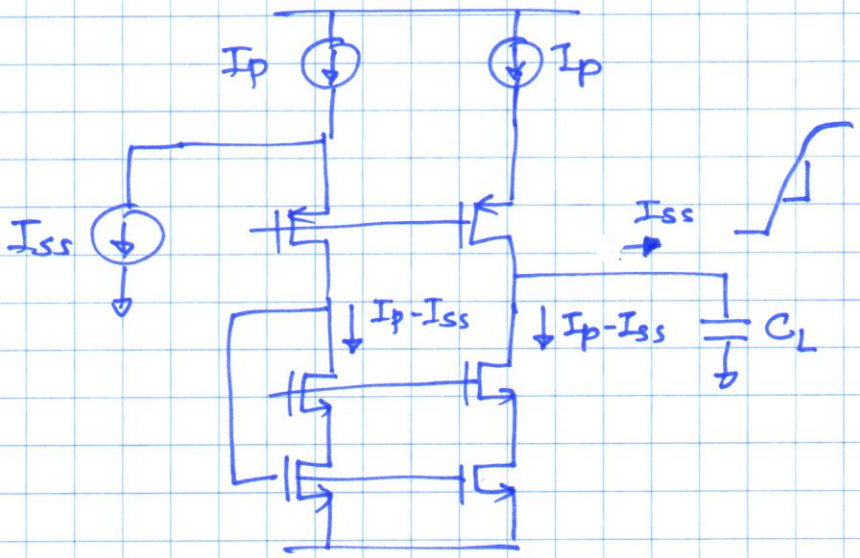
-ve slew rate = $\frac{I_{ss}}{C_L}$

Folded Cascode Opamp



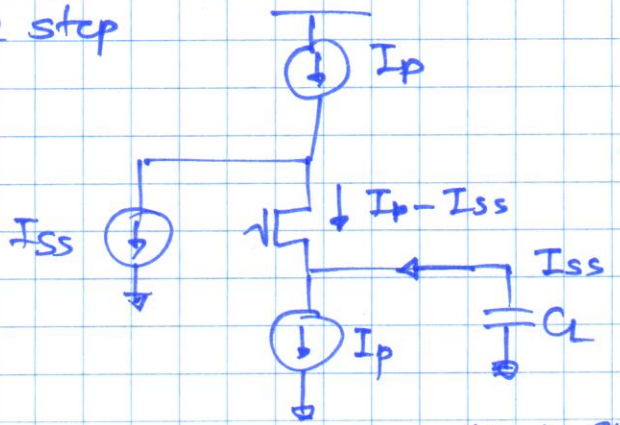


+ve step



+ve slew rate $= \frac{I_{ss}}{C_L}$

-ve step

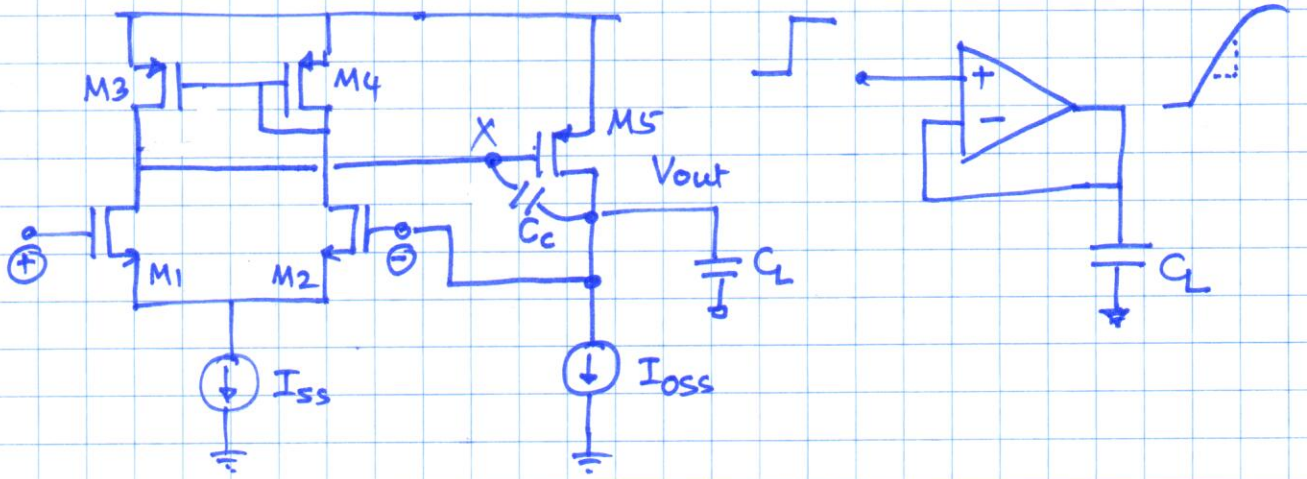


-ve slew rate $= \frac{I_{ss}}{C_L}$

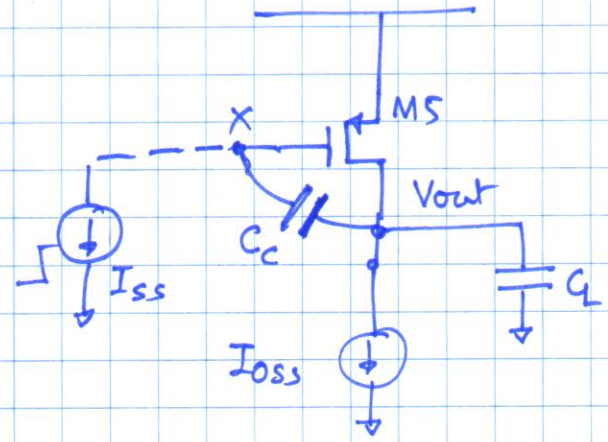
Keep $I_p = I_{ss}$ atleast

Else Slew rate limited to I_p/C_L I

Two stage op-amps slew rate.



+ve i/p step



Node x virtual gnd due to gain of M5.

$$\frac{dV_{out}}{dt} = \frac{I_{ss}}{C_c}$$

Current thru. $C_L = C_L \cdot \frac{dV_{out}}{dt}$

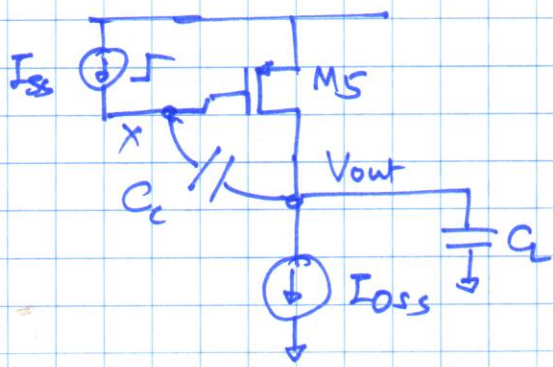
$$= \frac{C_L}{C_c} \cdot I_{ss}$$

M5 must support & stay in sat.

$$\left(I_{ss} + \frac{C_L}{C_c} I_{ss} + I_{oss}\right)$$

Slew rate = $\frac{I_{ss}}{C_c}$

-ve i/p step



$$\frac{dV_{out}}{dt} = \frac{I_{ss}}{C_c} \quad \text{(slew rate)}$$

if. $I_{oss} \geq I_{ss} + \frac{C_L}{C_c} I_{ss}$

Slew rate if $I_{oss} < I_{ss}\left(1 + \frac{C_L}{C_c}\right)$

$$= \frac{(I_{oss} - I_{ss})}{C_L}$$ | M5 off

How to increase slew rate?

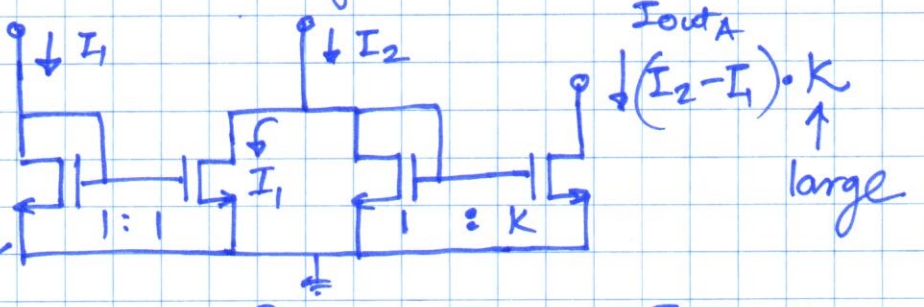
→ ↑ I_T → Increase in Quiescent Power

→ increase I_T only when large i/p voltage step applied.

→ Adaptively Biased opAMP. JSSC - JUNE 82

REFERENCE : ADAPTIVE BIASING CMOS AMP - DEGRAUWE

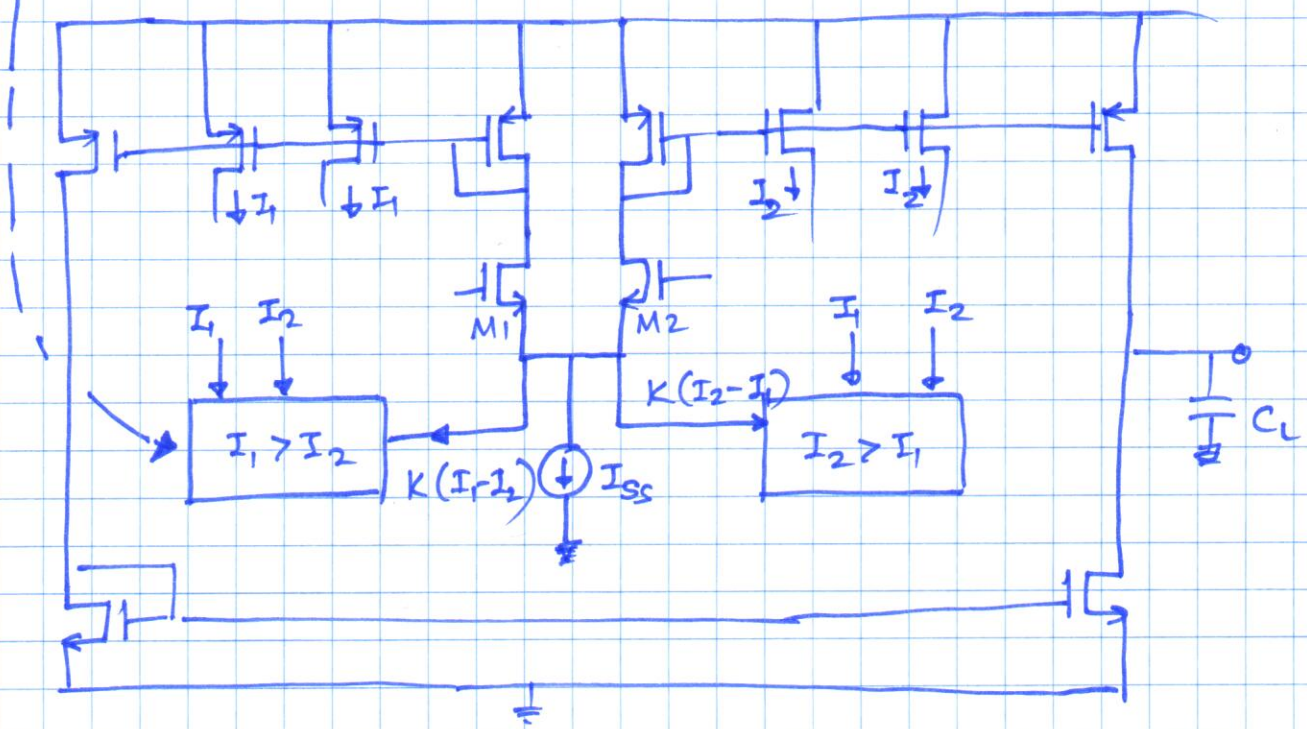
Consider following current mirror based circuit

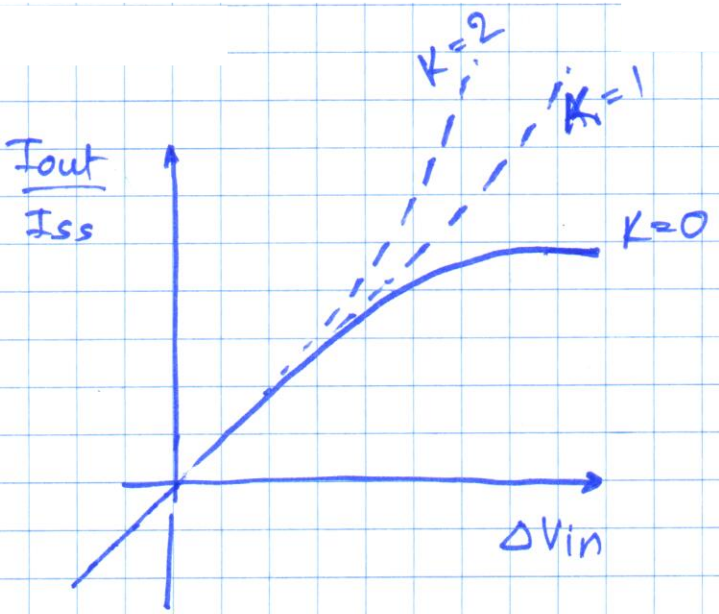


⇒ when $I_1 = I_2$ → $I_{out_A} \cong 0$

when $I_2 \gg I_1$ → $I_{out_A} = \underbrace{K(I_2 - I_1)}_{\text{large current}}$

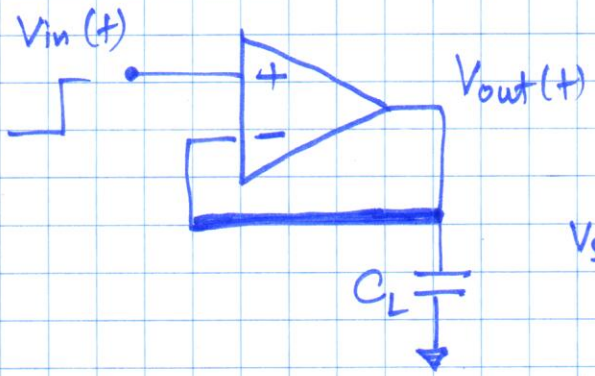
$I_2 < I_1$ → off. $I_{out_A} = 0$

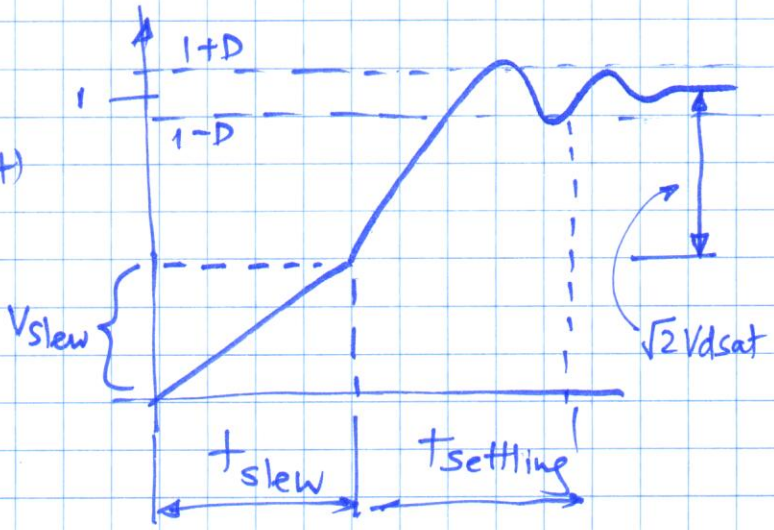




✡ Settling Time — Small-signal

Consider





Excellent Reference

Considerations for fast Settling Amplifiers

Howard Yang, Allstot —

IEEE Tran. CAS March 90

(from Allstot Notes)

Consider Opamp with single pole response. $a(s) = \frac{a_0}{\left(1+\frac{s}{p_1}\right)}$

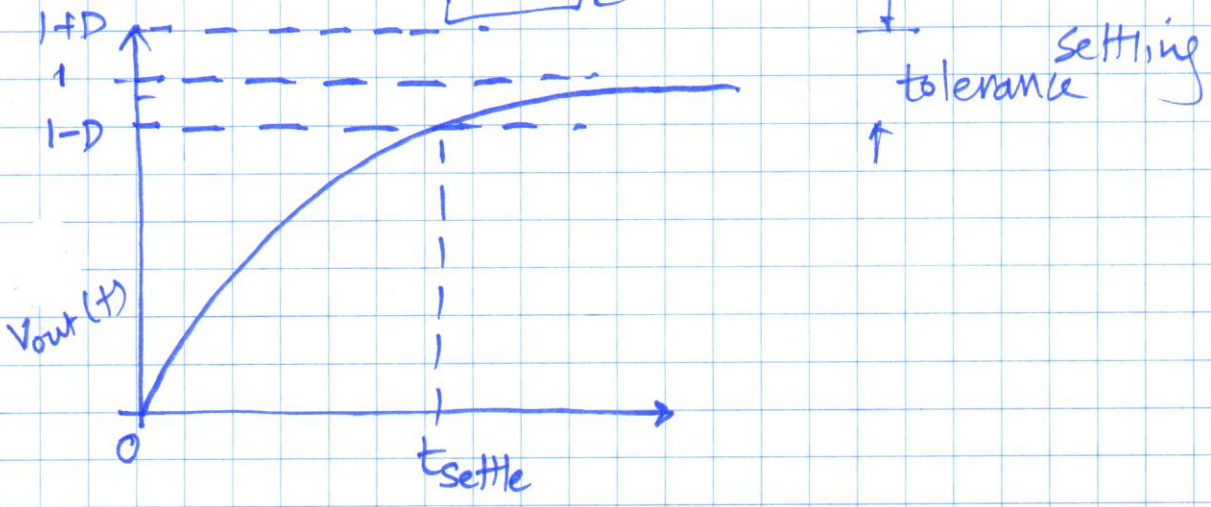
$$A(s) = \frac{a(s)}{1+a(s)} = \frac{a_0 p_1}{s + p_1(a_0+1)}$$

For unit step $V_{in}(s) = \frac{1}{s}$

$$V_{out}(s) = A(s) V_{in}(s) = \frac{a_0}{a_0+1}\left[\frac{1}{s} - \frac{1}{s+p_1(a_0+1)}\right]$$

Time domain ($\frac{a_0}{a_0+1} \to \sim 1$)

$$V_{out}(t) = \left[\frac{a_0}{a_0+1}\right]\left[u(t) - e^{-p_1(a_0+1)t}\right]$$



τ = small-signal settling time constant

$$= \frac{1}{p_1(a_0+1)} \simeq \frac{1}{p_1 a_0} \simeq \frac{1}{\omega_u} \leftarrow \underline{\text{GBW}}$$

D (%)	$t_s = -\tau \ln D$	f_u
1 (6.64 bits)	4.61τ	73.4 MHz
0.01 (13.3 bits)	9.21τ	147 MHz
0.001 (16.6 bits)	11.51τ	183 MHz
0.0001 (20 bits)	13.82τ	220 MHz

for 100 MHz operation.

Example $D = 0.01\%$ $\quad 20\log(0.01/100)^{-1}$

$= 80\,dB$ SNR

$\Rightarrow \frac{80}{6} \Rightarrow$ 13.33 bits resolution

$t_s = -\tau \ln D = -\tau \ln(0.0001)$

$= 9.21\tau.$

we wish to settle in $\frac{1}{100MHz}$ time $= 10nS.$

$t_{settle} = 10ns = 9.21\tau.$

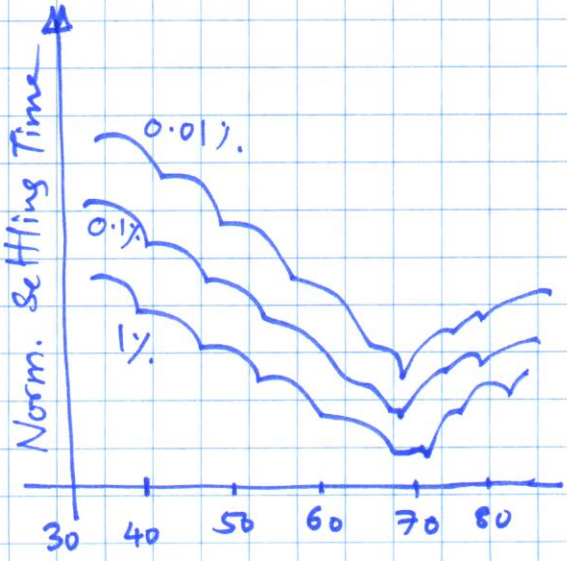
$\Rightarrow \tau = 1.0857\,nS.$

$f_u = \frac{1}{2\pi\tau} = 146.6\,MHz$

Yang paper describes Minimum Settling Time as a function of Phase margin. for two pole system

Note Phase Margin depends on relative positions of two poles.

$$a(s) = \frac{a_0}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)}$$



(from Allstot Notes)

Consider Opamp with single pole response. $a(s) = \frac{a_0}{\left(1+\frac{s}{p_1}\right)}$

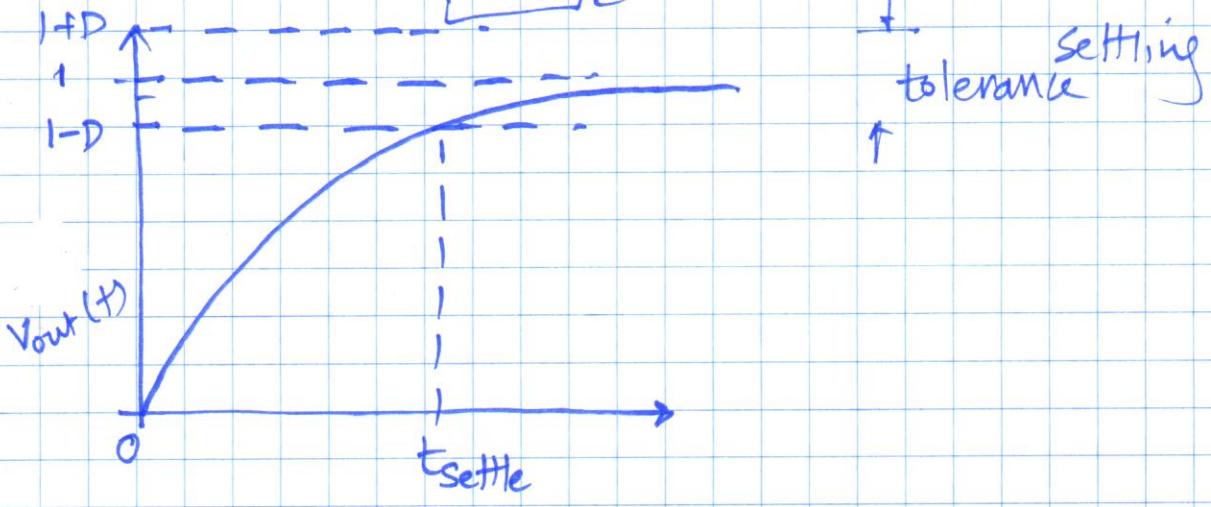
$$A(s) = \frac{a(s)}{1+a(s)} = \frac{a_0 p_1}{s + p_1(a_0+1)}$$

For unit step $V_{in}(s) = \frac{1}{s}$

$$V_{out}(s) = A(s) V_{in}(s) = \frac{a_0}{a_0+1}\left[\frac{1}{s} - \frac{1}{s+p_1(a_0+1)}\right]$$

Time domain ($\frac{a_0}{a_0+1} \to \sim 1$)

$$V_{out}(t) = \left[\frac{a_0}{a_0+1}\right]\left[u(t) - e^{-p_1(a_0+1)t}\right]$$



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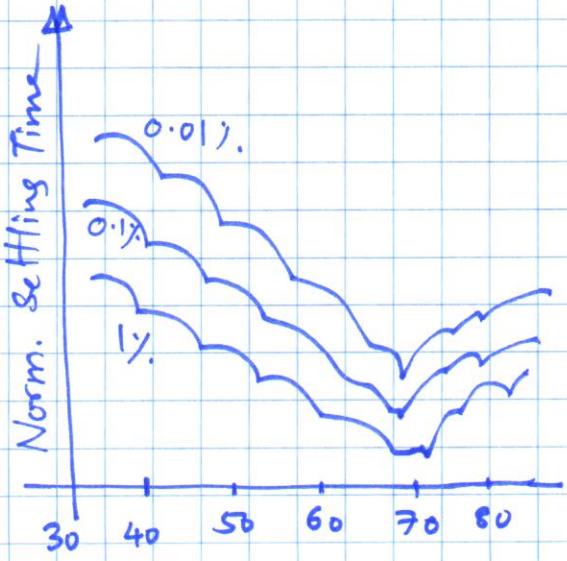
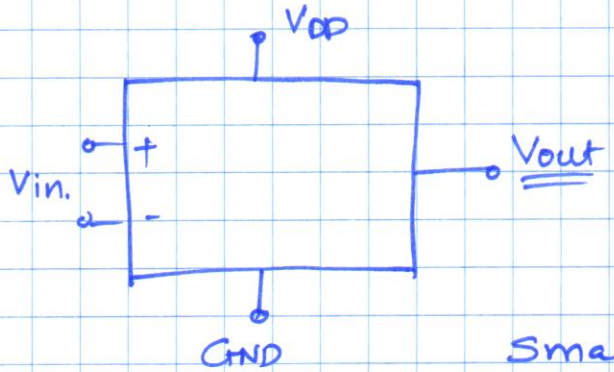


24 September 2019

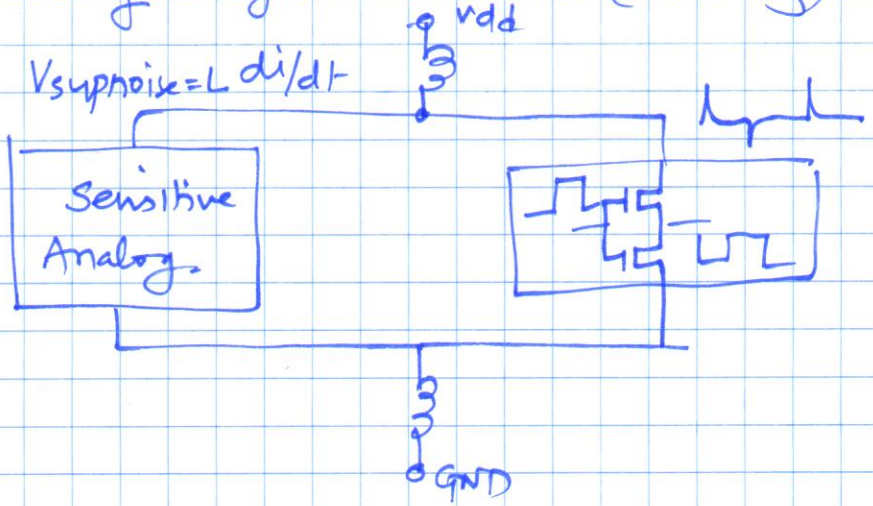
Power Supply Rejection Ratio PSRR



Supply noise either on Vdd or GND can leach into Vout - limiting smallest signal we can detect.

Source of Supply noise

* Off-chip noise electrically coupled through pins
* Noise of V_{DD} (regulators - switching power supplies)
* Noise coupled through V_{DD} / GND bondwires sharing digital circuits. (switching)

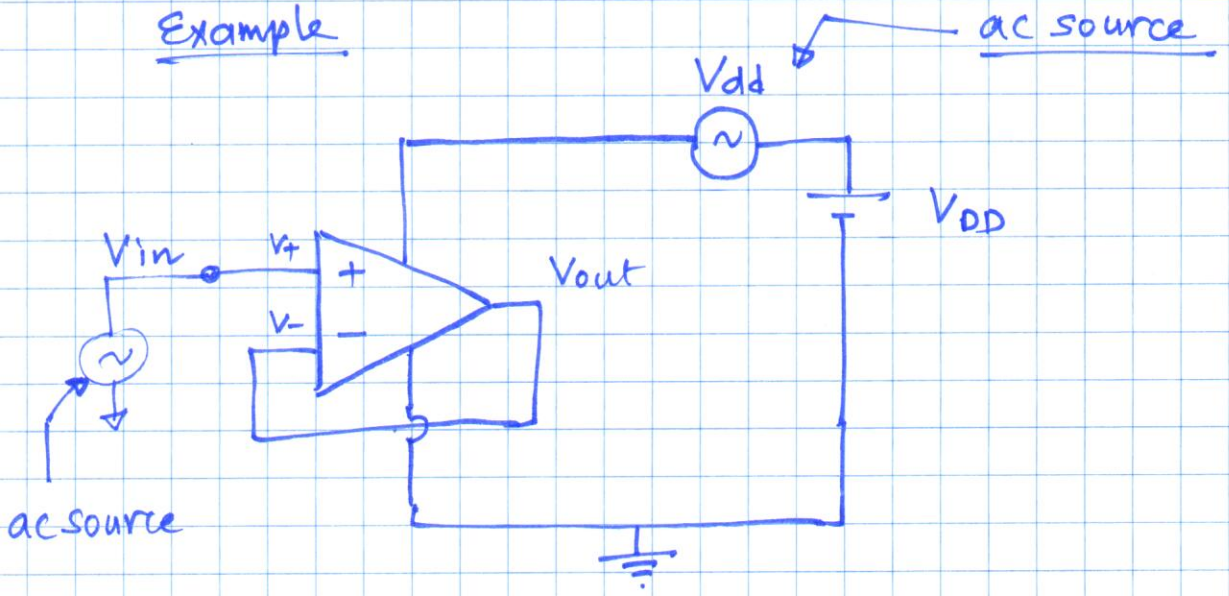


$$PSRR\ (definition) = \frac{A_{dm}\ (\sim V_{dd}\ or\ \sim GND = 0)}{A_{ps}\ (V_{in} = 0)}$$

A_{ps} = AC gain from Vdd or Gnd to Vout when $V_{in} = 0$.

Measuring PSRR

Example



To calculate gain from Vdd to Vout Vin = 0

$$V_{out} = A_{Ps\,Vdd} V_{dd} + A_{dm}(V_+ - V_-)$$

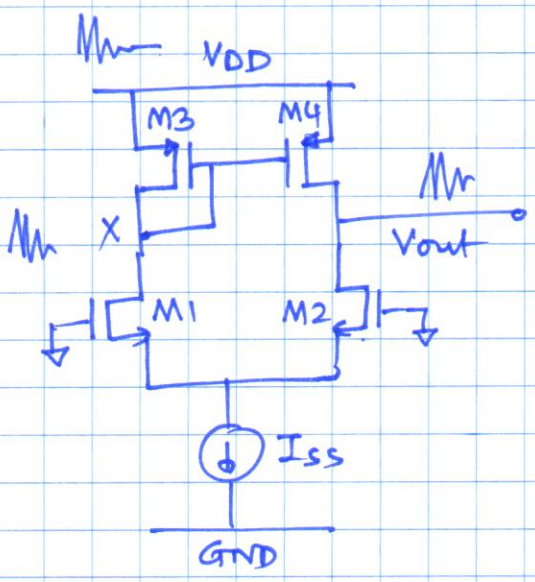
$$V_{out} = A_{Ps\,Vdd} V_{dd} + A_{dm}(0 - V_{out})$$

$$V_{out}(1 + A_{dm}) = A_{Ps\,Vdd} V_{dd}$$

$$\frac{V_{out}}{V_{dd}} = \frac{A_{Ps\,Vdd}}{(1 + A_{dm})} \cong \frac{A_{Ps\,Vdd}}{A_{dm}} = \frac{1}{PSRR}$$

Caution: During PSRR measurements, make sure all biasing circuits are included.

Insights on PSRR

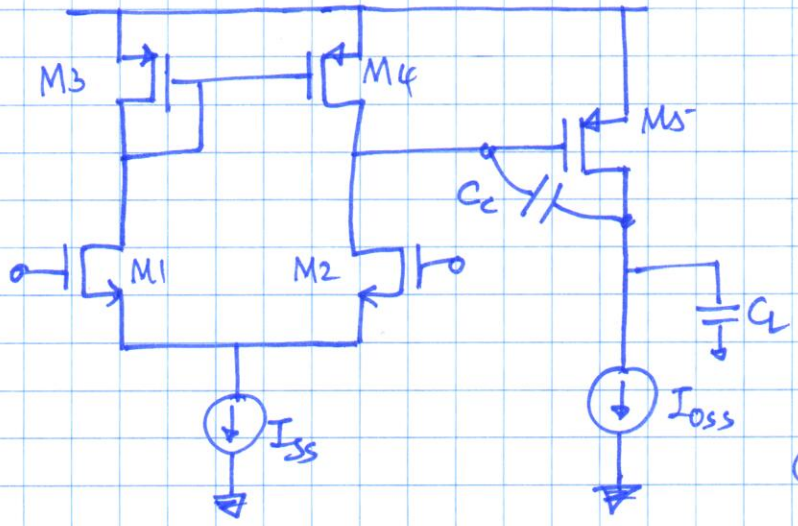


unity gain from V_{DD} to V_{out}

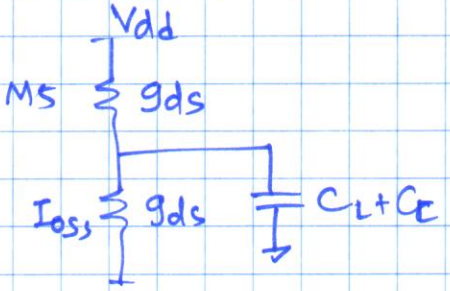
$$A_{PS_{VDD}} = 1$$

$$\therefore \text{PSRR} = \frac{g_{m_N} r_{out}}{1}$$

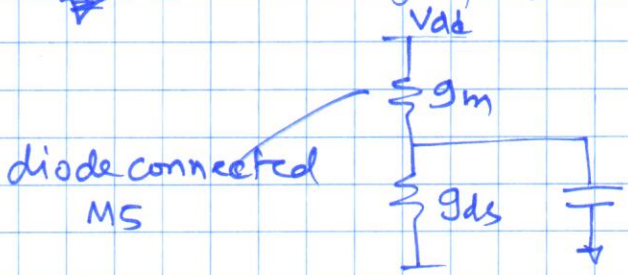
Two Stage OTA



@ Low frequency



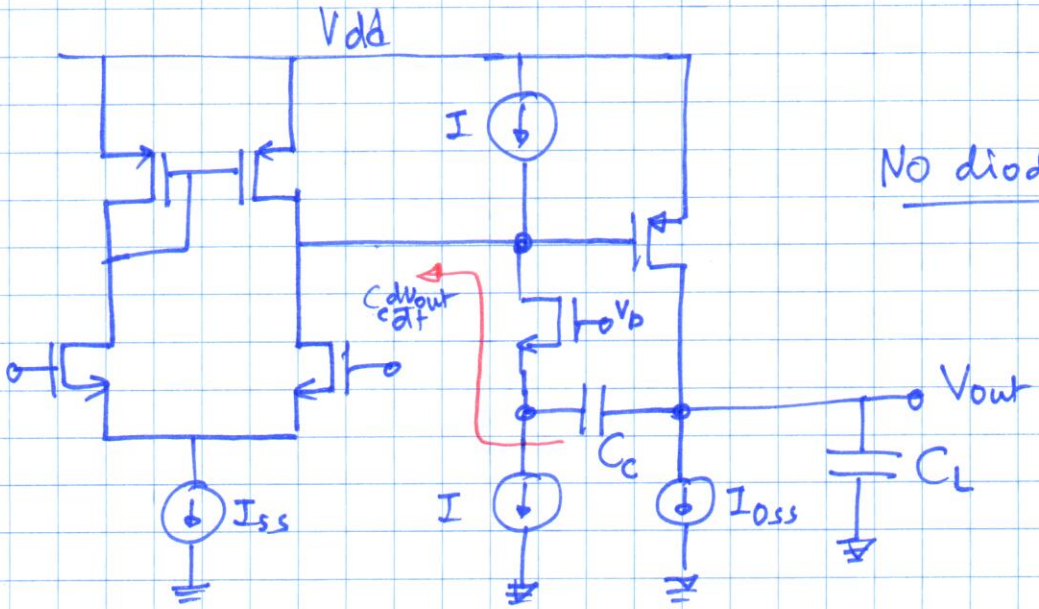
@ High frequencies



Poor PSRR @ High frequencies.

To improve High freq. PSRR — C_c decoupling from V_{dd}.

How?



No diode @ HF

ZELE EE618

LECTURE 14

24 September 2019

NOISE

Lecture Notes adapted from Chapter 7

B. Razavi (Design of Analog CMOS ICs)

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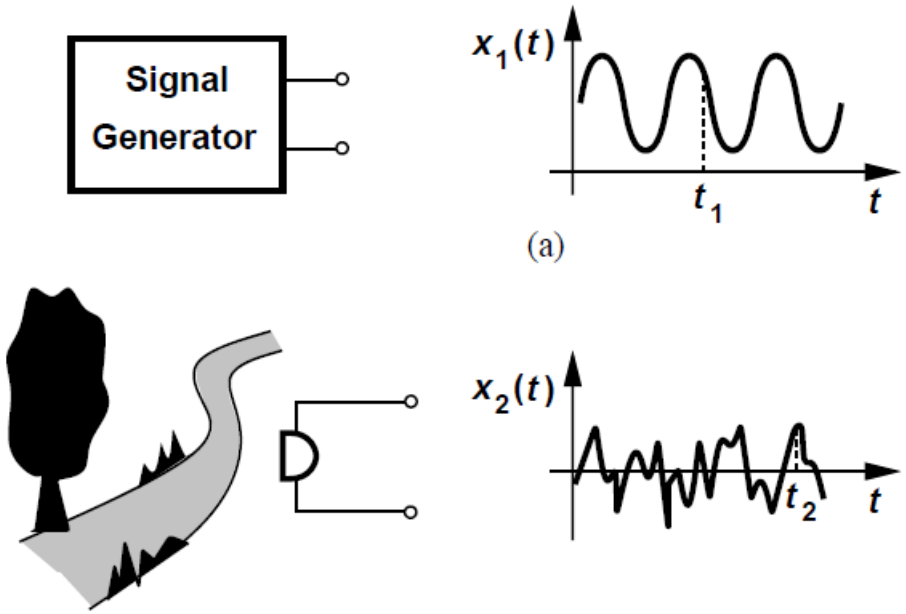
Statistical Characteristics of Noise



- **Noise - random process**
- **Noise is everywhere**
- ***$x_1(t_1)$ & $x_2(t_2)$* - Difference between deterministic and random**
- **Noise(t) unpredictable**
- **Noise can't be calibrated out**

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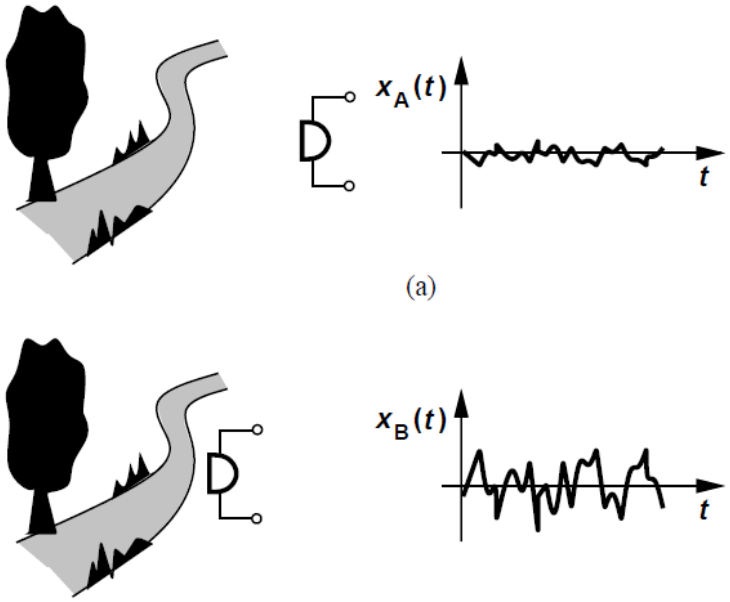
Statistical Characteristics of Noise



- **Average power of noise is predictable**
- **Average power delivered by a periodic voltage *v(t)* with period *T* to a load resistance R_L is defined as**

$$P_{av} = \frac{1}{T}\int_{-T/2}^{+T/2} \frac{v^2(t)}{R_L} dt$$

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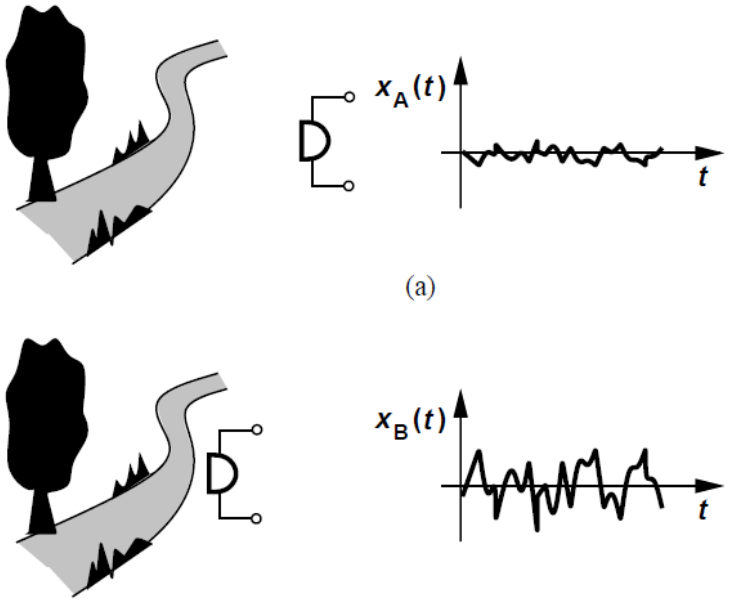
Statistical Characteristics of Noise



- **Random signal (aperiodic): measurement over a long time**

$$P_{av} = \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{+T/2} \frac{x^2(t)}{R_L} dt$$

- ***$x_B(t)$* delivers more power than *$x_A(t)$***

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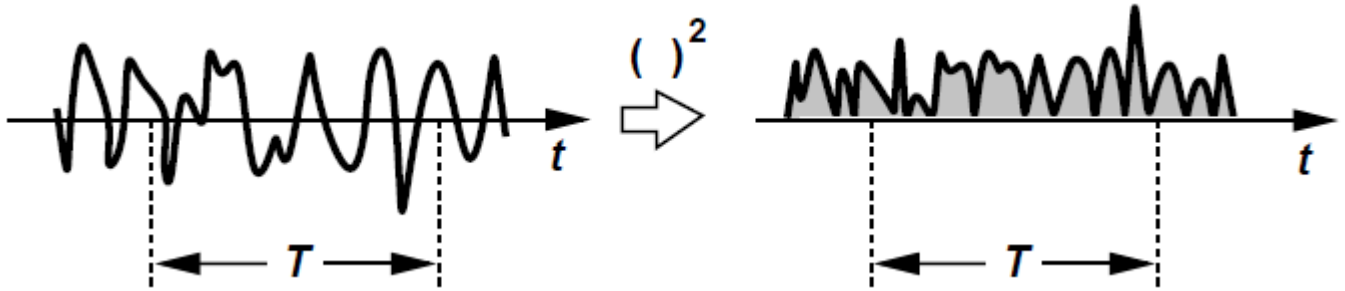
Statistical Characteristics of Noise

- To calculate average power of (noise) signal *x(t)*



- P_{av} is defined as

$$P_{av} = \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{+T/2} x^2(t)dt$$

- P_{av} is expressed in V^2 rather than *W*
- RMS voltage for noise can be defined as $\sqrt{P_{av}}$

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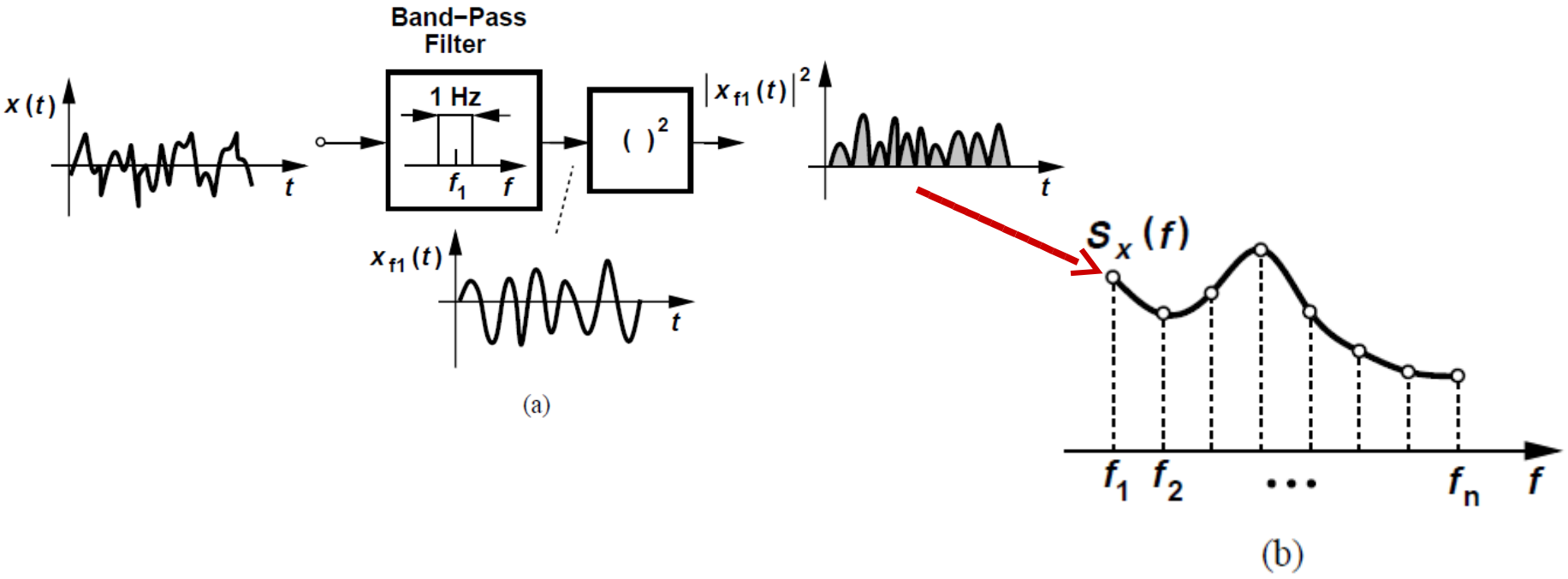
Noise Spectrum

- **Power Spectral Density (PSD) $S_x(f)$**
  - **signal power at each frequency**
- **$S_x(f)$ defined as the average power carried by $x(t)$ in a 1-Hz bandwidth around f**



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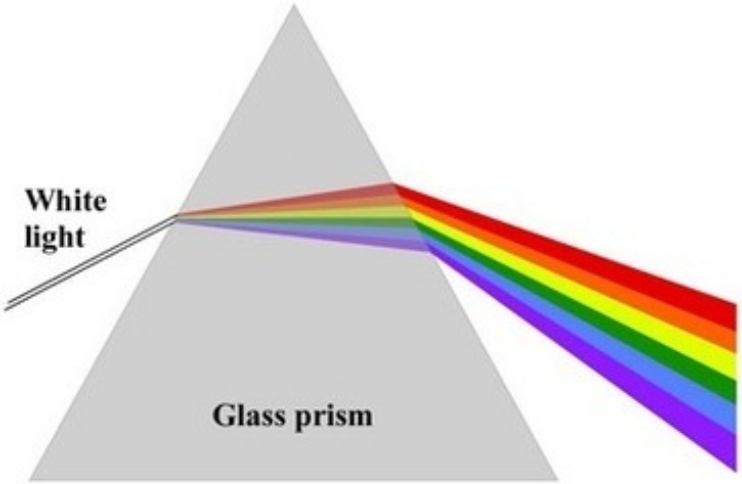
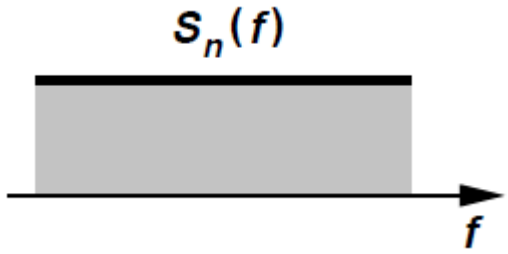
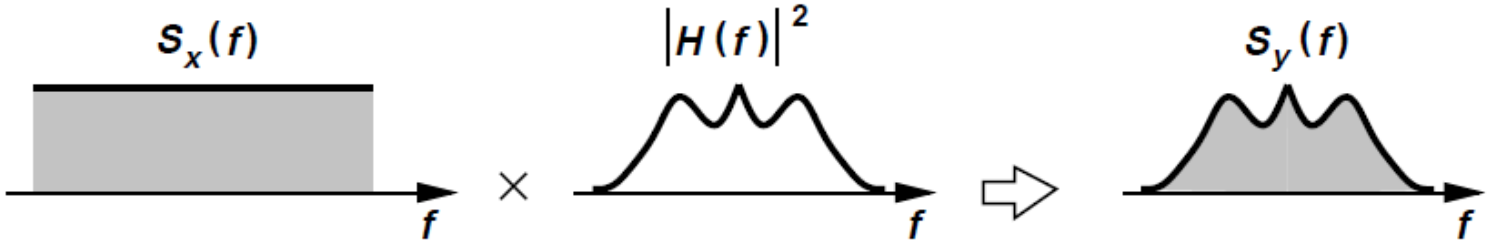
Noise Spectrum

- $S_x(f)$ -- V^2/Hz or $V/\sqrt{Hz}$
- **white noise PSD -- Noise spectrum that is flat *in the band of interest* is usually called white**



Color	λ (nm)	Freq (Hz)
Red	760-647	4.3×10^{14}
Orange	647-585	4.3×10^{14}
Yellow	585-575	5.2×10^{14}
Green	575-491	5.6×10^{14}
Blue	491-424	6.6×10^{14}
Violet	424-380	7.3×10^{14}





$$S_Y(f) = S_x(f)|H(f)|^2$$

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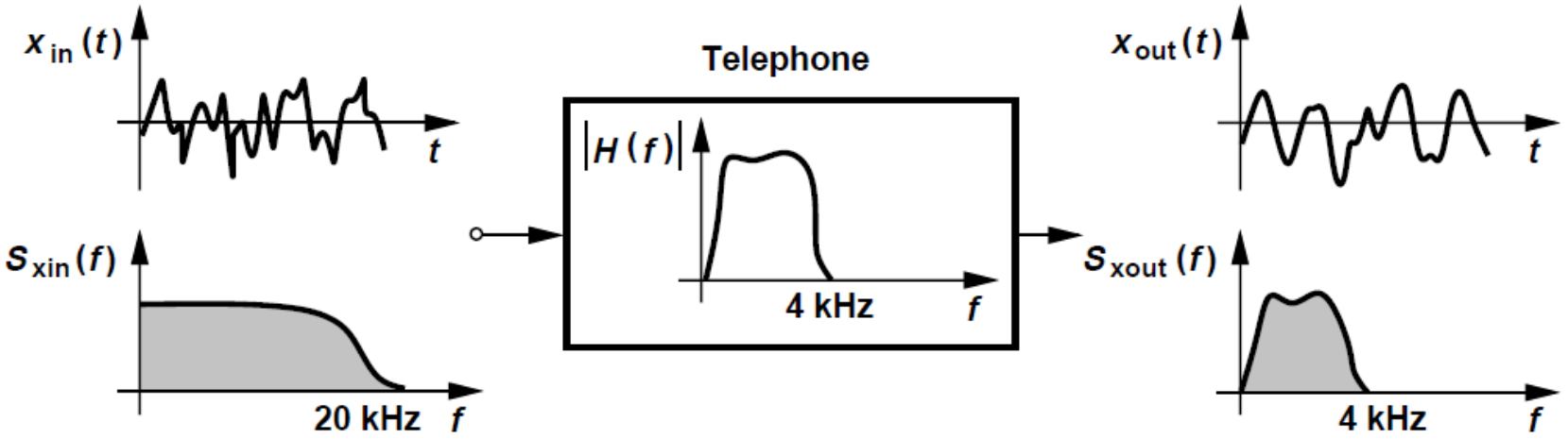
Telephone Example



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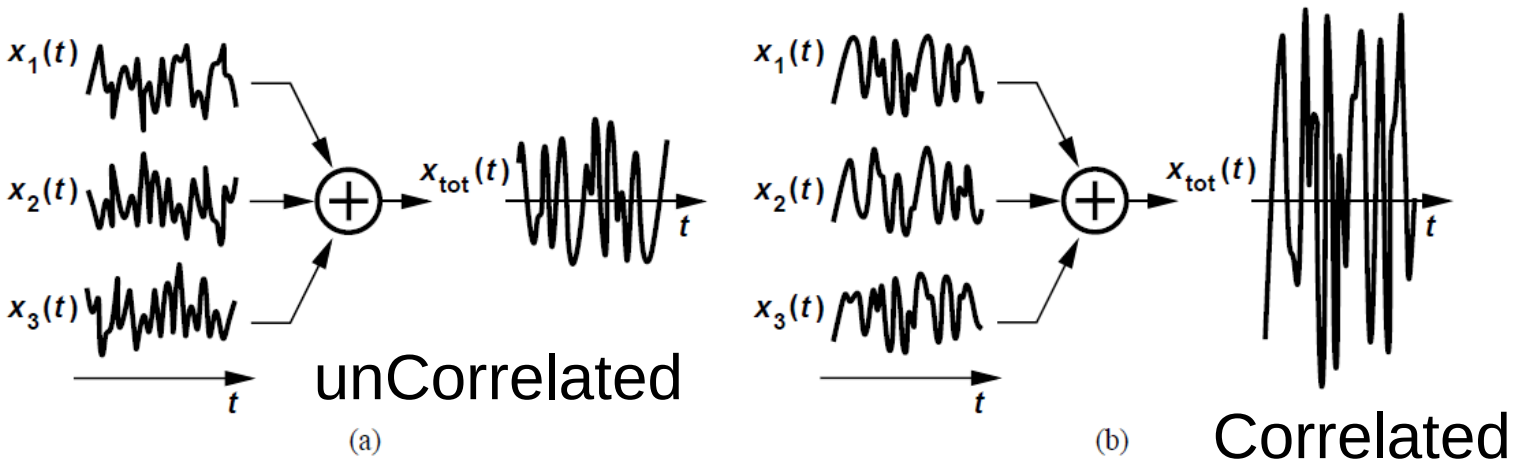
Correlated vs Uncorrelated Sources

- **Superposition Principle not suitable for random noise signals**
- **Average noise power**

$$
\begin{aligned}
P_{av} &= \lim_{T\to\infty}\frac{1}{T}\int_{-T/2}^{+T/2}[x_1(t)+x_2(t)]^2dt \\
&= \lim_{T\to\infty}\frac{1}{T}\int_{-T/2}^{+T/2}x_1^2(t)dt + \lim_{T\to\infty}\frac{1}{T}\int_{-T/2}^{+T/2}x_2^2(t)dt \\
&\quad + \lim_{T\to\infty}\frac{1}{T}\int_{-T/2}^{+T/2}2x_1(t)x_2(t)dt \\
&= P_{av1} + P_{av2} + \lim_{T\to\infty}\frac{1}{T}\int_{-T/2}^{+T/2}2x_1(t)x_2(t)dt,
\end{aligned}
$$

correlation

Stadium Noise



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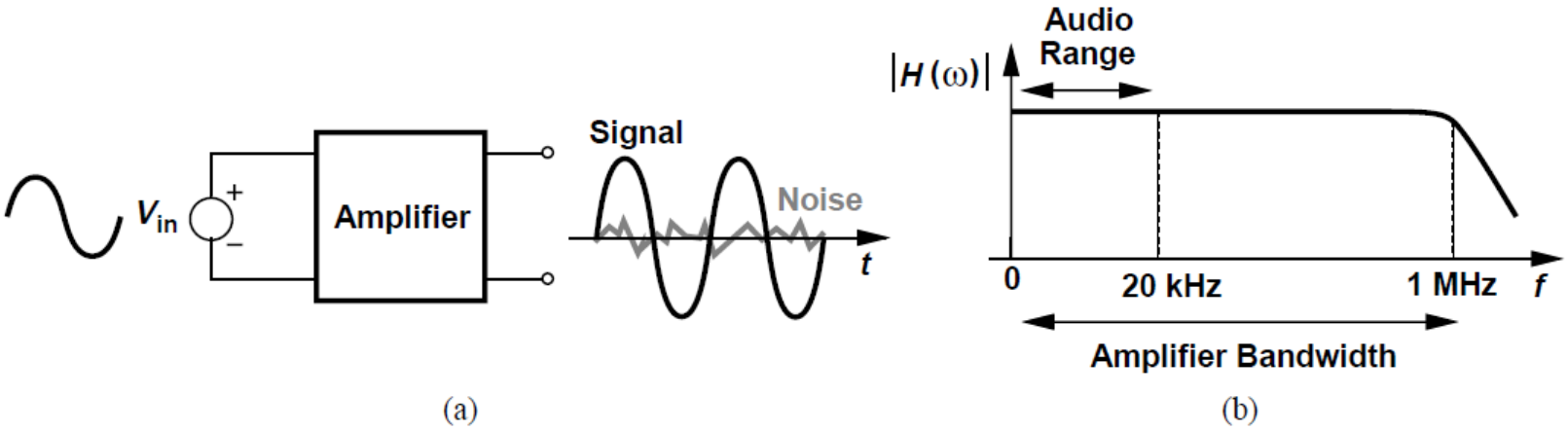
Signal-to-Noise Ratio (SNR)

- **SNR – intelligibility of the signal**

$$\text{SNR} = \frac{P_{sig}}{P_{noise}}$$

- **For a sinusoid with peak amplitude *A*, $P_{sig} = A^2/2$**
- **Noise Power**

$$P_{noise} = \int_{-\infty}^{+\infty} S_{noise}(f)\,df.$$



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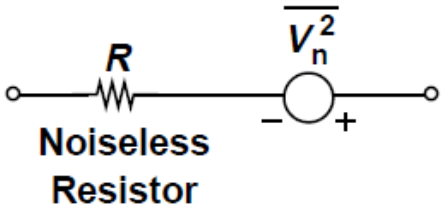
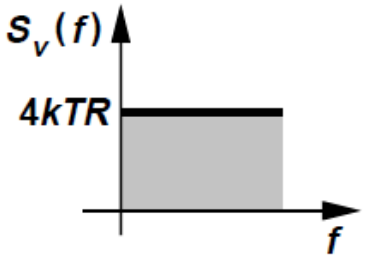
Resistor Thermal Noise

- **Random motion of electrons in a conductor induces fluctuations in the voltage measured across it even though the average current is zero**





$$S_v(f) = 4kTR, \quad f \geq 0$$

$$\overline{V_n^2} = 4kTR$$

- ***k*** **= 1.38 X 10^{-23} J/K is the Boltzmann constant**
- **1000 Ω (300 K) → 16 X 10^{-18} *V^2/Hz*, or 4 nV/√Hz**

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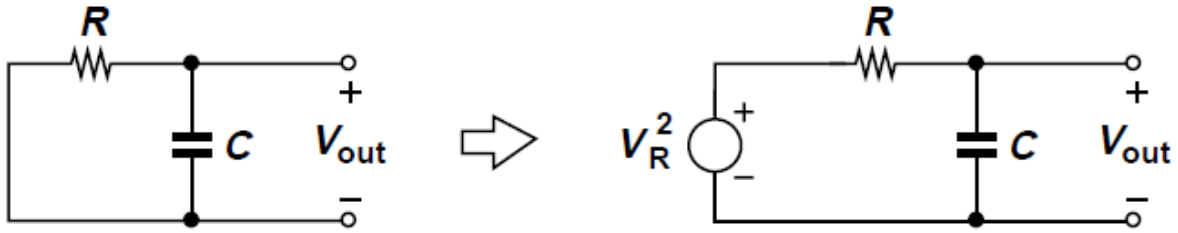
Resistor Thermal Noise: Example



Noise spectrum and total noise power in V_{out}

$$\frac{V_{out}}{V_R}(s) = \frac{1}{RCs+1}$$

$$P_{n,out} = \int_0^\infty \frac{4kTR}{4\pi^2R^2C^2f^2+1}df$$

$$S_{out}(f) = S_v(f)\left|\frac{V_{out}}{V_R}(j\omega)\right|^2$$

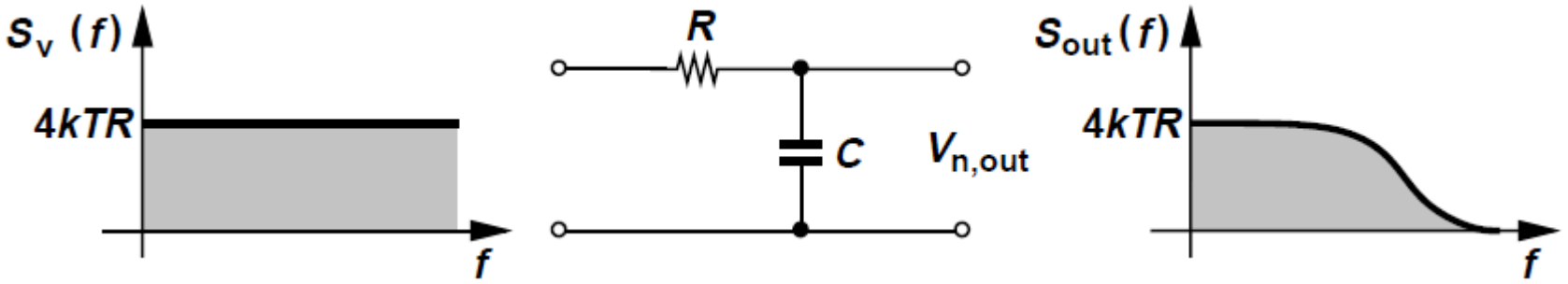
$$= 4kTR\frac{1}{4\pi^2R^2C^2f^2+1}$$

$$Put\ 2\pi RCf = u$$

$$P_{n,out} = \frac{2kT}{\pi C}\int_0^\infty \frac{du}{u^2+1}$$

$$P_{n,out} = \frac{2kT}{\pi C}\tan^{-1}u\Big|_{u=0}^{u=\infty}$$

$$= \frac{kT}{C}.$$



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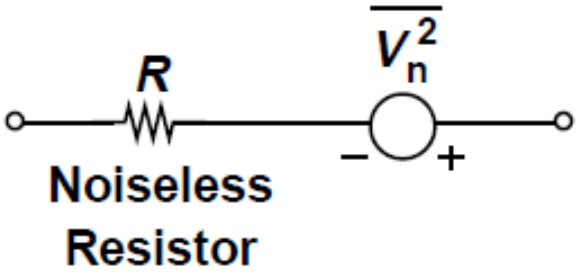
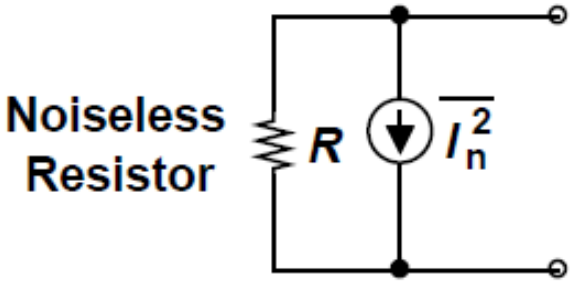
Resistor Thermal Noise



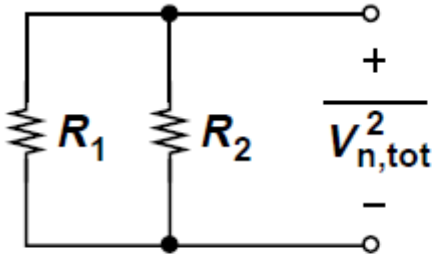
$$\overline{V_n^2} = 4kTR$$

V^2/Hz

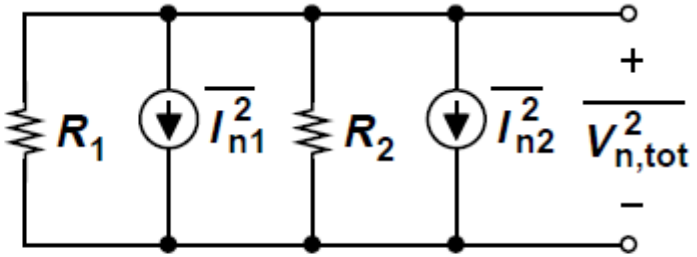


$$\overline{I_n^2} = 4kT/R$$

A^2/Hz



$$\overline{I_{n,tot}^2} = \overline{I_{n1}^2} + \overline{I_{n2}^2} = 4kT\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$$



$$\overline{V_{n,tot}^2} = \overline{I_{n,tot}^2}(R_1 \| R_2)^2 = 4kT(R_1 \| R_2),$$

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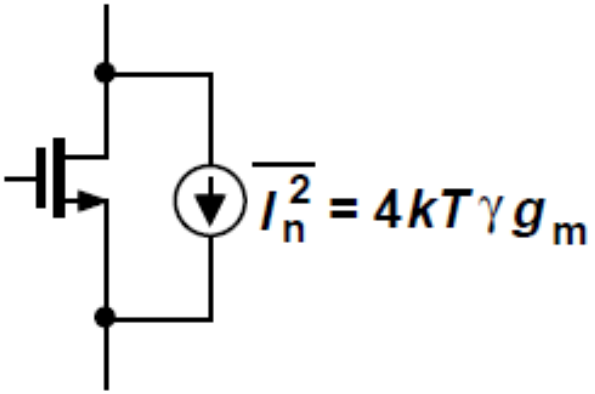
MOSFET Thermal Noise

- **The Thermal noise generated in the channel**
- **For long-channel MOS devices operating in saturation,**



γ *(Excess Noise Coefficient)* = 2/3 for long-ch transistors
2-3 for short-ch transistors

Short channel device – Ecritical – Velocity saturation – extra work done by Efield – dissipation → Noise ^

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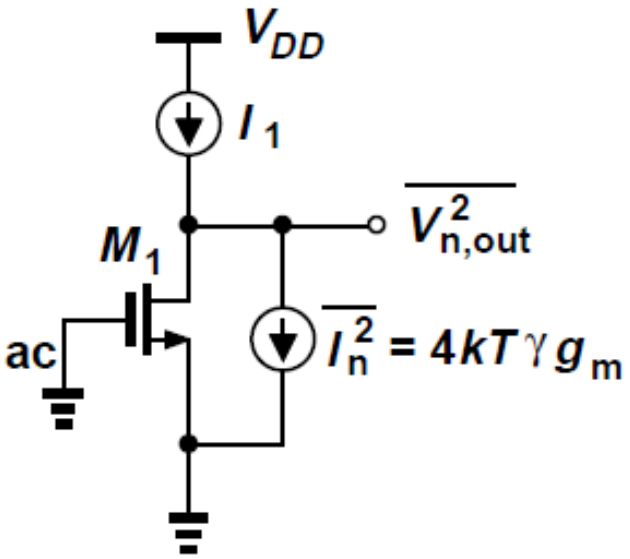
MOSFET Thermal Noise: Example



$$S_{out}(f) = S_{in}(f)|H(f)|^2$$

$$\overline{V_n^2} = \overline{I_n^2} r_O^2$$

$$= (4kT\gamma g_m) r_O^2$$

- **Input is set to zero for noise calculation**
- **The output resistance r_o does not produce noise because it is not a physical resistor**

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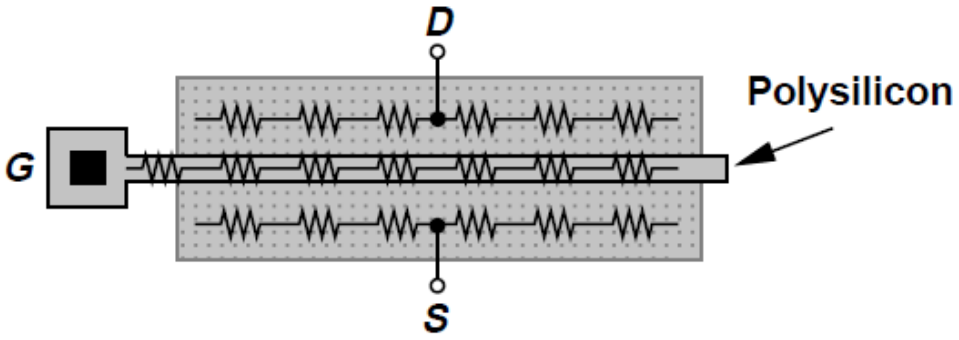
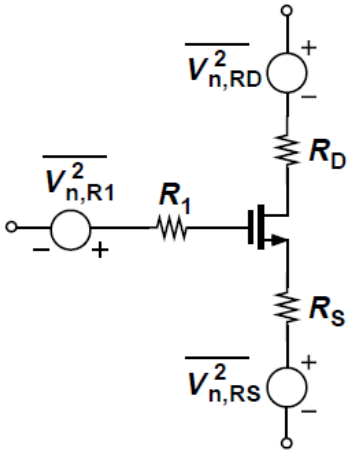
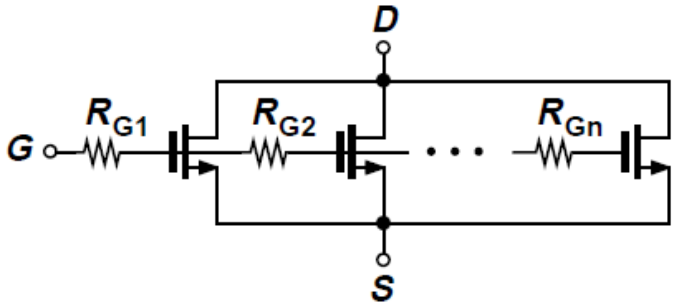
MOSFET Thermal Noise



(a)



(b)



$$R_{G1} + R_{G2} + \cdots + R_{Gn} = R_G$$

(c)

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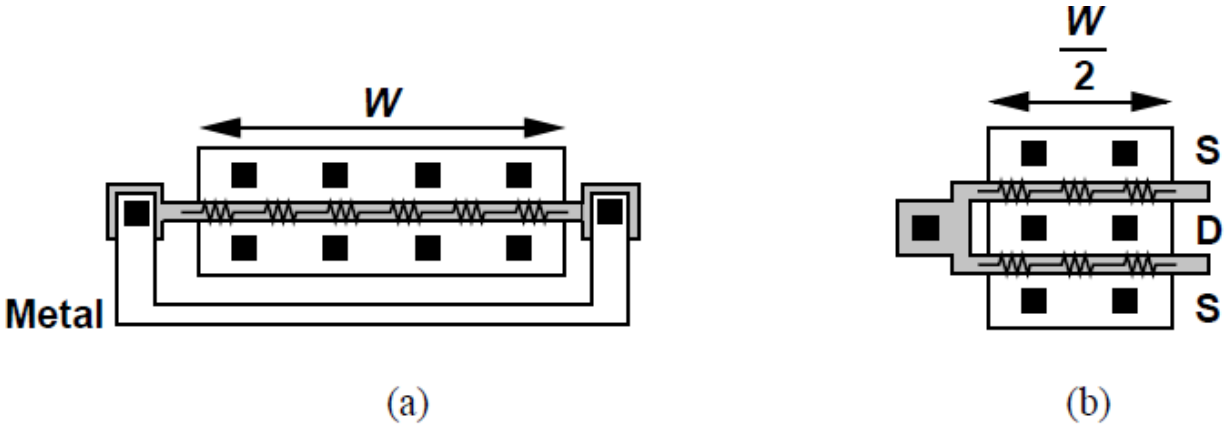
MOSFET Thermal Noise



- Effect of R_G can be reduced by proper layout
- For total gate resistance of R_G, equivalent noise resistance is $R_G/3$ (Distributed effects).

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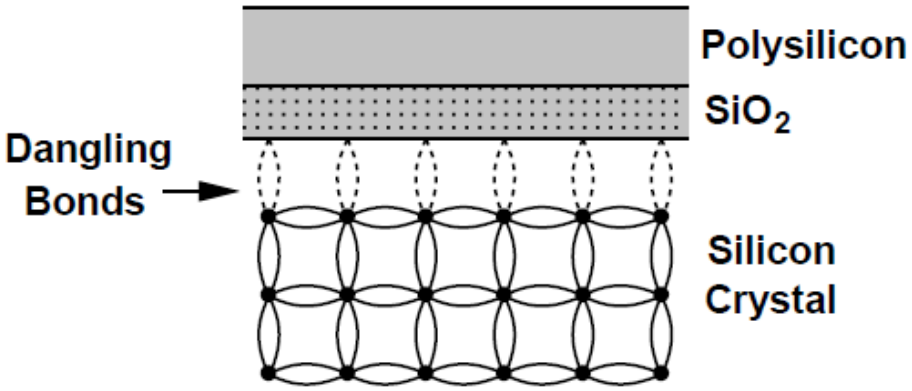
Flicker Noise



- "dangling" bonds giving rise to extra energy states
- Charge carriers moving at the interface are randomly trapped and later released by such energy states, introducing "flicker" noise in the drain current
- Depnds on cleanness of oxide-silicon interface and CMOS technology

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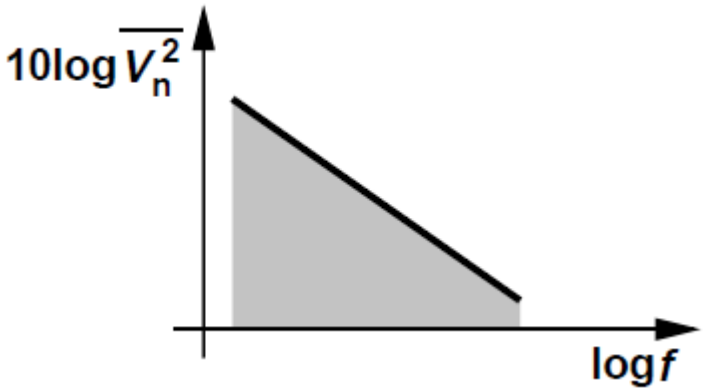
Flicker Noise

- **Modeled as a voltage source in series with the gate and in the saturation region, is roughly given by**

$$\overline{V_n^2} = \frac{K}{C_{ox} W L} \cdot \frac{1}{f}$$

- ***K* is a process-dependent constant on the order of 10^{-25} V^2F**
- ***Larger Area – Averaging effect – Less Flicker***



- **PMOS devices better *1/f* noise**

→ **Holes are carried in a "buried" channel, below oxide-silicon interface**

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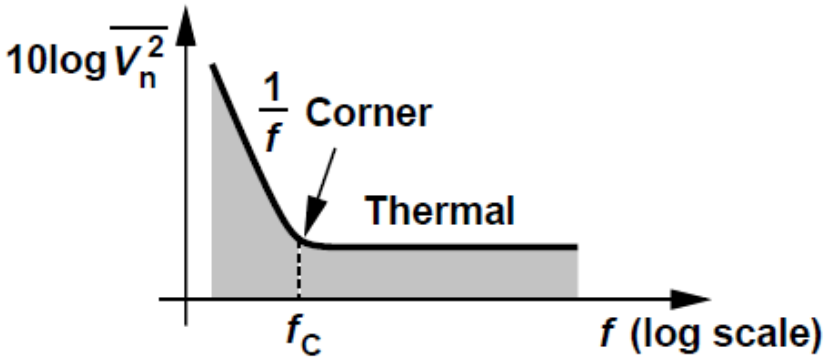
Flicker Noise Corner Frequency

- **At low frequencies, the flicker noise power approaches infinity**
- **Intersection point of thermal noise and flicker noise spectral densities is called "corner frequency" f_c**

At f=f_c ,
Thermal noise = Flicker noise. i.e.,

$$4kT\gamma g_m = \frac{K}{C_{ox}WL}\cdot\frac{1}{f_c}\cdot g_m^2$$



that is,

$$f_c = \frac{K}{\gamma C_{ox}WL}\cdot g_m\frac{1}{4kT}$$

$$f_c \approx \frac{K}{\gamma}.\omega_t.\frac{1}{4kT} \quad \text{and} \quad \omega_t \propto \frac{1}{L^2}$$

Hence, the f_c increases with technology scaling.

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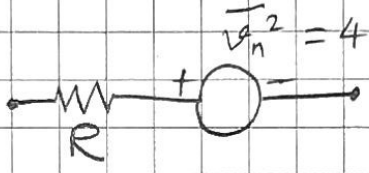
NOISE

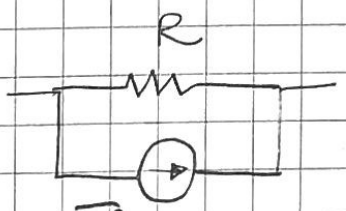
Repeat
Motivation: Why we are studying Noise?

Recap

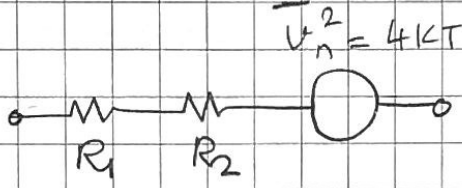


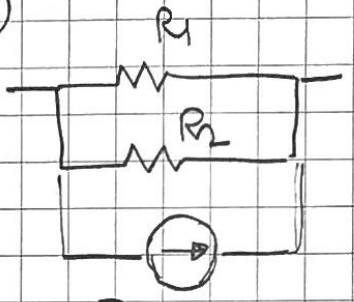
Noiseless

NOISELESS



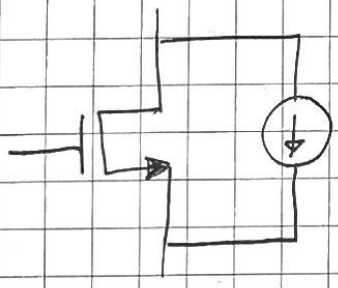
$\overline{i_n^2} = \frac{4KT}{R}$





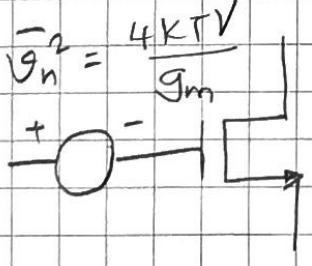
$\overline{i_n^2} = \frac{4KT}{(R_1 \| R_2)}$

MOSFET Thermal Noise



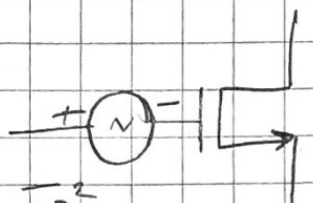
$\overline{i_n^2} = 4KT\gamma g_m$

Excess Noise Coeff. = 2/3 long ch
= 2-3 sh. ch.



r_o – Not physical resistor
– does not produce Noise

MOS FLICKER NOISE



$$\overline{V_{n,1/f}^2} = \frac{K_{1/f}}{C_{ox} W L} \cdot \frac{1}{f}$$

MOS in saturation region.

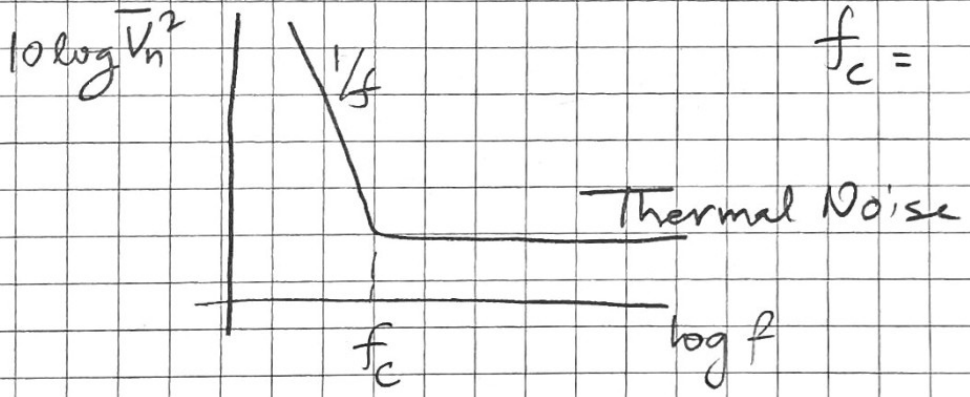
$K_{1/f}$ — process dependent $10^{-25}\ V^2F$

WL — Area ↑ — flicker ↓

Pmos — better 1/f

└ hole transport in buried channel

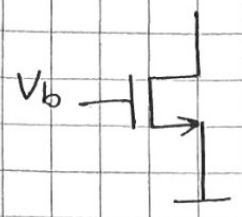
1/f corner



$$f_c = \frac{K_{1/f}}{4KT\gamma} \cdot \frac{g_m}{WLC_{ox}}$$

ω_T

Example: Calculate Thermal & flicker noise for nmos current source. (BW – 1KHz – 10MHz)



Assume $g_m = 1mS$

$C_{gs} = 50\,fF$

$K_{1/f} = 10^{-25}\,V^2F$

(integrated) $\overline{i_{n,thermal}^2} = 4KT\gamma g_m (10^7 - 10^3)$

$= 4 \times 1.38 \times 10^{-23} \times 300 \times \frac{2}{3} \times 1 \times 10^{-3} \times 10^7$

$\doteq 1.1 \times 10^{-16}\ A^2$

$\overline{i_{n\,rms}} = 10.48\ nA_{rms}$. (integrated)

FLICKER NOISE $\overline{i_{n\,1/f}^2} = \frac{K_{1/f}}{C_{ox} W \cdot L} \cdot \frac{1}{f} \cdot g_m^2$

$= \frac{10^{-25}\,V^2F}{50\,fF} \times \frac{(1mS)^2}{f} = \frac{2 \times 10^{-18}}{f}\ (A^2/Hz)$

Total 1/f noise (integrated)

$= \int_{1K}^{10M} \frac{2 \times 10^{-18}}{f}\, df = 2 \times 10^{-18} \ln\left(\frac{10M}{1K}\right)$

$= 18.42 \times 10^{-18}\ A^2$

$\overline{i_{n\,1/f\,rms}} = 4.29\ nA_{rms}$.

$$\overline{i_{n\,1/f}^2} = K' \ln\left(\frac{f_H}{f_L}\right)$$

(total integrated noise)

$f_L \to 0 \rightarrow$ Extremely slow noise components.

$0.01\,Hz \rightarrow 10\,s$; $10^{-6}\,Hz \rightarrow 1$ day

@ Slow rate - noise indistinguishable from thermal drift & aging.

* Voice Band (20 Hz - 20 KHz)

1/f below 20 Hz - insignificant corruption of signal.

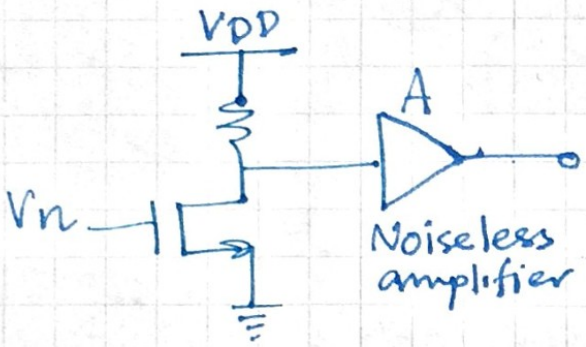
* Total integrated 1/f noise $= K' \ln\left(\frac{f_H}{f_L}\right)$

$K' \ln(10000) = 9.21\,K'$

$K' \ln(1 \times 10^6) = 13.8\,K'$

Taking f_L lower doesn't ~~ing~~ increase integrated noise as fast. - due to "ln" function.

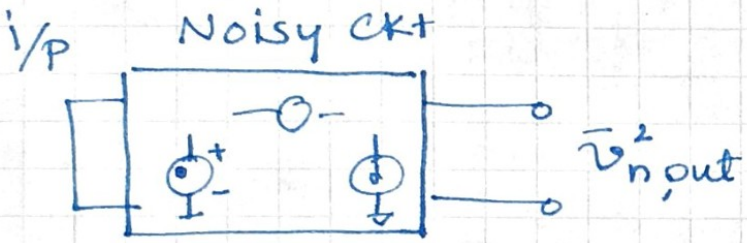
Concept of input referred noise.

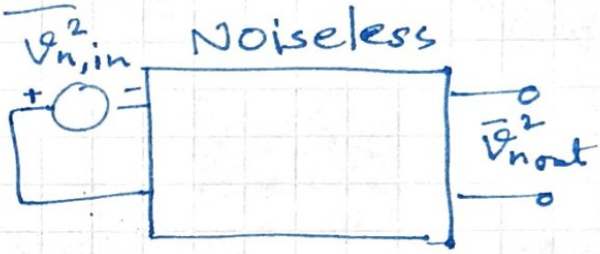


As A ↑ o/p noise ↑.

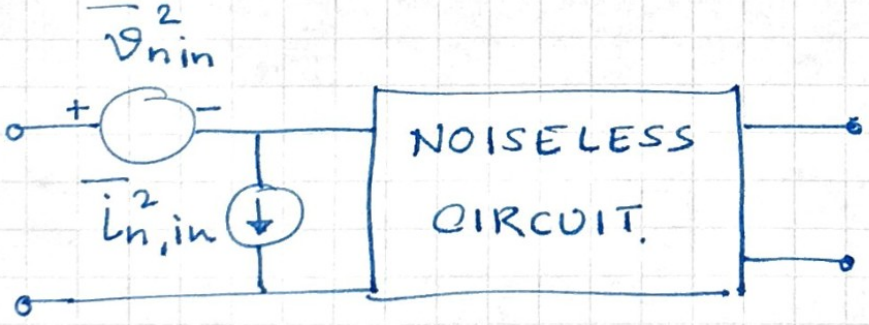
→ A ↑ Signal ↑.

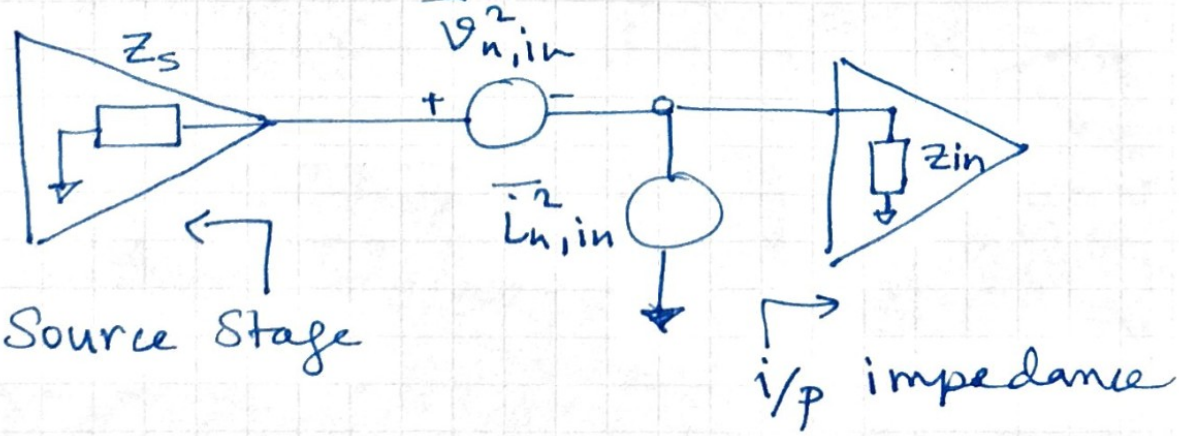
SNR – i/p referred noise.



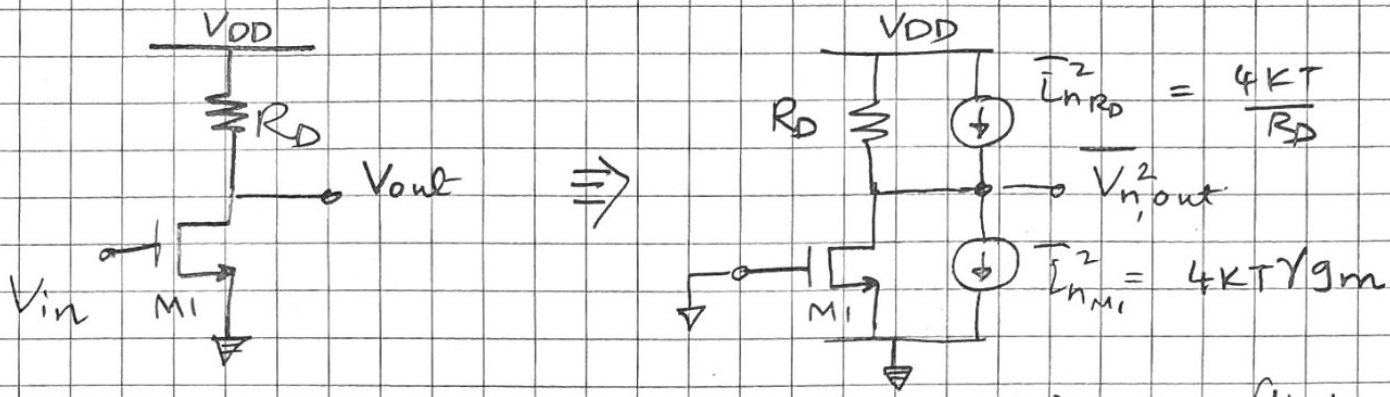


✡ To account for input ~~source~~ impedance of the circuit & source impedance.



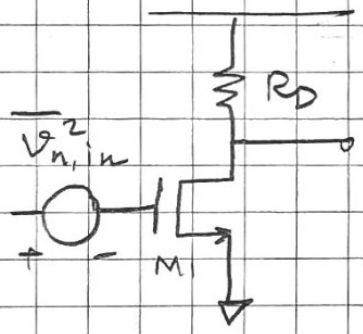


Noise Analysis Examples



(ignoring flicker)

$$\overline{V_{n,out}^2} = \left(\frac{4KT}{R_D} + 4KT\gamma g_m\right) R_D^2 \qquad (R_D \ll r_o)$$



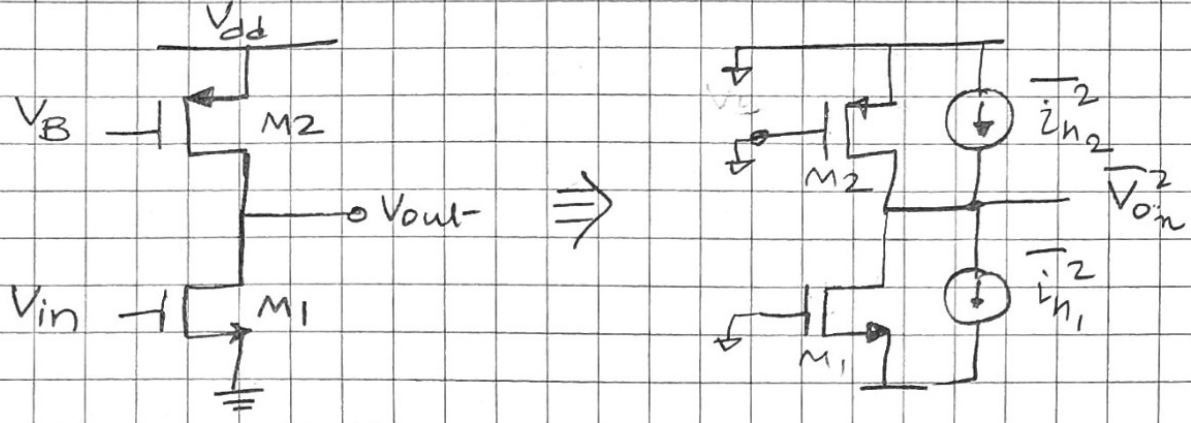
$$\overline{V_{n,in}^2} = \frac{\overline{V_{n,out}^2}}{A_V^2} = \frac{\overline{V_{n,out}^2}}{(g_m R_D)^2}$$

$$= \left(\frac{4KT}{R_D} + 4KT\gamma g_m\right) \frac{R_D^2}{(g_m \cdot R_D)^2}$$

$$= \frac{4KT}{g_m}\left(\frac{1}{g_m R_D} + \gamma\right)$$

(ONLY THERMAL NOISE CONSIDERED)

Example 2. CS AMP



$$\overline{v_{o_n}^2} = \left(4KT\gamma_n g_{m_1} + 4K\gamma_p g_{m_2}\right) r_{out}^2$$

$$\text{Gain} = A_0 = g_{m_1} r_{out}$$

$$\overline{v_{o,in}^2} = \left(4KT\gamma_n g_{m_1} + 4KT\gamma_p g_{m_2}\right) \frac{r_{out}^2}{g_{m_1}^2 r_{out}^2}$$

$$= \frac{4KT\gamma_n}{g_{m_1}} + \frac{4KT\gamma_p}{g_{m_2}} \left(\frac{g_{m_2}}{g_{m_1}}\right)^2$$

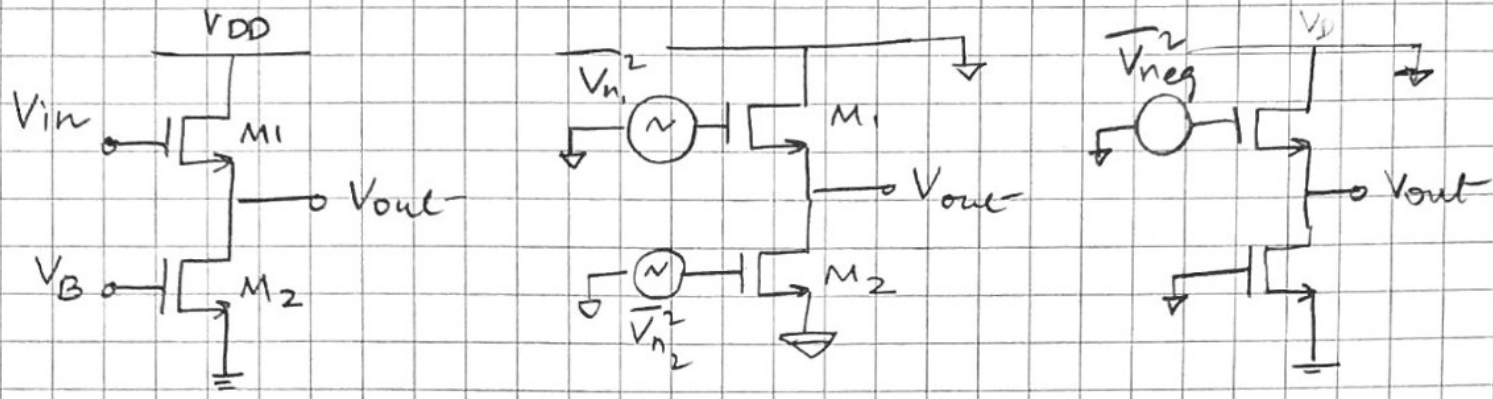
↑ i/p refered due to M_1 only.

→ Keeping g_{m_1} high. Reduces contributions of current source.

$$= \overline{v_{n_1}^2} + \overline{v_{n_2}^2} \left(\frac{g_{m_2}}{g_{m_1}}\right)^2$$

Gate Refered Noise of Each transistor.

Example 3 SOURCE FOLLOWER



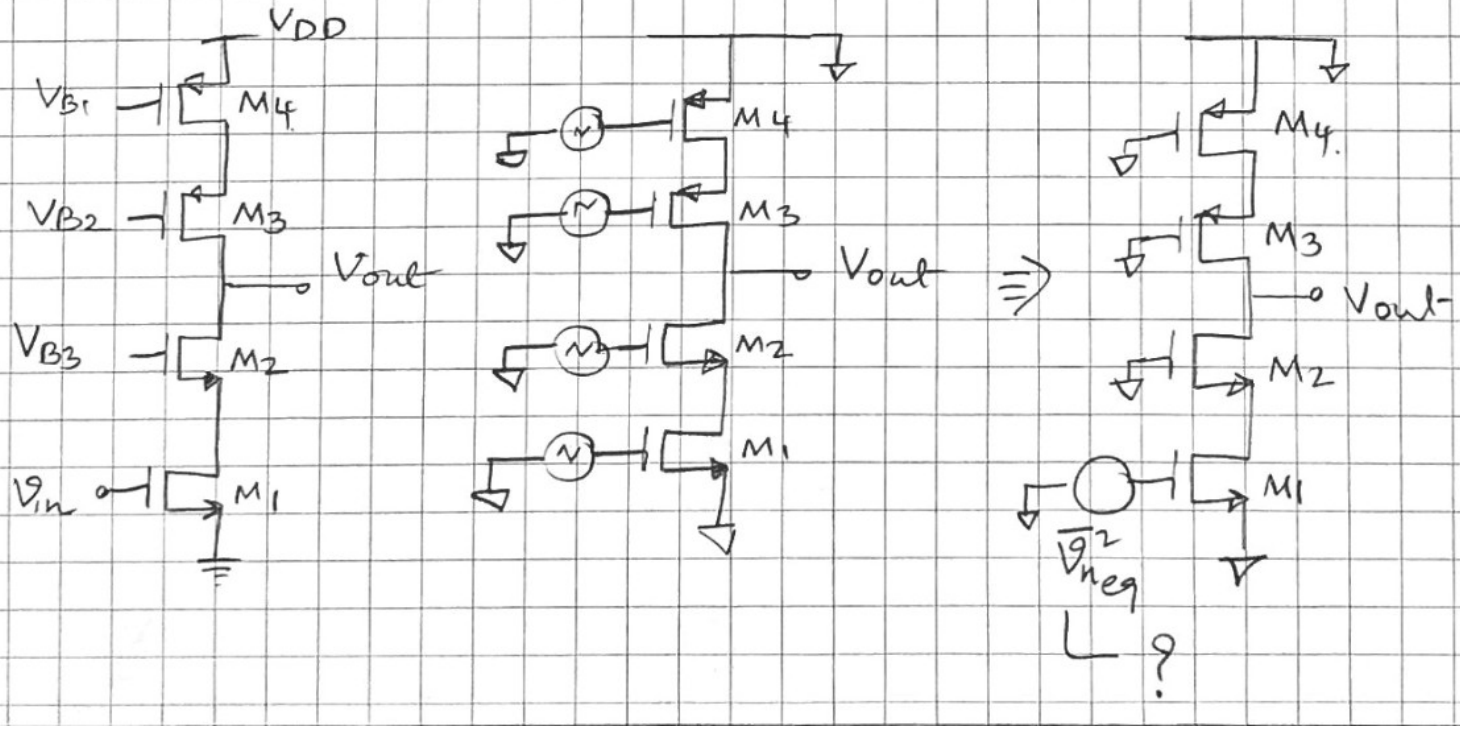
Using superposition

$$\overline{V_{out}^2} = \overline{V_{n_1}^2} + \overline{V_{n_2}^2}\left(\frac{g_{m_2}}{g_{m_1}}\right)^2 = \overline{V_{neq}^2}$$

(Since $A_V = 1$ unity gain)

$$\overline{V_{neq}^2} = \left(\overline{V_{n_1}^2} + \overline{V_{n_2}^2}\left(\frac{g_{m_2}}{g_{m_1}}\right)^2\right)$$

Example 4 CASCODE CS AMP.

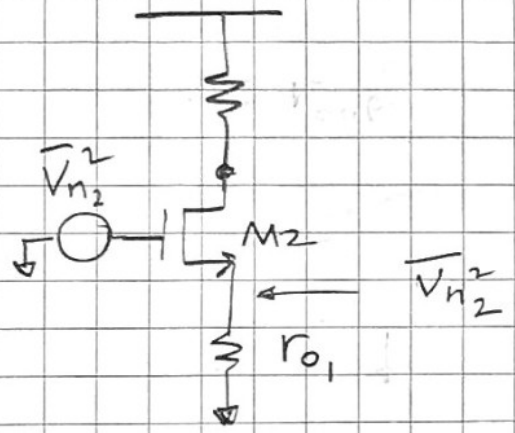


Consider M_1 & M_4 only.

$$\overline{V_{neq}^2} = \overline{v_{n_1}^2} + \overline{v_{n_4}^2}\left(\frac{g_{m_4}}{g_{m_1}}\right)^2$$

(Based on previous example)

Imp point Cascode $\leftrightarrow$ Noise ?

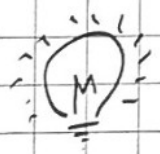


$$\overline{v_{nout}^2} = \frac{\overline{v_{n_2}^2}}{r_{o_1}^2} \times r_{out}^2$$

i/p referred to gate of M_1

$$\overline{V_{neq}^2} = \frac{\overline{V_{n_2}^2}}{r_{o_1}^2} \times \frac{r_{out}^2}{g_{m_1}^2 r_{out}^2}$$

$$= \frac{\overline{V_{n_2}^2}}{(g_{m_1} r_{o_1})^2}$$



Insight Cascode Noise contributions divided by $(g_m r_o)$

Large #

Same applicable to M3.

By superposition

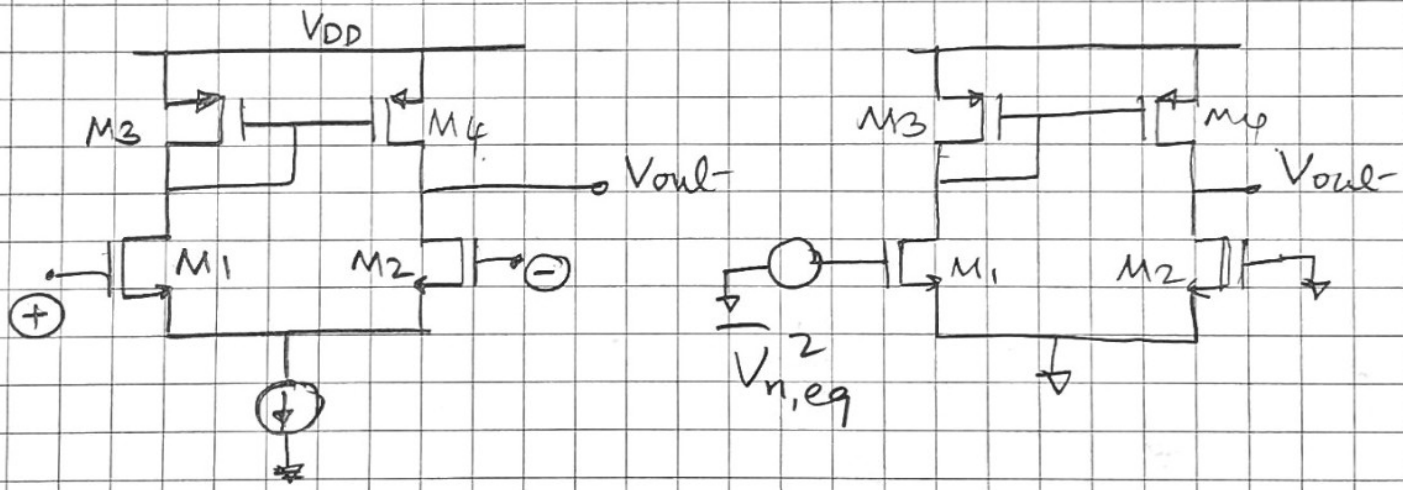
$$\overline{V_{neq}^2} = \overline{v_{n1}^2} + \overline{v_{n4}^2}\left(\frac{g_{m4}}{g_{m1}}\right)^2 + \frac{\overline{v_{n2}^2}}{(g_{m1}r_{o1})^2} + \frac{\overline{v_{n3}^2}}{(g_{m1}r_{o4})^2}$$

Cascode contribution

Cascode generally does not degrade noise performance.

Example: 5

CMOS DIFF AMP



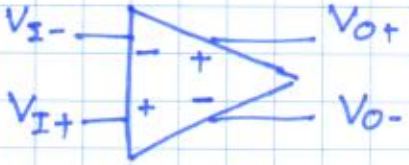
$$\overline{V_{n,eq}^2} = 2\left[\overline{v_1^2} + \overline{v_3^2}\left(\frac{g_{m3}}{g_{m1}}\right)^2\right]$$

(PROVE URSELF)

Standard Differential Amplifier (Lecture 7)

- → Differential i/p
- → Common-mode (i/p) is rejected by diff pair with current source
- → Single-Ended Output (DE to SE conversion) using mirror.

Std. Diff. Amplifier



Fully Differential Amplifier

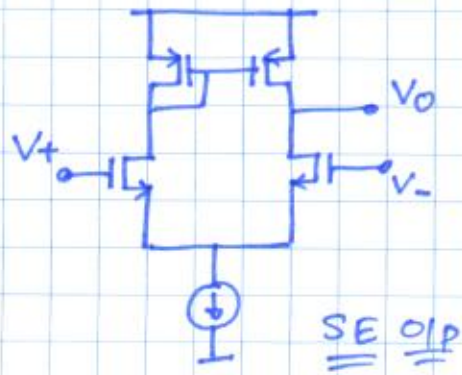
Fully. Differential Amplifier

- → Differential i/p, Differential O/p.
- → i/p common-mode is rejected by i/p diff pair
- → O/p common-mode set independently

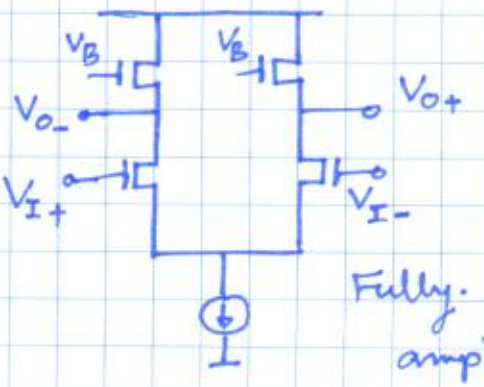
Why?

- ✡ Increased (double) O/p swing.
- ✡ Excellent Power Supply rejection
- ✡ Immune to noise coupling from any external sources.
- ✡ Improved freq. response ← NO DE2SE conversion

Simplest Example

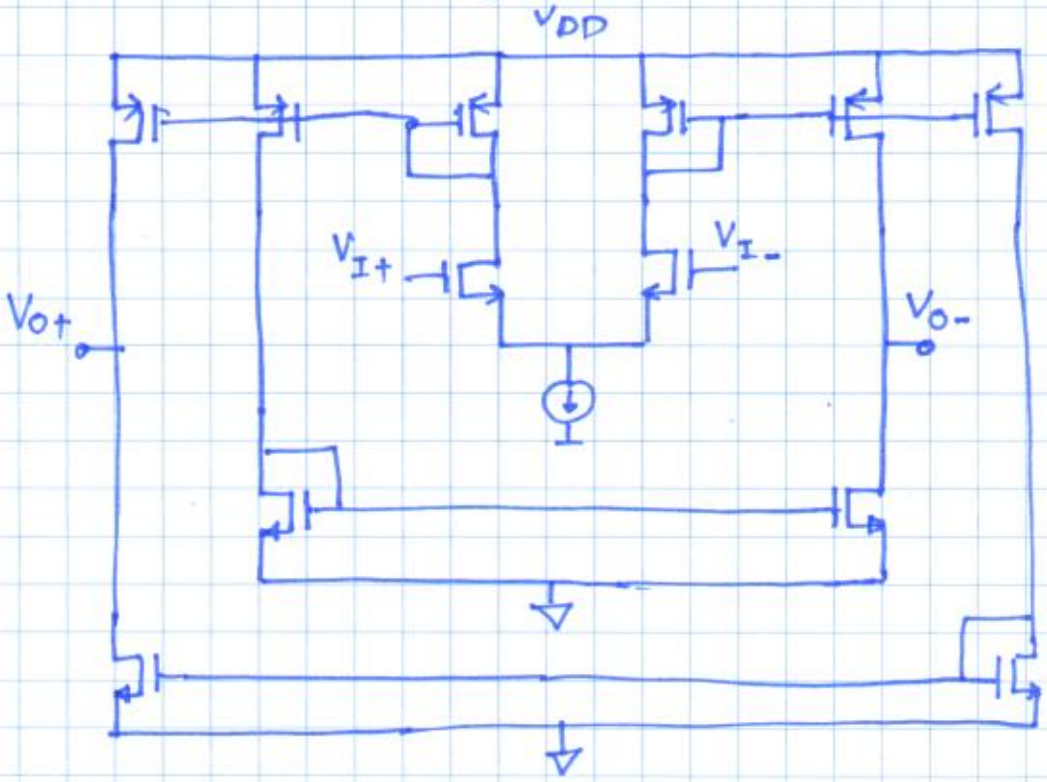


SE O/P

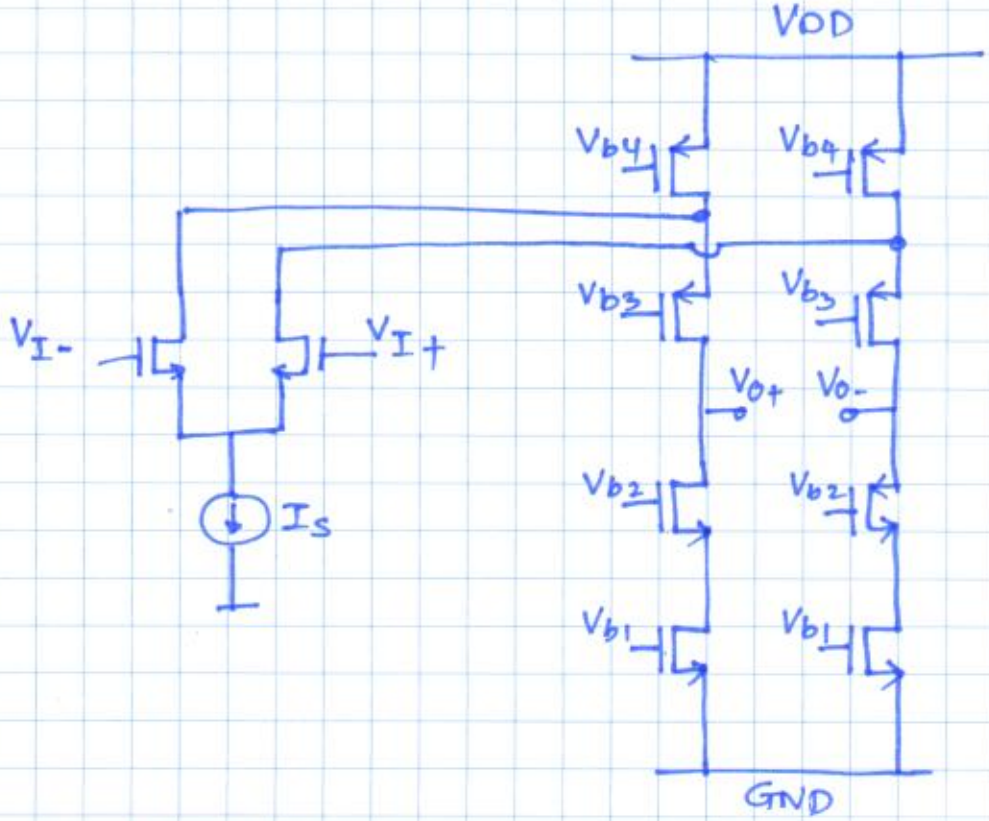


Fully. Diff. amplifier

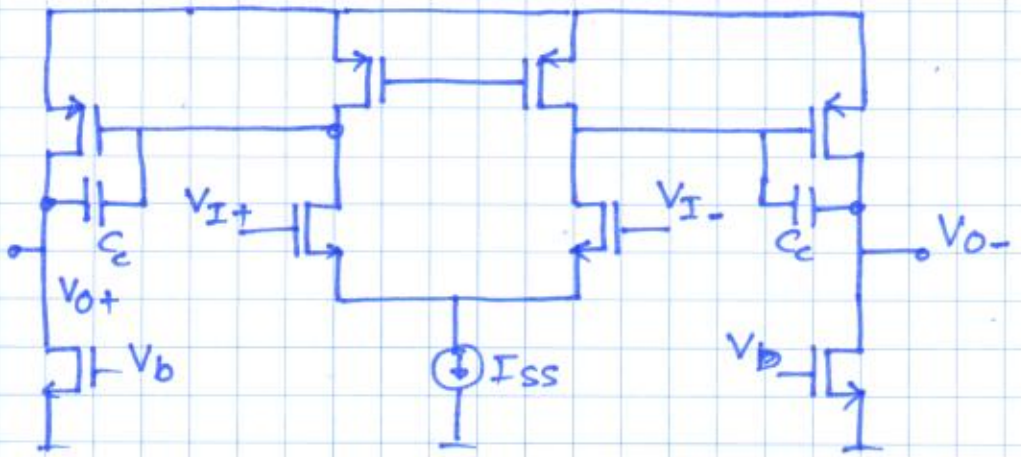
Examples of fully. differential Amplifiers



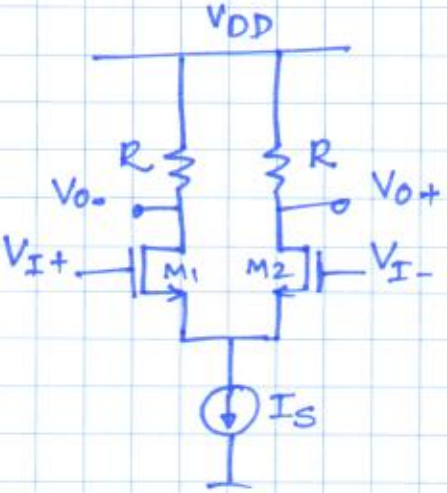
Fully Diff Folded Cascode Opamp



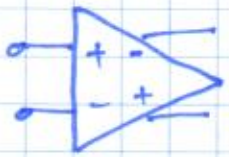
Fully-Differential Two Stage Opamp



Consider Simple diff pair with Rload. (fully diff)



$\Rightarrow$

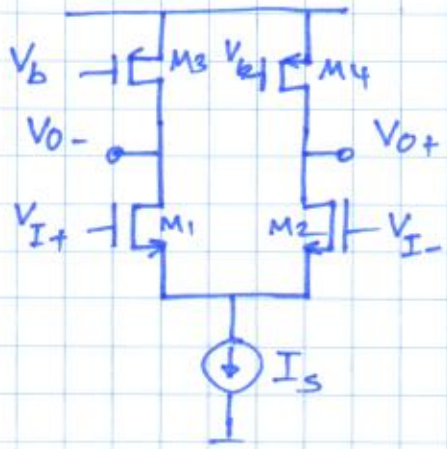


Assume: $V_{I+} = V_{I-} = V_{ICM}$.

M_1, M_2 sat.

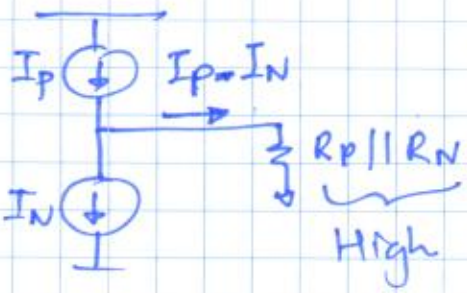
$V_{OCM} = V_{DD} - \frac{I_S}{2} R$ ← very well defined.

Current Source loading — High Gain



For common mode i/p V_{ICM}.

Assume all Transistor in Sat.



V_{OCM} undefined

I_P ; I_N are defined by process, temp, voltage
→ will change.
∴ → Even mismatches will impact V_{OCM}.

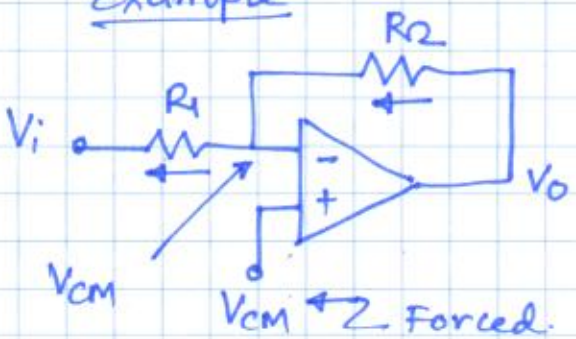
→ Tweeking I_P, I_N to get $V_{OCM} = V_{DD}/2$

→ DOESNOT work – V_{OCM} will keep changing with PVT & mismatches.

→ Need Feedback at o/p to stabilize output common-mode voltage.

→ Note: Differential feedback does not correct common-mode.

Example

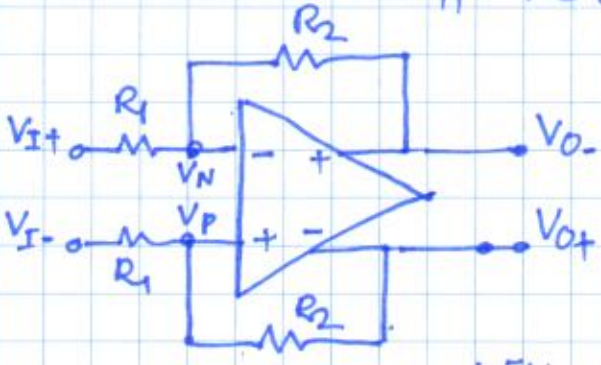


$$\frac{V_o - V_{CM}}{R_2} = \frac{V_{CM} - V_i}{R_1}$$

$$V_o = \frac{R_2}{R_1}(V_{CM} - V_i) + V_{CM}$$

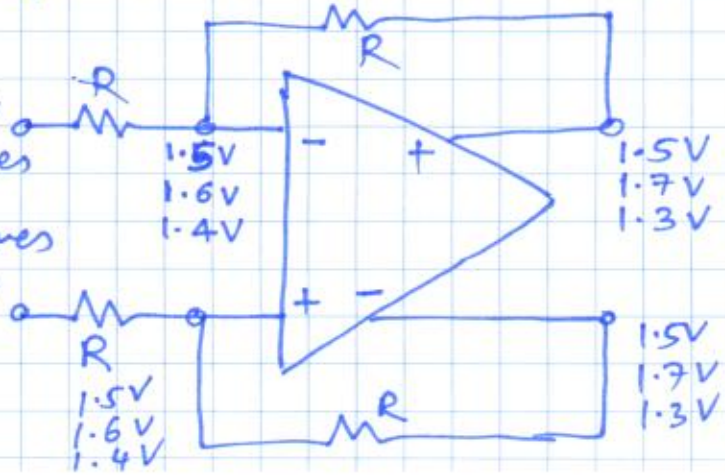
$$= -\frac{R_2}{R_1} V_i + \left(1 + \frac{R_2}{R_1}\right) V_{CM}$$

o/p DC (common Mode) very well defined.



Lets assume $(V_{I+}, V_{I-})_{CM} = V_{icm}$.
$= 1.5V$

$R_1 = R_2 = R$



V_P, V_N can take any values

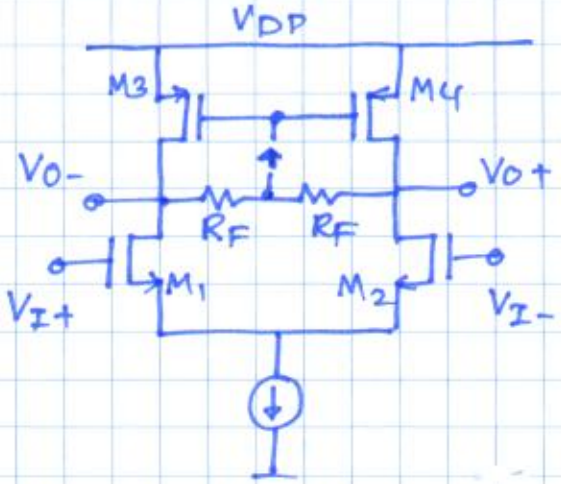
V_{op}, V_{o-} can take any values

o/p CM poorly defined

Need CMFB Common-Mode Feedback circuit

→ Required for high gain fully differential ckt.

Simple Example



Diff gain $g_{m_1}(r_{o_1} \| r_{o_3} \| R_F)$

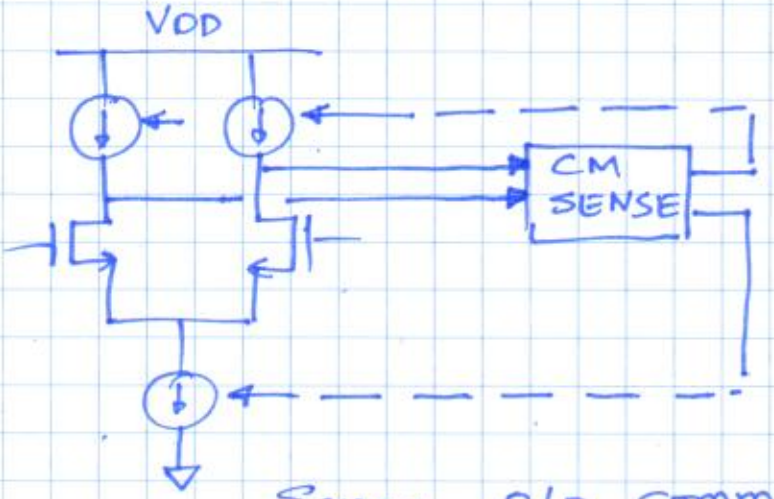
R_F → large.

O/p Common-mode

$$V_{OCM} = V_{DD} - |V_{GS_3}|$$

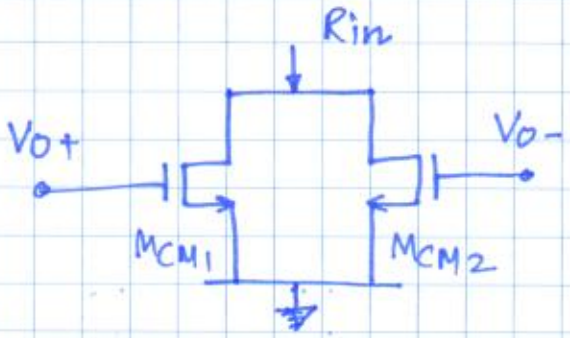
$$V_{DD\,min} = 2V_{dsat} + |V_{GS_3}| = 3V_{dsat} + |V_{T_P}|$$

Generic CMFB Strategy



Sense O/p common-mode voltage & adjust one of current sources.

CMFB using MOSFETs in triode region.



$$R_{in} = R_{CM1} \parallel R_{CM2}$$

↑ ↑

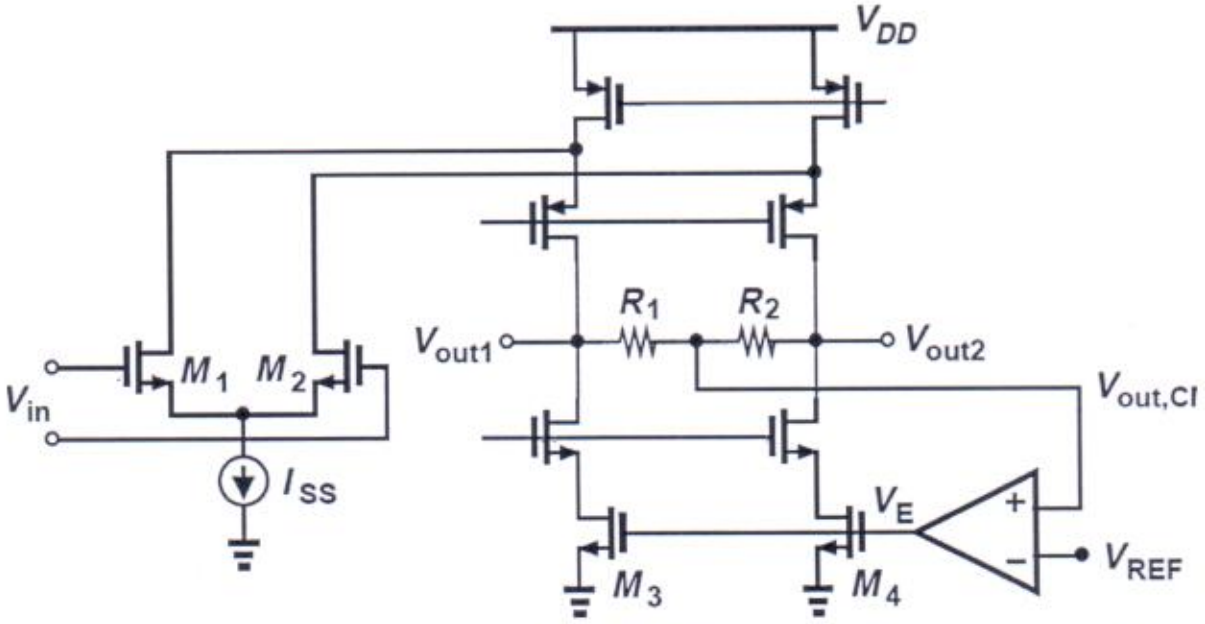
Triode region Resistance

$$R_{in} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{O+} - V_{TH})} \parallel \frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{O-} - V_{TH})}$$

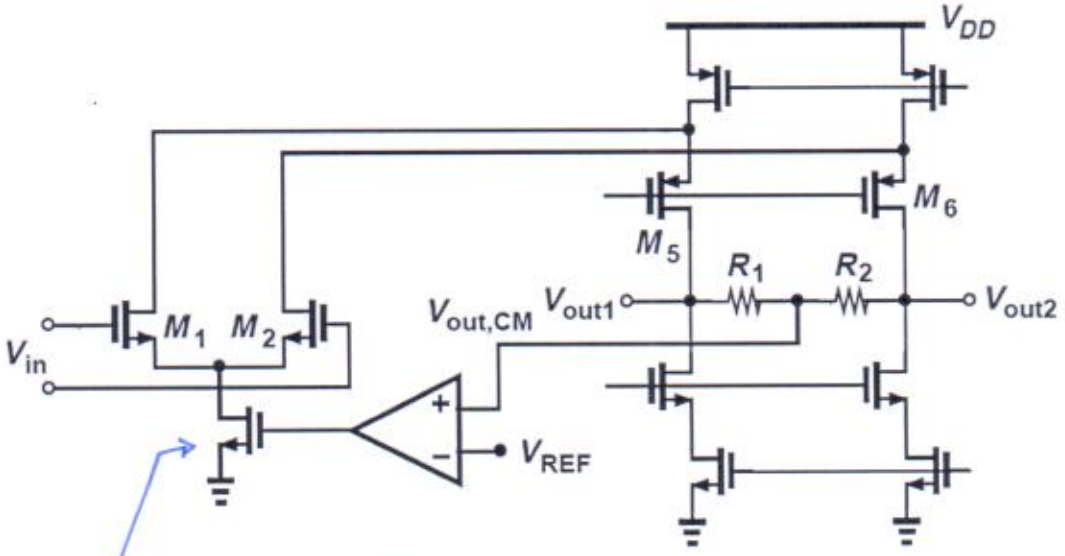
$$= \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{O+} + V_{O-} - 2V_{TH})}$$

$V_{O+} + V_{O-} \propto \frac{1}{V_{CM}}$ ← Independent of $(V_{O+} - V_{O-})$ (diff o/p voltage)

CMFB implementations (Folded-Cascode opamps)



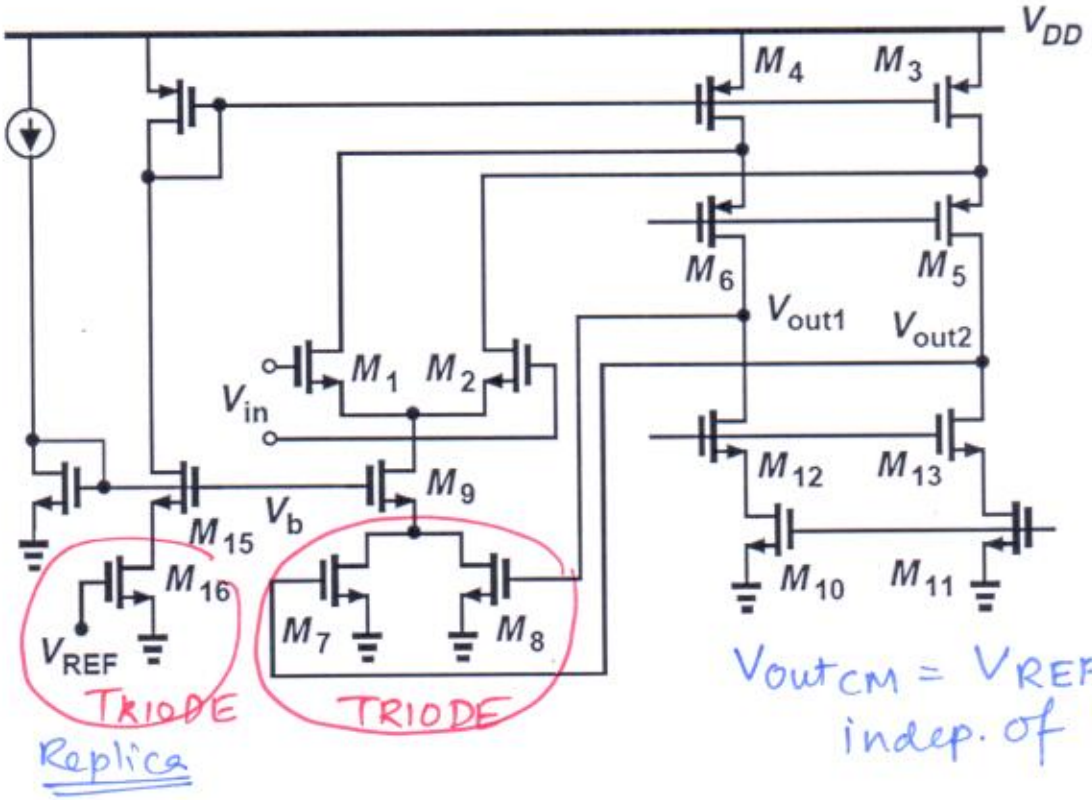
o/p current source control.



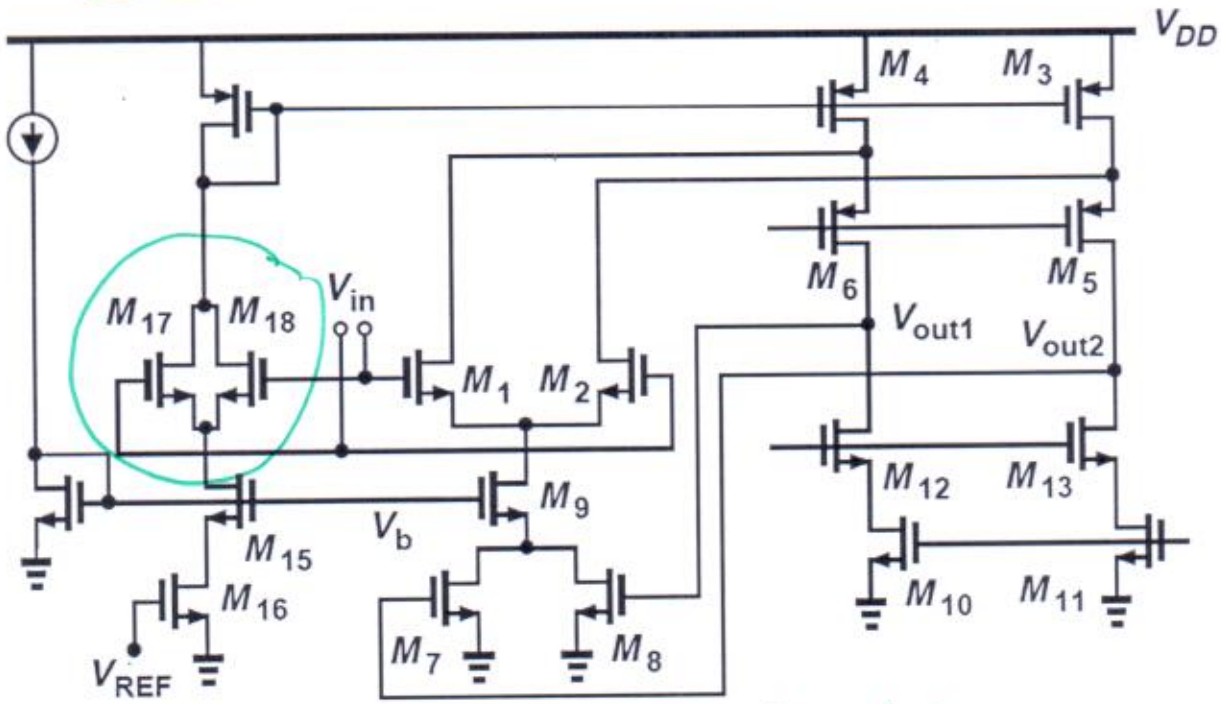
Diff pair tail current source control

Illustrations from Razavi Textbook

CMFB using triode region transistors



$V_{out_{CM}} = V_{REF}$ indep. of V_b.



M_{17} & M_{18} – Replica of diff pair

→ Make sure $V_{DS_{15}} = V_{DS_9}$

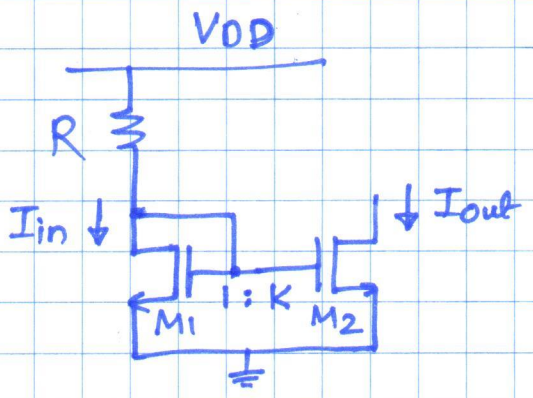
Indep. of Ch. length Mod?

REFERENCE CIRCUIT DESIGN.

* Voltage or Current Reference
* Process, Temperature or Supply independent
* Or. well-defined (predictable) dependence on Temp.

⇒ Goal - Overall Chip performance predictable / consistent over PVT. Yield. - Meet specs over PVT.

1. Supply Independent Current-source



$I_{in} = \frac{V_{DD} - V_{GS}}{R}$

$\Delta I_{in} = \frac{\Delta V_{DD} - \Delta V}{R}$

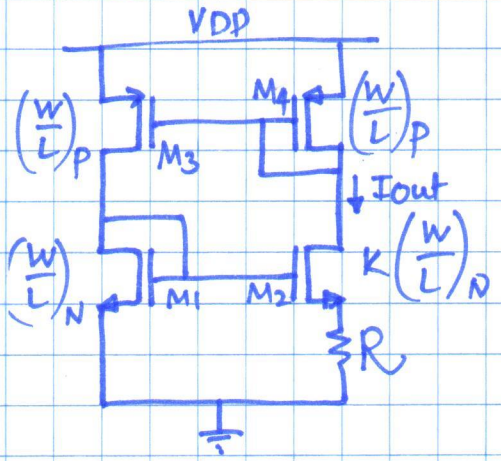
$\Delta V_{GS_1} = \frac{\Delta I_{in}}{g_{m_1}}$

$\Delta I_{in} = \frac{\Delta V_{DD}}{R + \frac{1}{g_{m_1}}}$

$\Delta I_{out} = K \frac{\Delta V_{DD}}{R + 1/g_{m_1}}$ ← fn of I & hence V_{DD}

No good. ☹

Consider



$V_{GS_1} = V_{GS_2} + I_{out} R$

$K_n = \mu_n C_{ox}$

$V_T + \sqrt{\frac{2 I_{out}}{K_n (W/L)_N}} = V_T + \sqrt{\frac{2 I_{out}}{K_n K (W/L)_N}} + I_{out} R$

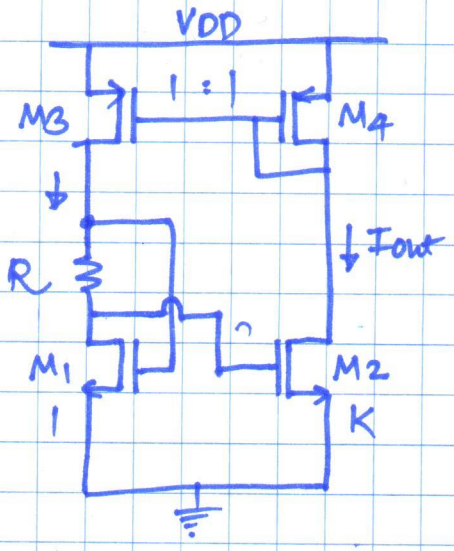
$\sqrt{I_{out}} = \frac{1}{R} \left[\sqrt{\frac{2}{K_N (W/L)_N}} \left(1 - \frac{1}{\sqrt{K}} \right) \right]$

$I_{out} = \frac{1}{R^2} \cdot \frac{2}{K_N (\frac{W}{L})_N} \left(1 - \frac{1}{\sqrt{K}} \right)^2$

→ indep of V_{DD} – dependson process & T & R value.

⊖ Body effect of M_2.

Improved circuit



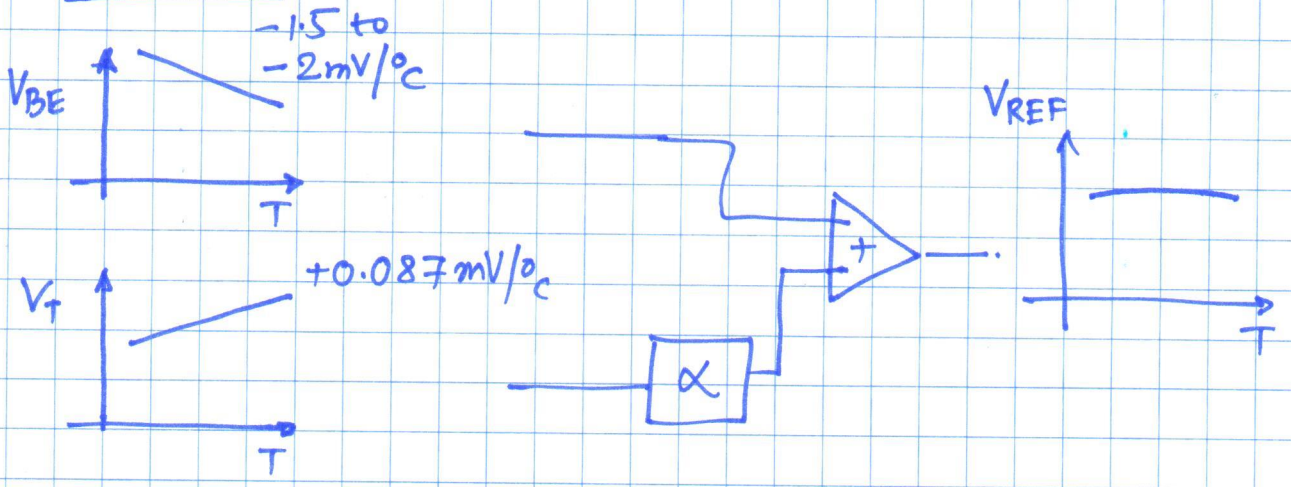
No Body effect for M_2.

Same Iout equation.

Use long channel devices to reduce Ch. length modulation.

Temperature Independent Reference

Concept



$$V_{REF} = V_{BE} + \alpha V_T$$

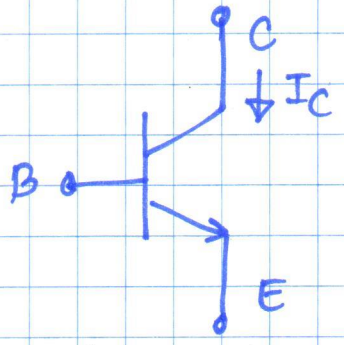
V_{BE}: -ve Temp Co

αV_T: +ve Temp Co

→ Process, Supply & Temp Independent

→ Need to use Bipolar Transistors

Bipolar Basics



$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right), \quad V_T = \frac{kT}{q}$$

Saturation current $\propto \mu k T n_i^2$

$\mu k T n_i^2$ ← (intrinsic carrier conc), Bandgap → 1.12 eV

mobility $\propto \mu_0 T^m$, $m \sim \left(-\frac{3}{2}\right)$; $\propto T^3 \exp\left[-E_g/kT\right]$

Overall $I_S = b\, T^{4+m} \exp\frac{-E_g}{kT}$

constant. indep. of T

$$V_{BE} = V_T \ln\left(\frac{I_C}{I_S}\right)$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_T}{\partial T} \cdot \ln\left(\frac{I_C}{I_S}\right) - \frac{V_T}{I_S}\frac{\partial I_S}{\partial T}$$

Simplification: I_C held constant

$$\frac{V_{BE}}{T} \qquad (4+m)\frac{V_T}{T} + \frac{E_g}{kT^2}V_T$$

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - E_g/q}{T}$$

Older Tech $V_{BE} = 0.7\,V$ $T = 300^\circ K$ $\Rightarrow \frac{\partial V_{BE}}{\partial T} \approx -1.9\,mV/^\circ K$

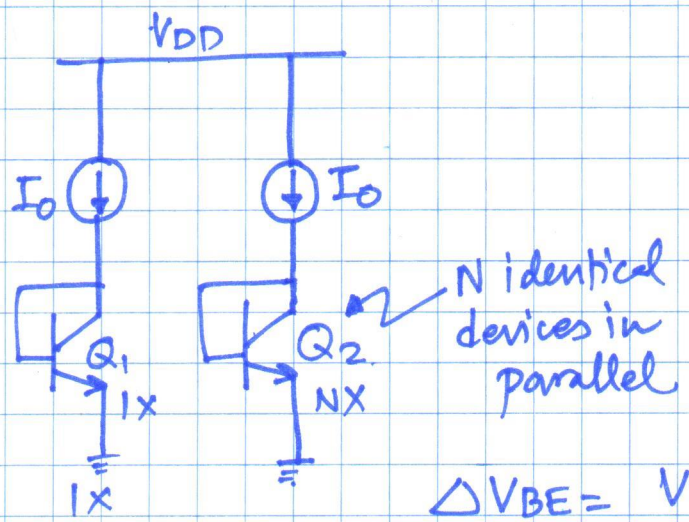
Modern Tech. $V_{BE} = 0.8\,V$ $T = 300^\circ K$ $\Rightarrow \frac{\partial V_{BE}}{\partial T} \approx -1.5\,mV/^\circ K$

NOTE: If you take into account collector current var^n ($I_C = \frac{V_T \ln N}{R}$), then equation modified as $(3+m)$ instead of $(4+m)$ (Razavi pp. 517)

How to generate the TC voltage?

PTAT Proportional to Absolute Temperature.

Hilbiber 1964



$$V_{BE_1} = V_T \ln\left(\frac{I_o}{I_s}\right)$$

$$V_{BE_2} = V_T \ln\left(\frac{I_o/N}{I_s}\right)$$

$$\Delta V_{BE} = V_{BE_1} - V_{BE_2}$$

$$= V_T \ln\left(\frac{I_o}{I_s}\right) - V_T \ln\left(\frac{I_o/N}{I_s}\right)$$

$$= V_T \ln(N) = \frac{kT}{q} \ln(N)$$

k, q constants $N \rightarrow$ scaling ratio

$\Delta V_{BE} \propto T$ indep of P.V.

$$V_{REF} = V_{BE} + \alpha V_T$$

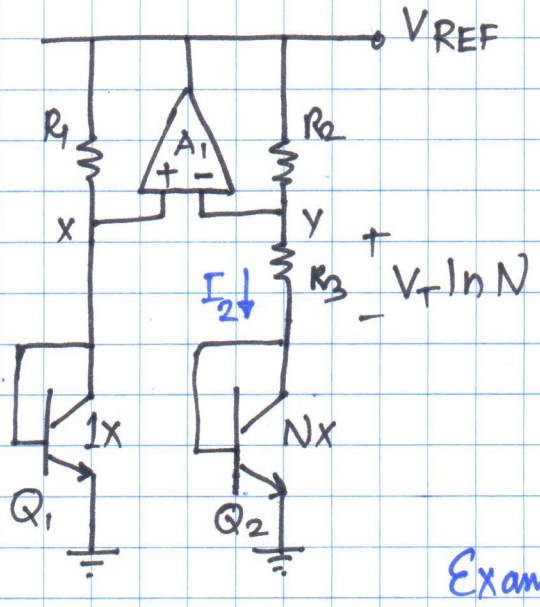
$-1.5\,mV/^\circ K$ $0.087\,mV/^\circ K$

$\alpha = 17.2$

$$V_{REF} = 800mV + (17.2 \times 26mV)$$

$$\cong 1.25\,V$$ (Bandgap Voltage)

Circuit Implementation

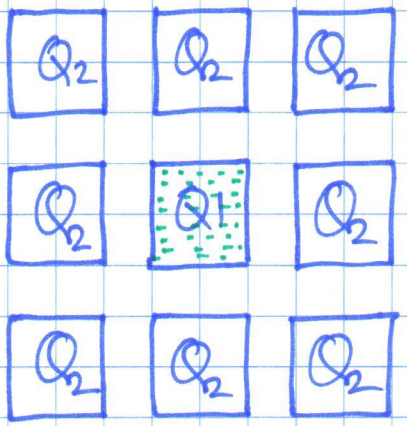


$$V_{REF} = (R_2+R_3)I_2 + V_{BE}$$

$$= V_{BE} + (R_2+R_3)\left(\frac{V_T \ln N}{R_3}\right)$$

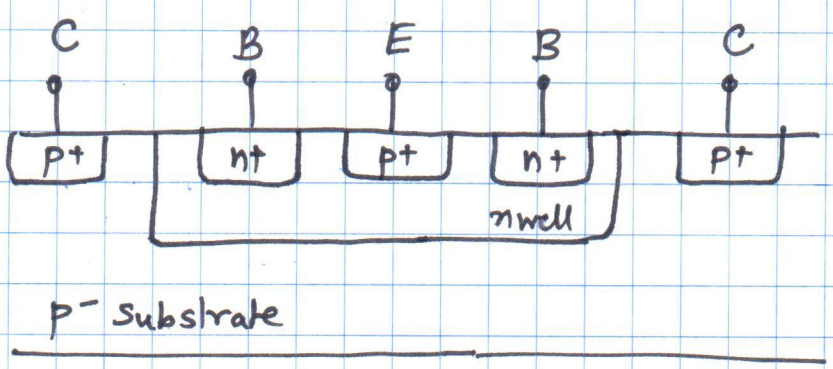
$$= V_{BE} + \left(1 + \frac{R_2}{R_3}\right) V_T \ln n.$$

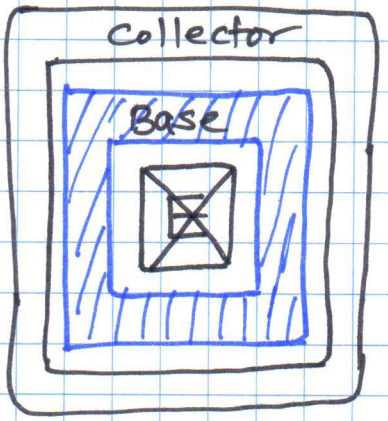
Example $n = 8$ $\quad \frac{R_2}{R_3} = 7.3$

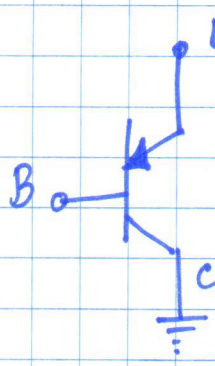


Common Centroid layout
— matching between Q_1 & Q_2

Bipolar Transistors in CMOS Technology

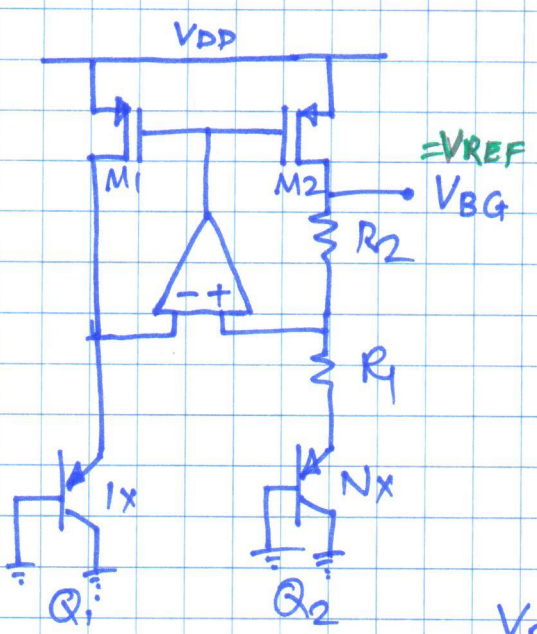






← Collector is always grounded [substrate]

CMOS implementation



$$x = \left(\frac{R_2+R_1}{R_1}\right)$$

$$V_{REF} = V_{BE} + xV_T \ln N$$

$$\frac{\partial V_{REF}}{\partial T} = \frac{\partial V_{BE}}{\partial T} + x\frac{V_T}{T}\ln N = 0$$

for flat response...

$$-\frac{xV_T}{T}\ln N = \frac{V_{BE} - (4+m)V_T - E_g/q}{T}$$

Substitute

$$\Rightarrow xV_T \ln N = (4+m)V_T + \frac{E_g}{q} - V_{BE}$$

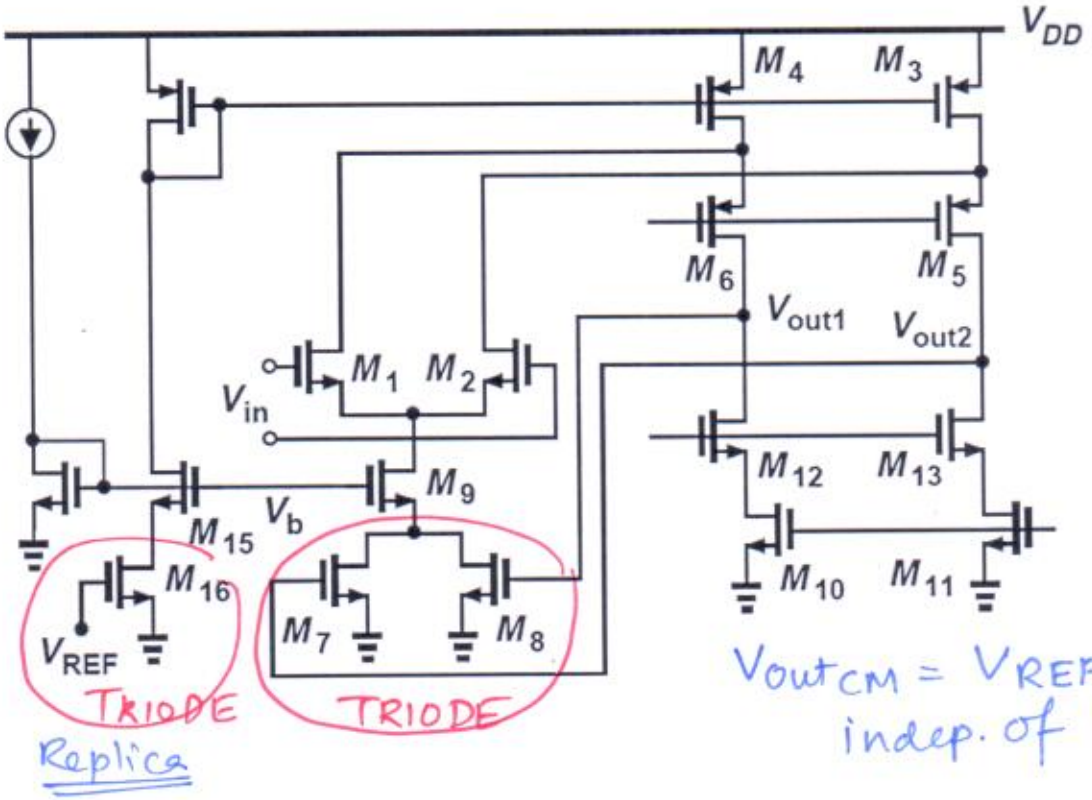
$$V_{REF} = \frac{E_g}{q} + (4+m)V_T$$

↑ μ Temp exponent

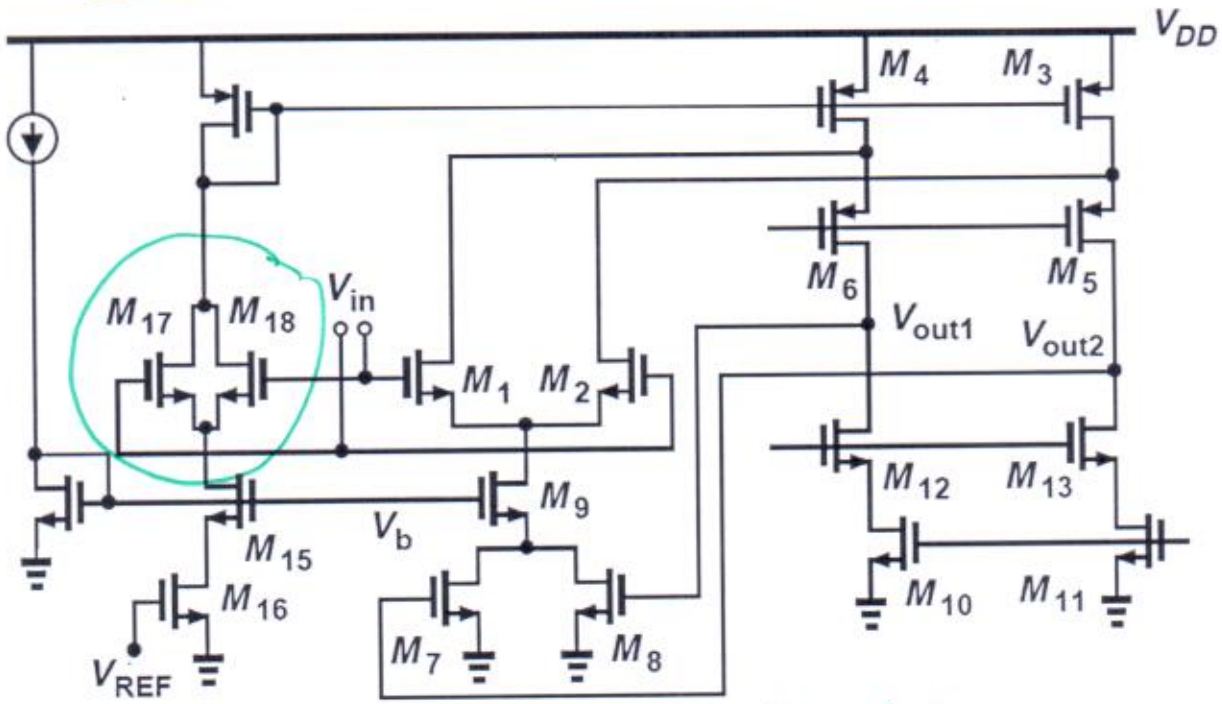
as $T \to 0$ $V_{REF} = \frac{E_g}{q}$ (Bandgap voltage)

Explain opamp +/- connection.

CMFB using triode region transistors



$V_{out_{CM}} = V_{REF}$ indep. of V_b.



M_{17} & M_{18} – Replica of diff pair

→ Make sure $V_{DS_{15}} = V_{DS_9}$

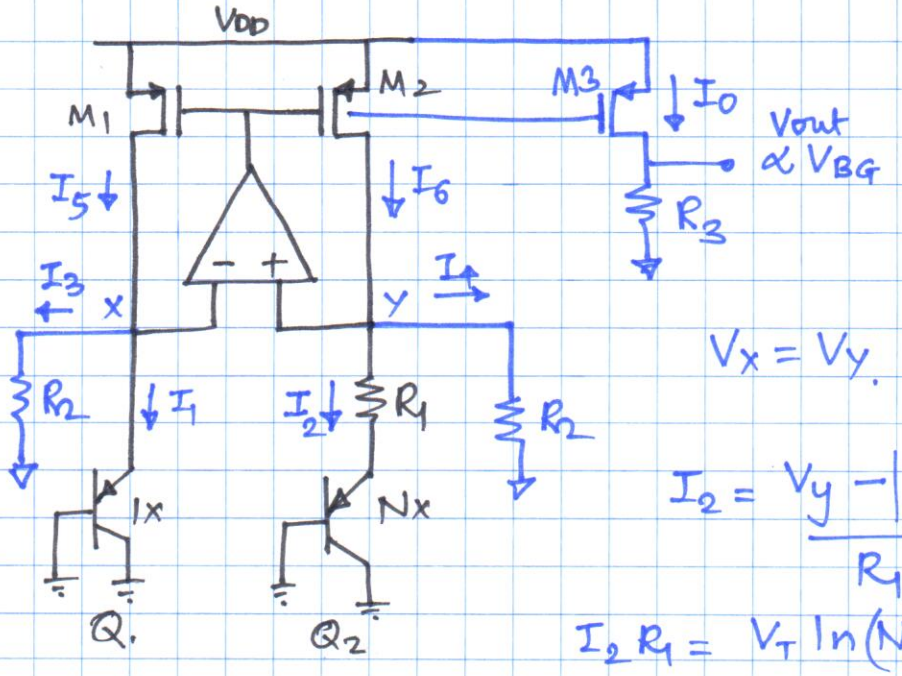
Indep. of Ch. length Mod?

Since $V_{REF} \cong 1.25V$ $V_{DD} > 1.25V$.

What about V_{REF} for $V_{DD} < 1V$.?

Reference

H. Banba "CMOS BGAP REF with Sub.1-V op" JSSC NOV 1997.



$V_x = V_y$ due to fbk (OPAMP)

$$I_2 = \frac{V_y - |V_{BE_2}|}{R_1} = \frac{|V_{BE_1}| - |V_{BE_2}|}{R_1}$$

$$I_2 R_1 = V_T \ln(N) \quad \text{—①}$$

Also $I_3 = I_4 = \frac{V_{BE1}}{R_2}$

$$I_6 = I_2 + I_4 = \frac{V_T \ln N}{R_1} + \frac{|V_{BE_1}|}{R_2} = \frac{1}{R_2}\left(|V_{BE_1}| + V_T \ln N \left(\frac{R_2}{R_1}\right)\right)$$

By choosing $\frac{R_2}{R_1}$. term inside brackets $= V_{BG}$

$$I_6 = \frac{V_{BG}}{R_2}$$

$$I_0 = \frac{V_{BG}}{R_2} \Rightarrow \boxed{V_{out} = \frac{R_3}{R_2} V_{BG}}$$

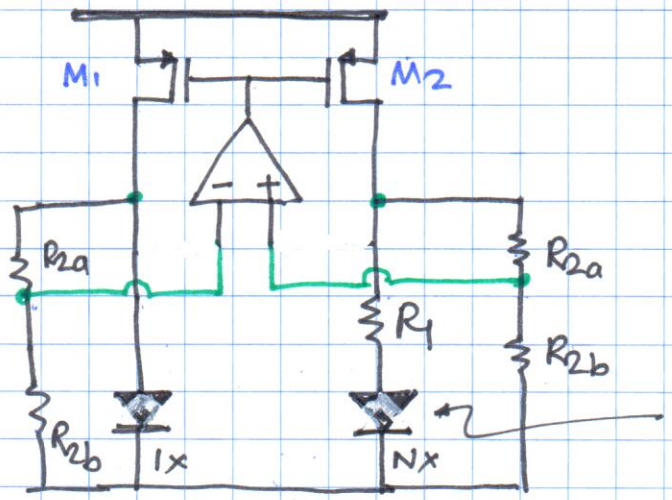
keep $\frac{R_3}{R_2} < 1$ for $V_{DD} < 1V$

Issue with Banba Bgap.

Nodes x & y DC voltage 0.7V — 0.9V ~

→ Input diff pair of opamp — Native NMOS ($V_T \simeq -0.2V$)

→ Leung / Mok solution | IEEE JSSC Apr. 2002 "A Sub-1-V 15-ppm/°C CMOS Bgap ...



Lower common mode i/p range of opamp using resistive divider.

V_{BE} junction shown as diode

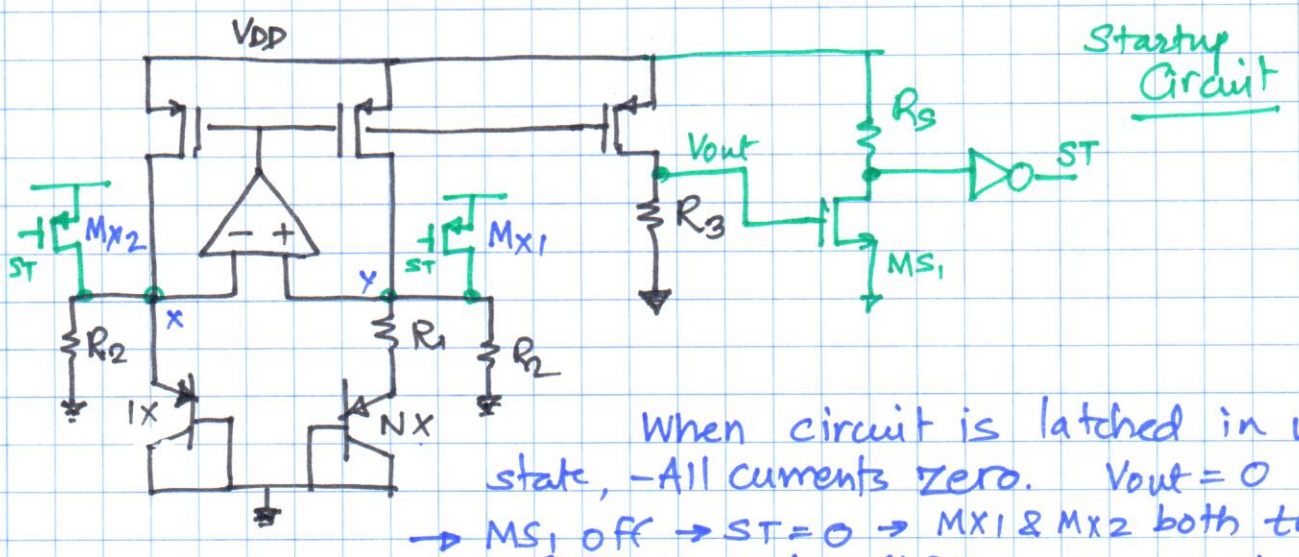
✱ Bandgap Startup Problem

→ Undesired Stable solution. - All currents zero.

→ Can be observed when you ramp up power supply.

→ Startup circuit detects this condition & pumps in juice to get to desired operation point.

Startup Solution (one possible)

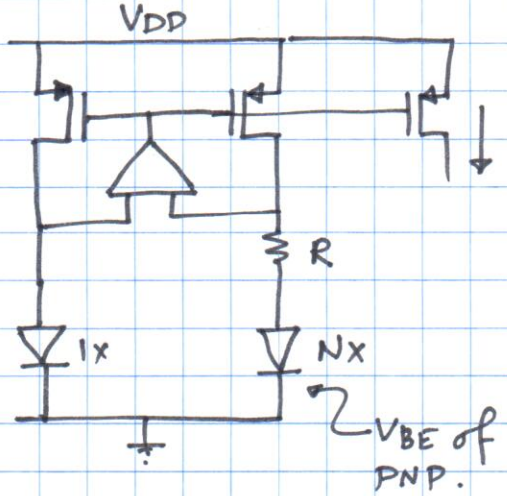


When circuit is latched in undesired state, -All currents zero. Vout = 0

→ MS1 off → ST = 0 → MX1 & MX2 both turn on

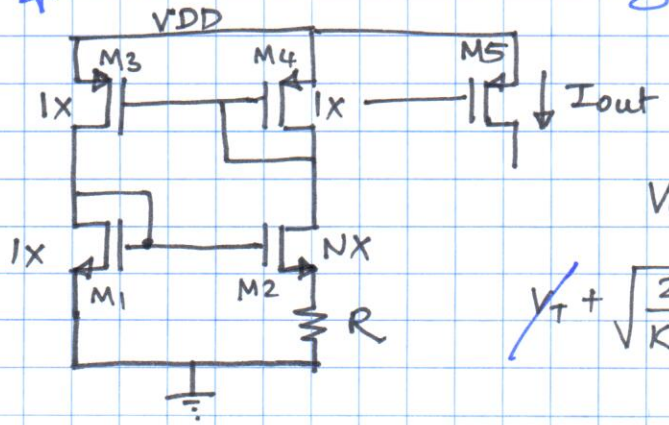
→ Lift both Nodes X & Y → Opamp starts to work.

✱ PTAT Current source



$$I_{out} = \frac{V_T \ln(N)}{R}$$

✱ Constant Gm Biasing → Gm → PVT independent



$$V_{GS_1} = V_{GS_2} + IR$$

$$V_T + \sqrt{\frac{2I}{K_n (W/L)_1}} = V_T + \sqrt{\frac{2I}{K_n N (\frac{W}{L})_1}} + IR$$

$$\Rightarrow I_{out} = I = \frac{2}{K_N\left(\frac{W}{L}\right)_1} \cdot \frac{1}{R^2} \cdot \left(1 - \frac{1}{\sqrt{N}}\right)^2$$

$$g_{m_1} = \sqrt{\underbrace{2\mu_n C_{ox}}_{K_N}\left(\frac{W}{L}\right)_1 I_1}$$

$$= \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_1 \times \frac{2}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}\left(\frac{1}{R^2}\left(1 - \frac{1}{\sqrt{N}}\right)^2\right)}$$

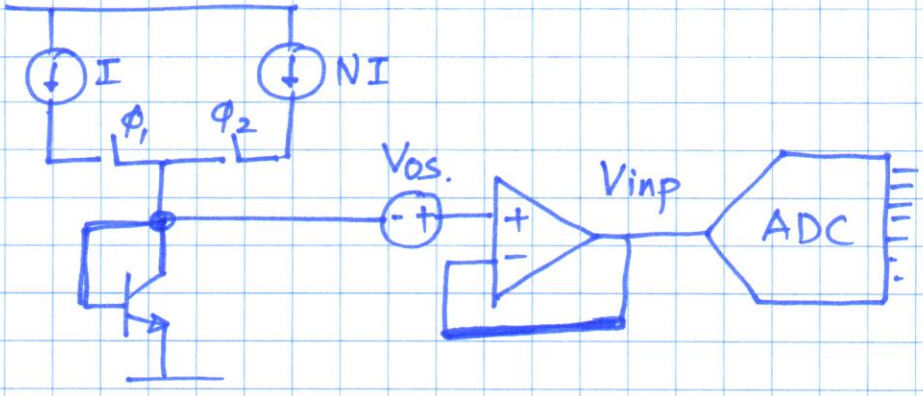
$$= \frac{2}{R}\left(1 - \frac{1}{\sqrt{N}}\right)$$

↑ on-chip or off chip

↖ Scaler Ratio

→ can be tuned digitally

On-Chip Temperature Sensor



In ϕ_1 $V_{inp} = V_{os} + V_T \ln\left(\frac{I}{I_s}\right)$

In ϕ_2 $V_{inp} = V_{os} + V_T \ln\left(\frac{NI}{I_s}\right)$

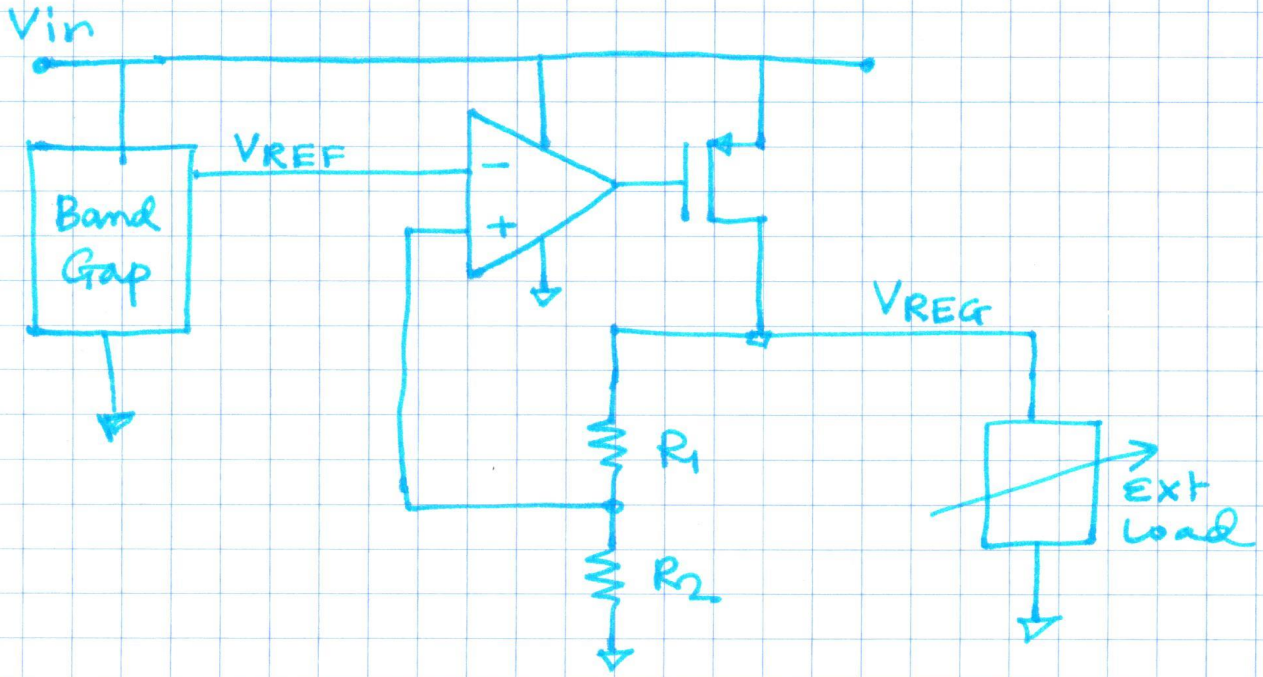
↘ A2D conversion & subtract digitally

Measure $V_T \ln(N)$ ⇒ Give T in °K

↑ Known Ratio

Voltage Regulator

→ is a constant voltage source independant of load current and input voltage.



→ V_{REF} — from Bandgap Reference. ~ 1.2V

→ Error Amplifier — OTA

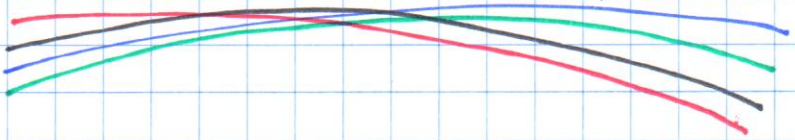
→ Feedback Network

→ Pass Transistor — V_{SG} increases as I_L increa

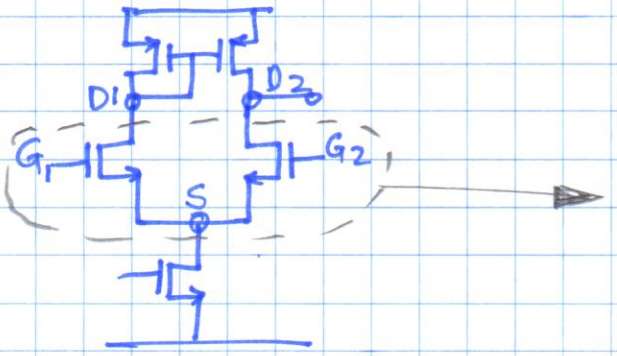
PMOS — large. — should be able to carry desired max load current.

$$V_{REG} = \left(1 + \frac{R_1}{R_2}\right) V_{REF}$$

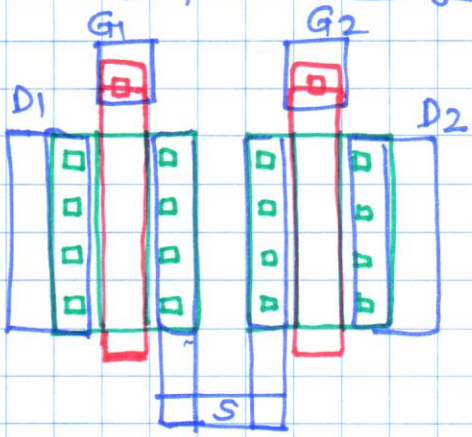
ANALOG LAYOUT TECHNIQUES



Schematic design



Layout design



In schematic design, only internal device parasitics are modeled for purpose of simulation.

Layout → Placement of all mask layers to create devices & interconnect. – New parasitics R, LC are added. when layout is created. – Can degrade performance of your circuits.

Circuit Design Engineer → EE background

Layout Design Engineer → Artists., good Engineering drawing skills
3.D visualization

Overall responsibility → you. as design Engineer

Layout Design.

DRC Design Rule Checks

— Guarantee Functional transistor & interconnects. in presence of process variations.

* Min Width.
* Min. Enclosure
* Min Spacing
* Min Extention.

Caliber tools

LVS Layout Vs. Schematic Check.

→ Layout → Netlist ↘ identical check.
Schematic → Netlist ↗ Device sizes same.

ERC Electrical Rule Check.

→ Electrical Connection of all wells, substrate
→ Devices connected to proper supply voltage
1V device → 1V supply.

Extraction PEX, RCX.

parasitic
→ R - only Resistance extracted - IR drop.
→ C → only p. Cap. extracted (to gnd)
→ CC → coupled cap. extracted (to adjacent lines)
→ R+CC → Final verdict for simulation.

→ L extraction → painful with std. tools
→ EMX used to model par. inductor
2-d simulator — Ind. Standard.

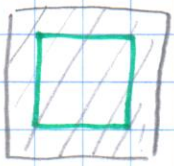
Crosssection of CMOS Technology.

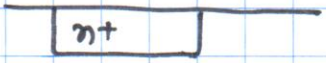
Reference: Chapter 18. Razavi CMOS Proc. Tech.
→ Review.

Slides discussed in class.

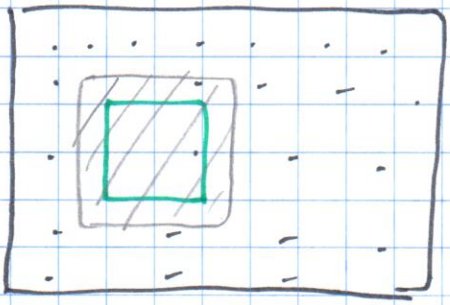
Nwell. poly Diffusion

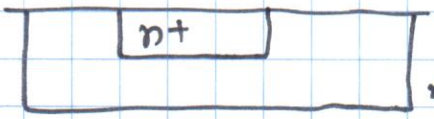
N type p-type



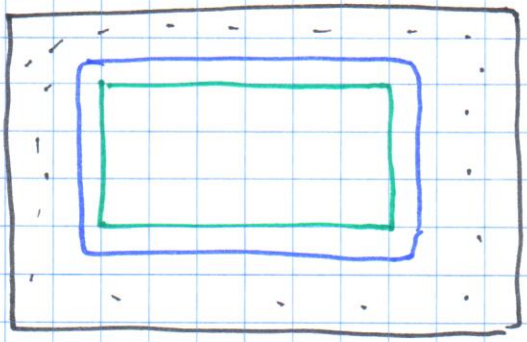


Diode

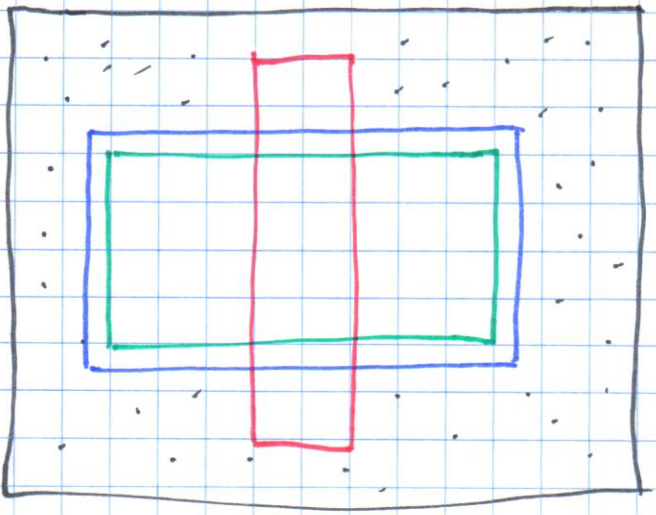


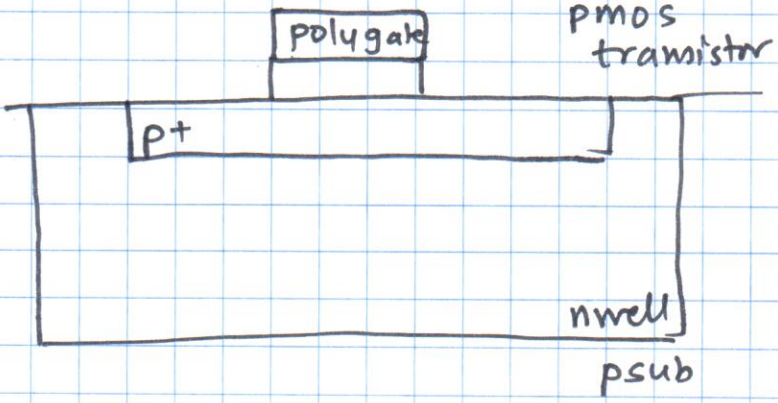


n-well contact



p+ - nwell diode





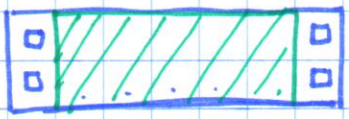
pmos transistor

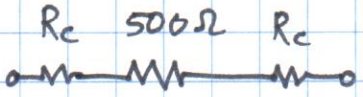
Device Parasitics

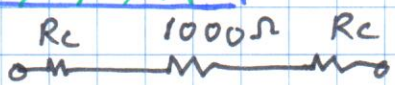
1. Resistor

$R_1 = 500\Omega$

$R_2 = 1000\Omega$





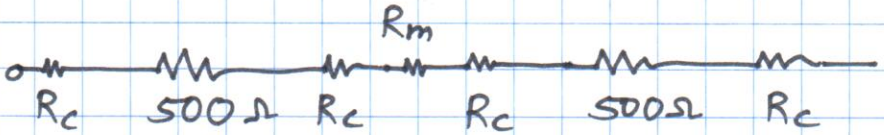


R_c - contact Resistance
- parasitic.

generally much higher than Metal R

Will NOT Match

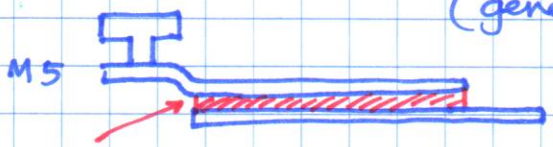
Better implementation



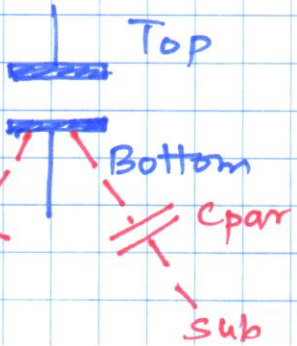
R_m - metal R
R_c - contact R
$R_m \ll R_c$

2. Capacitors

MIM - Metal Insulator Metal Cap
- Requires special mask layer to create thin oxide between two metals. (generally top two metals)

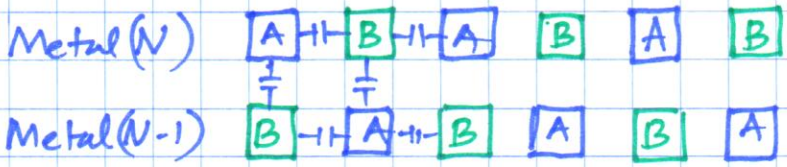


Thin ox - special mask layer



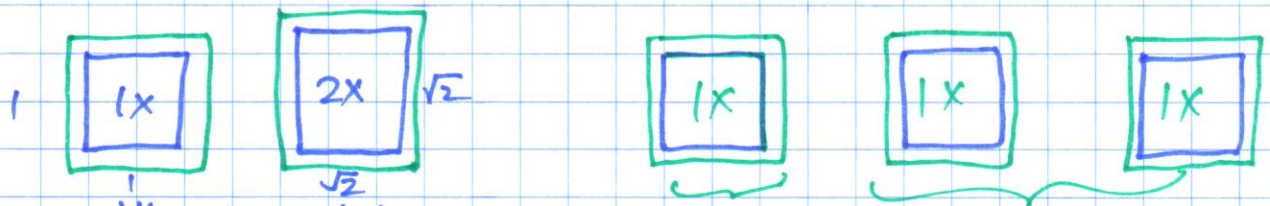
Bottom plate has large parasitics
← Try to use it as gnd connect.

MOM capacitor Metal Oxide Metal
— No special Mask needed



Good density in high Metal layer count process.

Cap Matching



Will not match

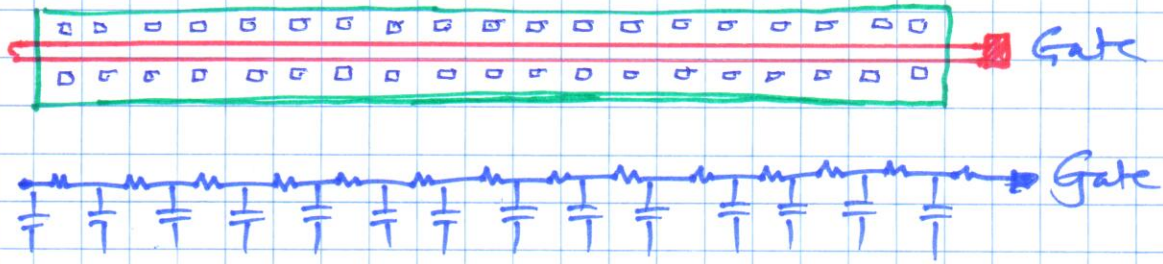
Better matching

→ Make sure you watch out for fringe cap.

→ Keep identical environment around matched caps.

3. MOS Devices.

Consider Device size W = 10 μm L = 0.05 μm.



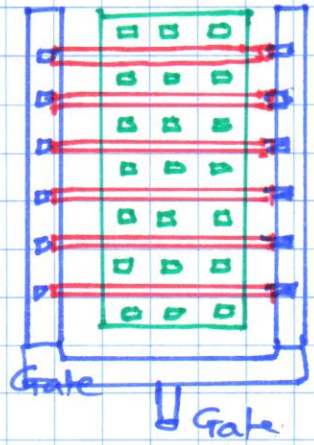
Long poly — large parasitic R + distributed cap.

→ Bad idea. → ↑ Noise

→ RC delay

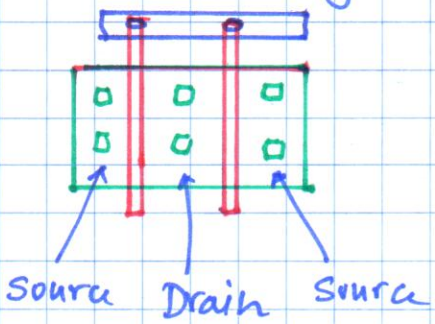
→ Cap Quality factor

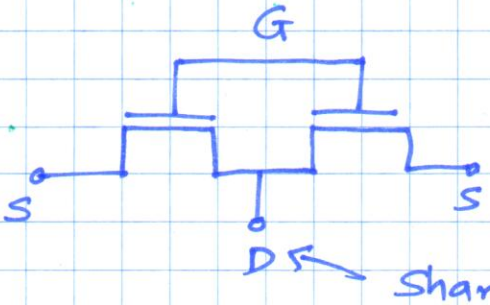
→ Increase number of fingers.
→ Connect gate with metal — poly resistance >> metal R.



→ Minimize gate resistance - RF performa

Reducing Drain Parasitics — Shared drain





Shared drain
→ Reduced parasitics

Well or Substrate connection for NMOS / PMOS

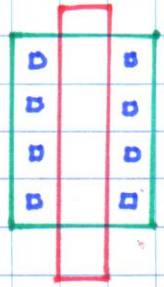
↳ Latchup consideration → Should have connection every 10 x 10 μm space (for example)

→ Connect to indiv. transistor or @ block level } judgement based on applicatio

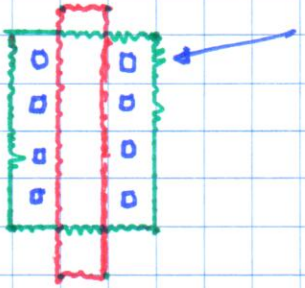
Matching

- Global variations
  - die 2 die
  - far away on same chip.
- Local Variations
  - mismatches
  - ↳ devices next to each other

Random Mismatch



Layout view



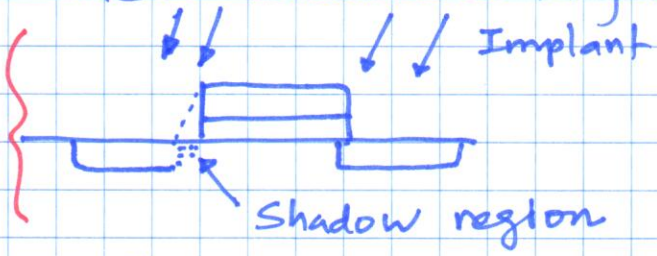
Actual After fabrication

Edge Effects due to
- → Etching uncertainities
- → Lithography

Matching Improves with increase in area (WL)
↳ Edge effects get averaged.

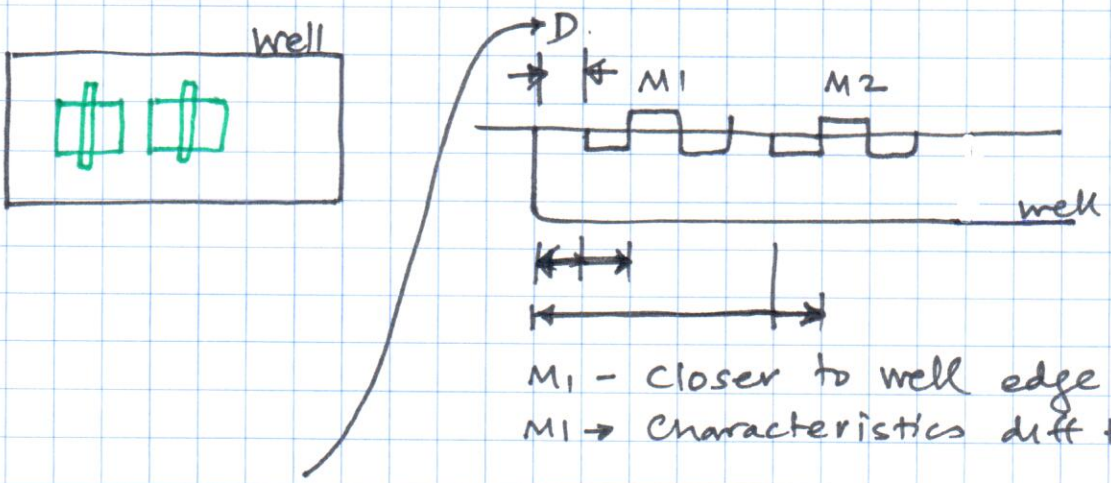
Process Variations → Due to inaccuracies in fab.

- → Mask Alignment
- → Shadowing effect



- → Proximity Effect
  - → Well prox. WPE
  - → STI - Shallow Trench Isol^{n}
- → Gradient Effect
- → Lateral Diffusion.

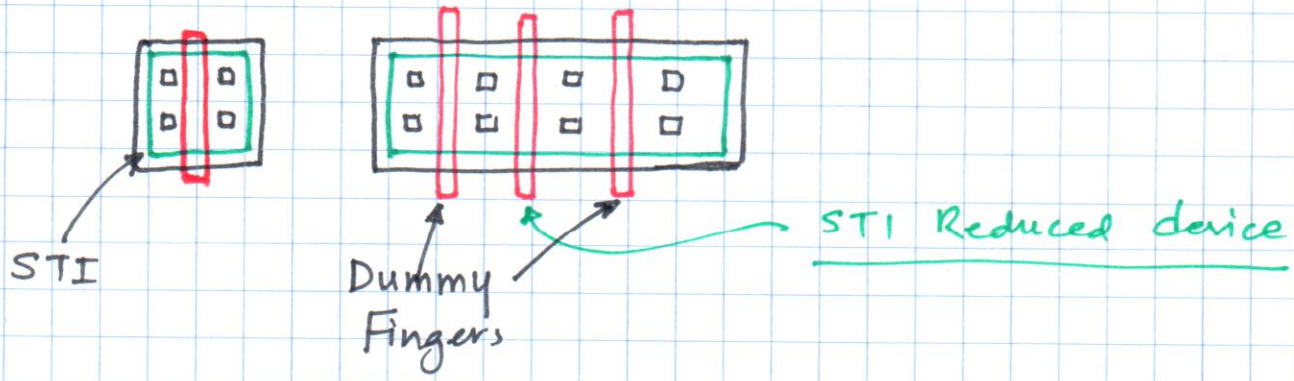
* WPE Well proximity effect



M_1 - closer to well edge than M2
M1 → Characteristics diff than M2

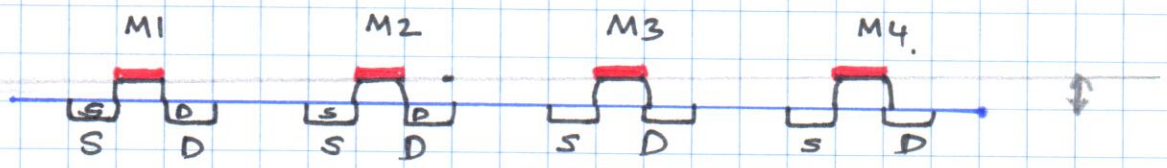
Increase D so that WPE is minimal.

* STI Shallow Trench Isolation effect



STI - to avoid formation of device between adjacent transistors. - Oxide trench. - Stress effect.

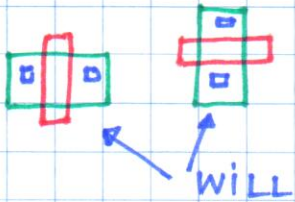
* Gradient Effect



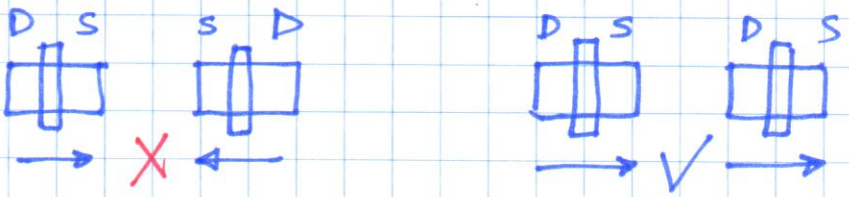
M4 & M1 will not match.
→ Common Centroid layout so that two dimentional gradient is cancelled out.

Critical Matching

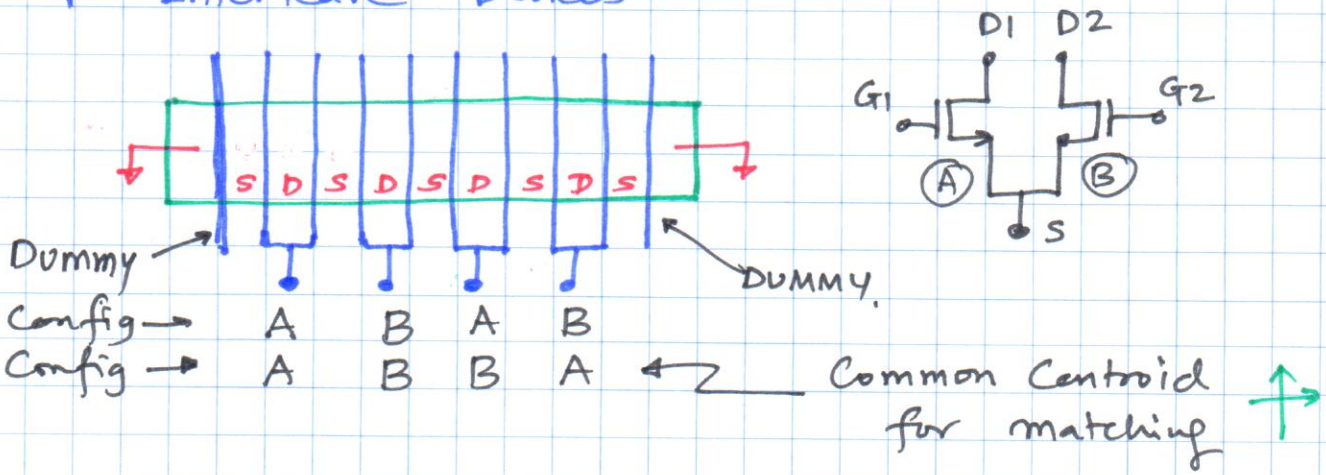
* Unit Cell layout
* Device orientation



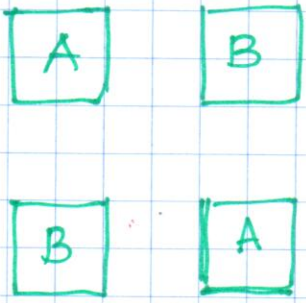
* Direction of current flow



* Interleave Devices



* Common Centroid layout



Gradient in any direction cancelled.

Keep dummy devices around matched devices to reduce edge effects.

* INTERCONNECT

→ parasitics R, L, C ↔ MINIMIZE / SYMMETRICALIZE"

High current lines – reduce R → IR drop ↓

High Frequency signals → Reduce C → Loading ↓

General Guideline

Use M1-M3 (lower Metals) for DC bias signals (Thin metals)

Use M_4-M_5-M_6 (High Freq) Signal Lines

↳ Reduce parasitic cap to substrate

Use Top thick metals (very low R) 2x, 4x thickness

↳ for VDD, GND lines.

Make these fat.

DO NOT SKIMP ON Metal.

(avoid overlap with signal lines)

In 28nm & below → Electromigration concern.

→ Burnin Issue.

Metals can carry limited current (Metal Width Shrinking)

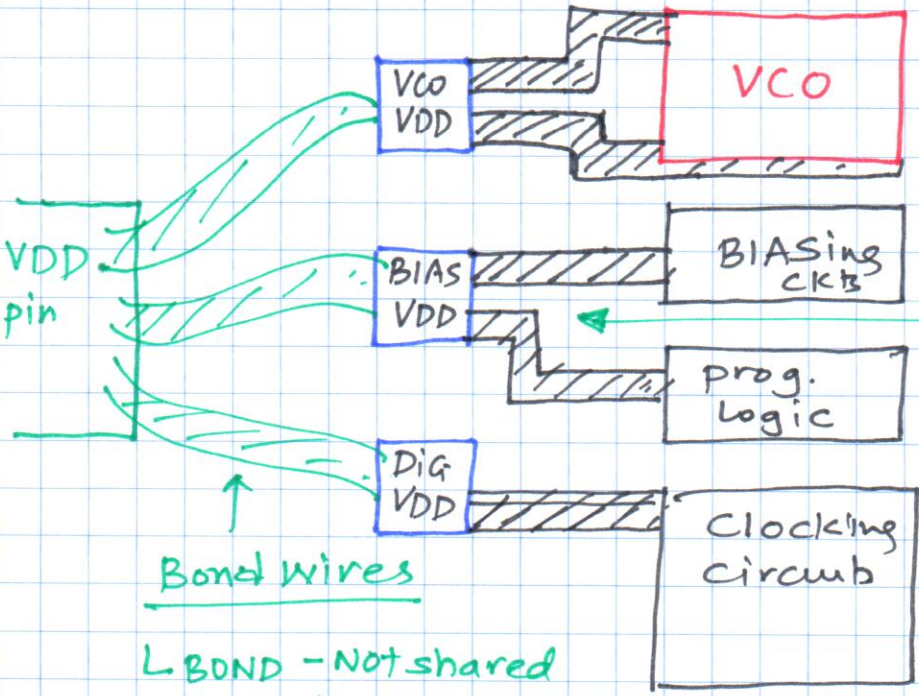
Strong Temperature Dependent

	115°C	125°	
1μm M1	X mA	0.7X mA	30% less.

→ CAD tools can be utilized to identify violation.

Voltus Fi

✱ Supply / Ground connections



✱ connection used.

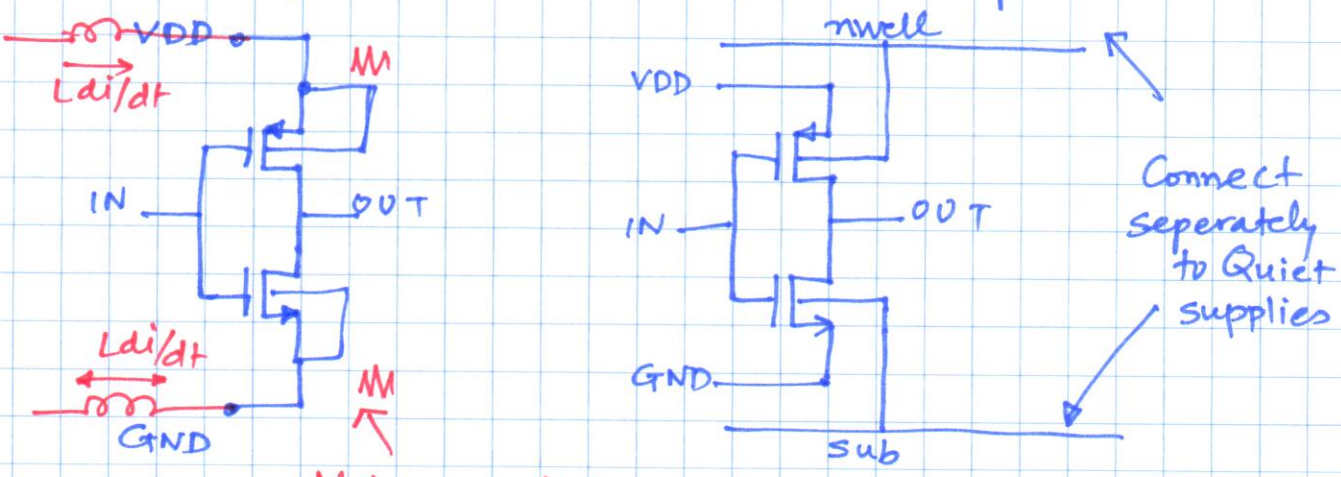
IR drop NOT shared

L_{BOND} - Not shared

$L\frac{di}{dt}$ → Noise coupling avoided.

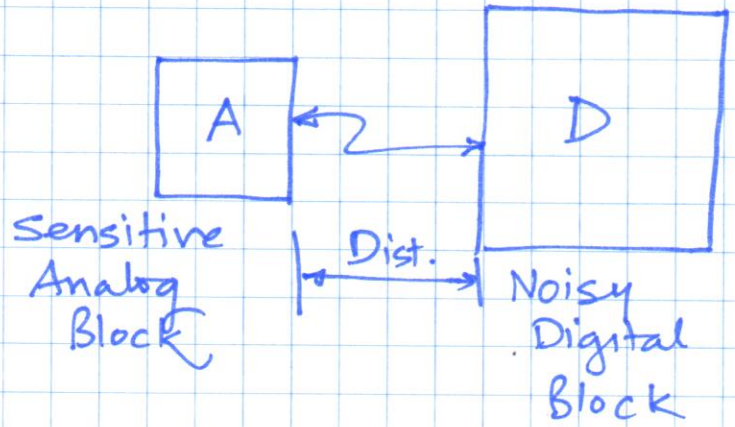
✱ Substrate & Well connection

→ Important to avoid latchup.



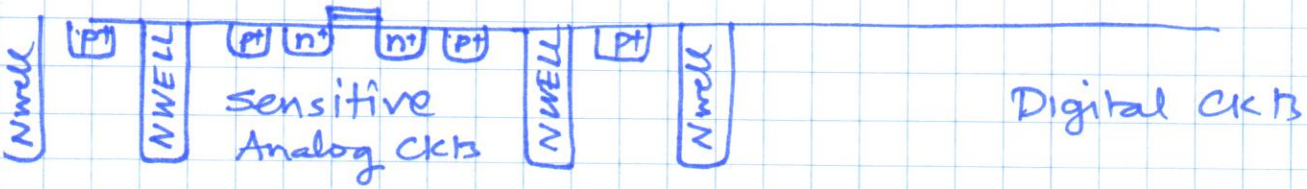
Locally generated noise (switching) is not transmitted to other (sensitive) circuits

✡ ISOLATION & COUPLING

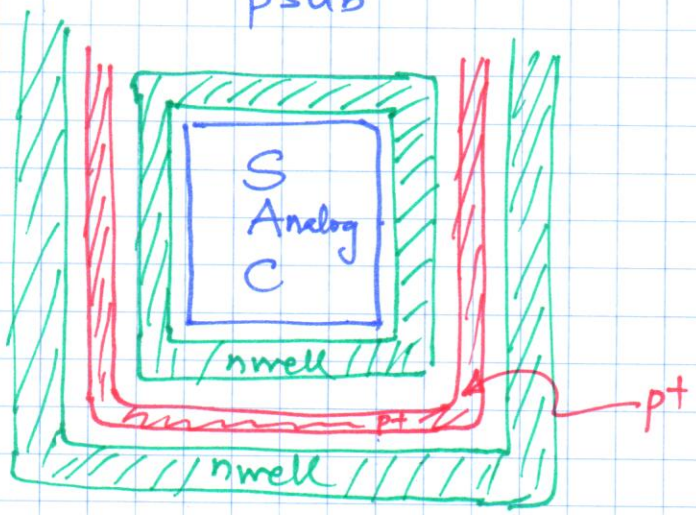


① → Maximize Distance D — Die area issues.

② → Guard Rings.



psub

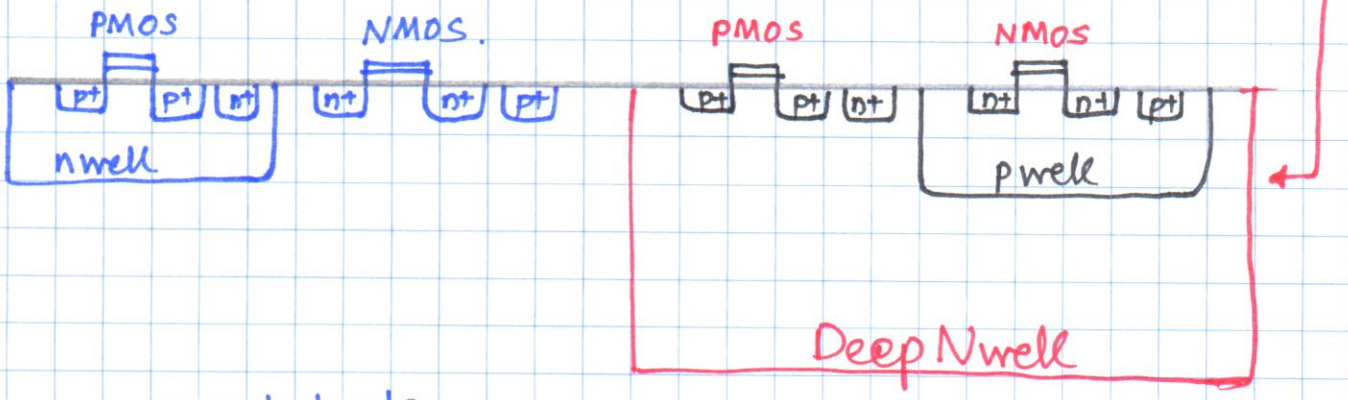


Like Moat around castle.

③ → Create isolated (Electrically) substrate

Deep-Nwell → Extra Mask Layer

Great for RF-Mixed Signal SOCs.



p-substrate

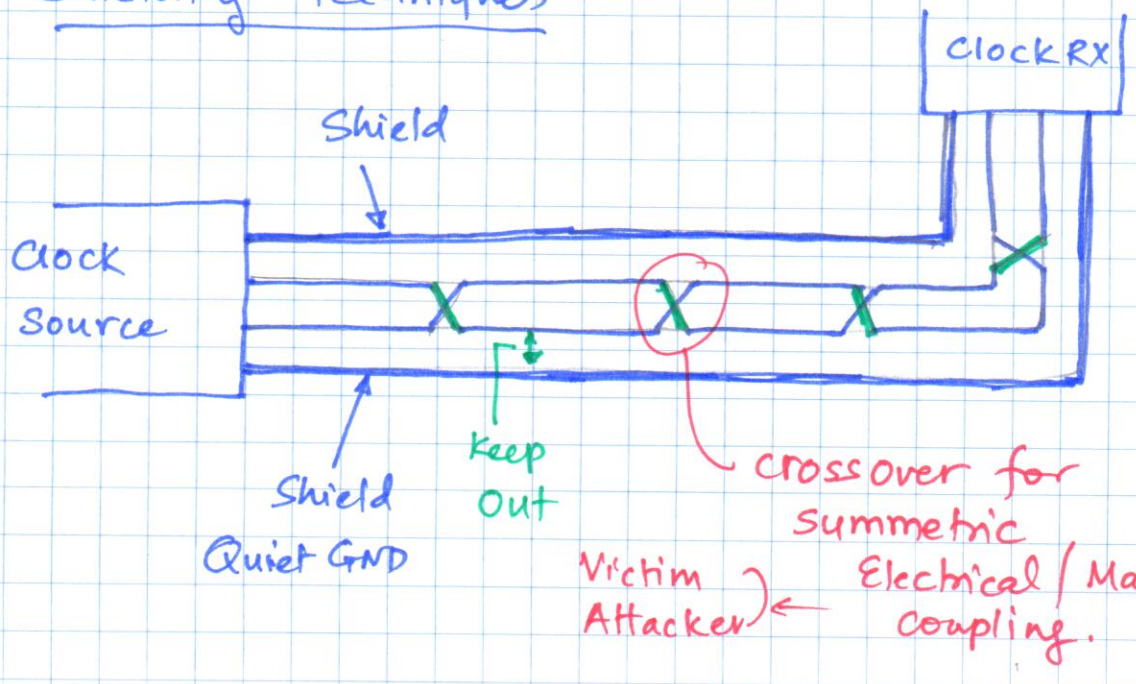
NMOS - in bare substrate

Body connection - sub → common ground

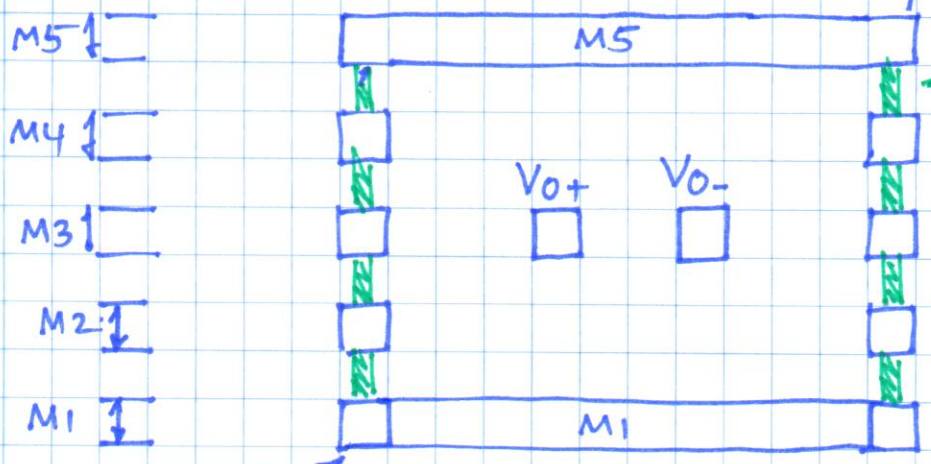
→ NMOS in isolated pwell.

→ Each Nmos can have separate well connection → isolated from substrate noise.

④ Shielding Techniques



Extra Shielding → Really Really Sensitive lines



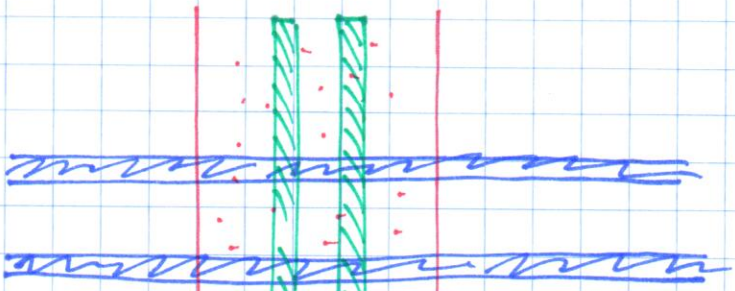
Coax Cable Type structure

2 CROSS-SECTION

Use M4 or M2 for crossovers

Connect Shield to good analog ground.

↳ Quiet with Low ohmic ~~resistance~~ impedance @ frequency of operation.

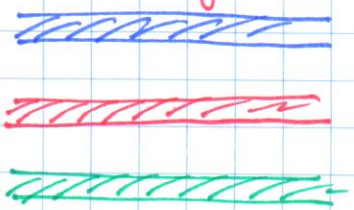


sensitive RF Lines.

Shield Metal (sandwitched)

Connect to good/Quiet AGND.

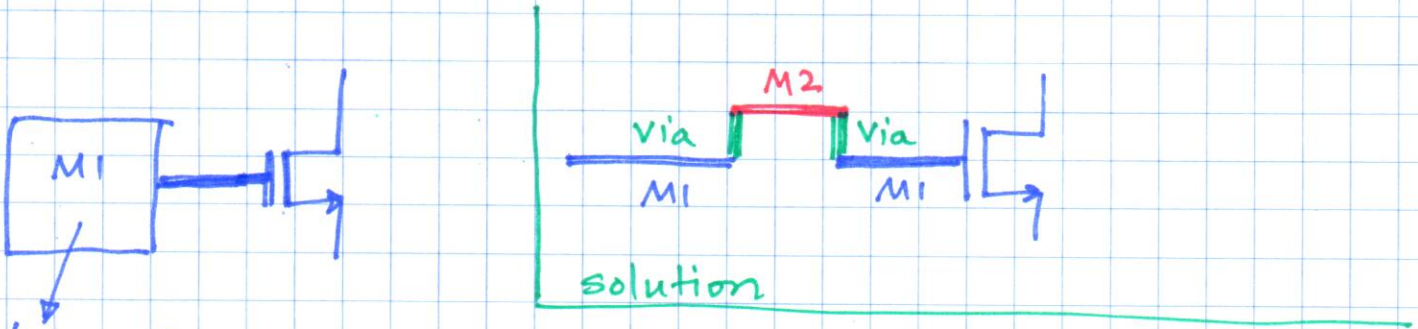
Noisy Digital Clock lines



Metal Stack crossection

Other Important Issues

✡ Antenna Effect



large piece of metal 1 Routing etc. → Collects ions/charge during etching + damages gate oxide.

→ Checked during DRC

✡ Metal Fills

In advance CMOS processes, with high number of metal layers, metal density needs to be carefully controlled within certain range.

→ depends on Fab requirement

→ Driven by Chemical Mechanical Polishing
→ plannerization of all metal layers

→ Design for manufacturability

→ After all Chip layout done
↓ auto tool adds/sprays sparkles of metal pieces to meet foundry requirement

→ Pieces of metal over sensitive circuits

can mess up symmetry, added coupling etc.

→ Do metal Fills @ block level

→ RF/analog senitive blocks – do manual fill & then extracted sims with fills

→ Can be a show-stopper if done@ last min.

✡ Planning For Metal Mask Changes

→ Assume you will have bugs

→ Add programmability / flexibility (digital)

→ Observability (test o/ps)

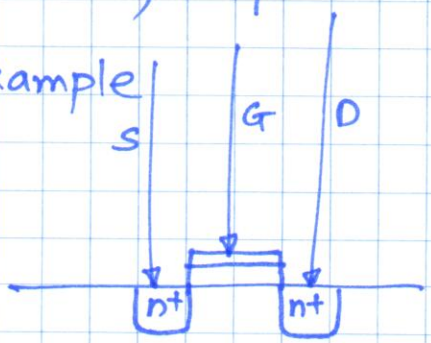
→ Add CyA-CyB circuit

→ Make sure you can use top metals to fix connection

Top metal mask 10K $

M1, Poly 50-60K $.

→ Example



Bring all S, G, D on all metals.

← spare kit

→ Keep them as fillers in empty spaces.

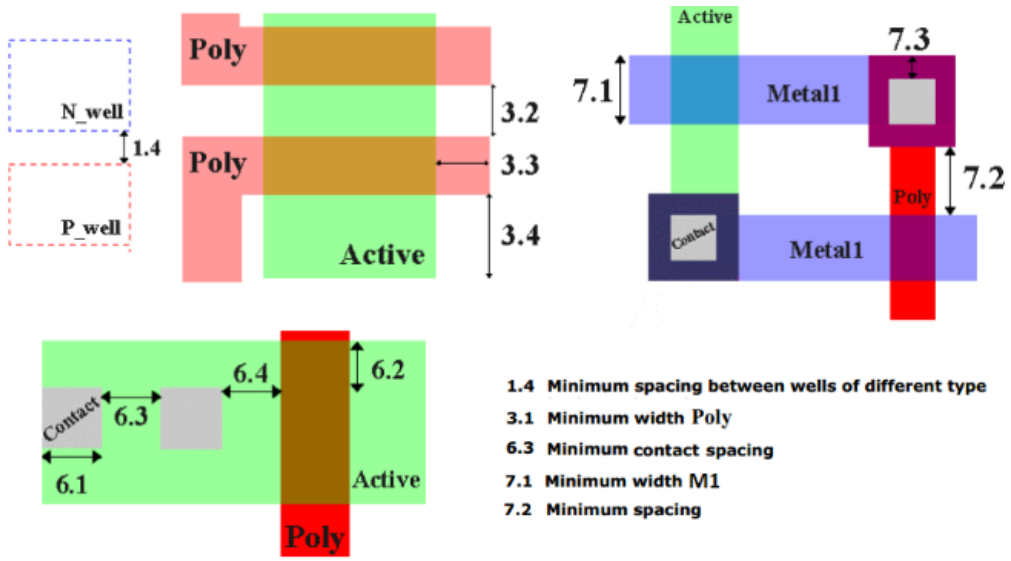
✡ Chip Planning

- City planning — architecture
- Board level layout / parasitics
- Supply / ground / Signal Routing @ board level
- Define package pin-outs / bonding diagram.
- Floorplan your chip — Analyze RF coupling issues
- Signal / Clocks / Vdd / Gnd flow
- Isolation between sensitive circuits
- Digital Circuits can also fail due to IR drops. Check VDD / GND IR drops
- Top level (chip level) connectivity Check
  - → Simulate → power up / down
    → Reliability Checks.
    → Electro-migration checks.
  - → make sure circuits somewhere else is not interacting with your ckts.
  - → Sensitive Routing R/L/C extraction to gain confidence

→ Just Maskset for 28nm CMOS can cost ~ 1 million $.
+ 4-6 K$ per wafer processed.

(i) Use all neurons / compute power before tape-out.

Sample of Design Rules provided by the foundry
(Below shown rules doesn't correspond to SCL process)

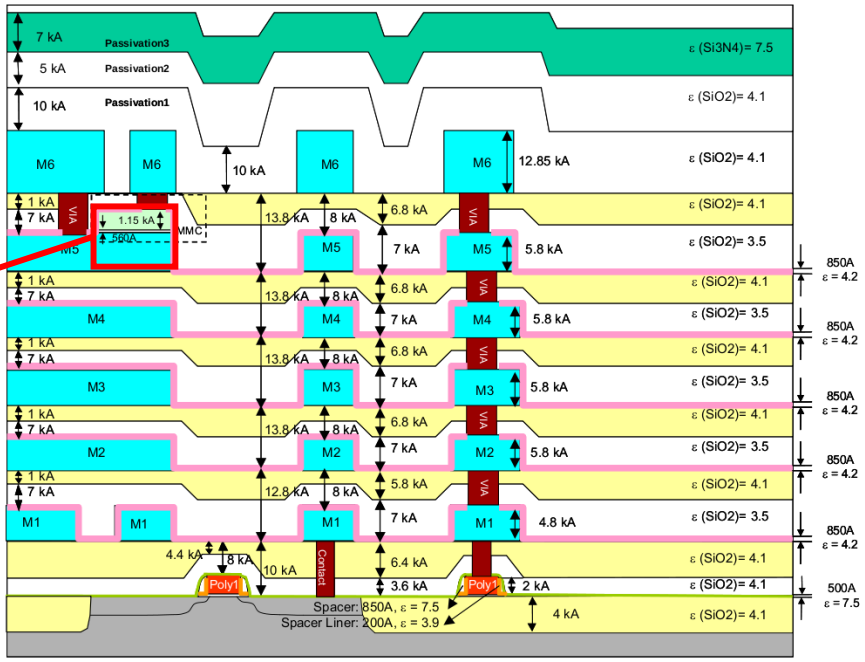


1.4 Minimum spacing between wells of different type
3.1 Minimum width Poly
6.3 Minimum contact spacing
7.1 Minimum width M1
7.2 Minimum spacing

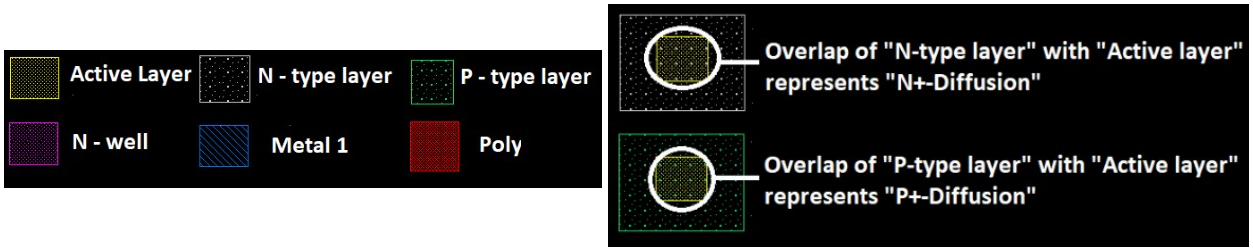
Interconnect layers (Doesn't correspond to SCL process)

MIM Capacitor
Top plate connected to M6
M5 acts as bottom plate

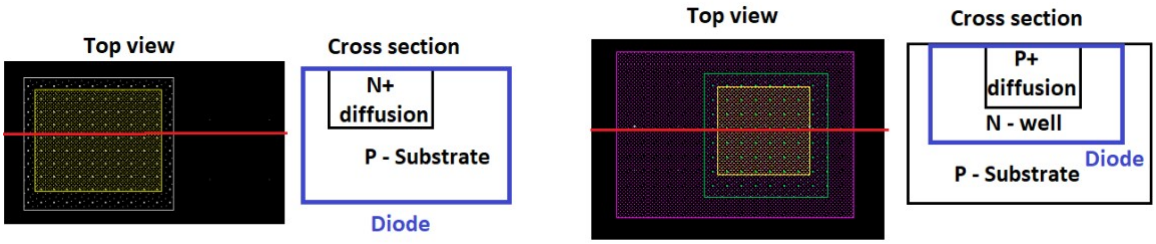
Dielectric thickness = 56nm



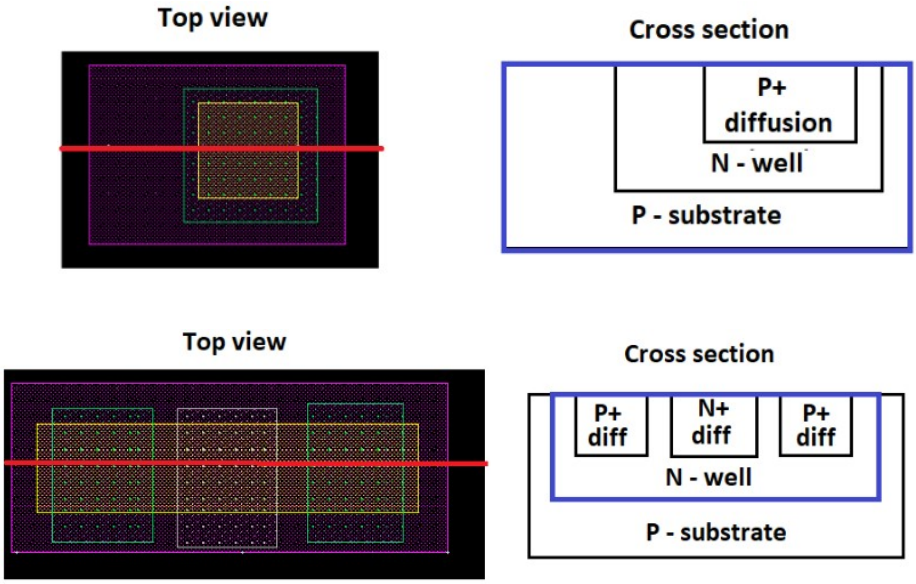
Basic Layers in SCL 180nm


Active Layer
N - type layer
P - type layer
N - well
Metal 1
Poly
Overlap of "N-type layer" with "Active layer" represents "N+-Diffusion"
Overlap of "P-type layer" with "Active layer" represents "P+-Diffusion"

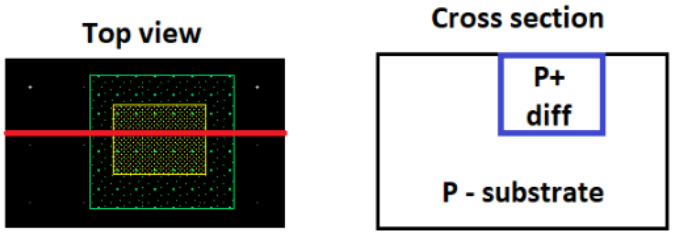
Different ways of forming Diode

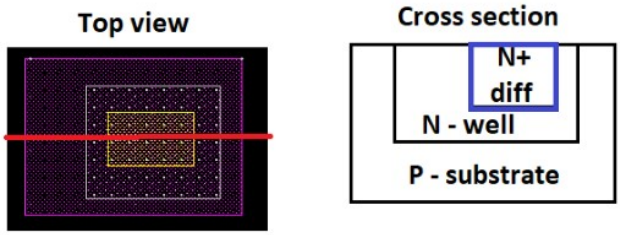


Different ways of forming BJT

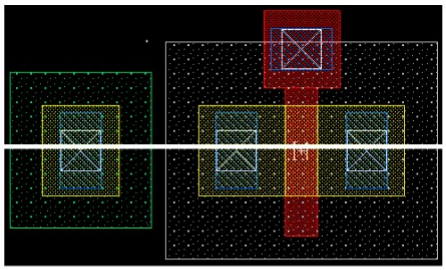


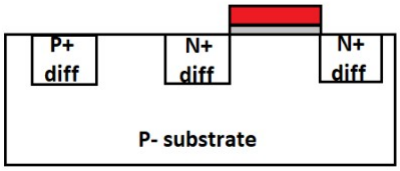
Contacts to regions





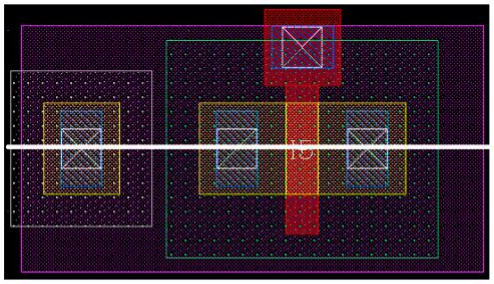
Top View of NMOS

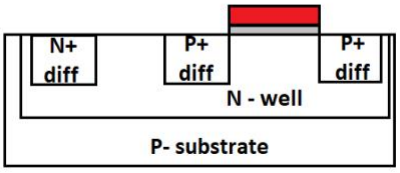




Cross sectional view of NMOS

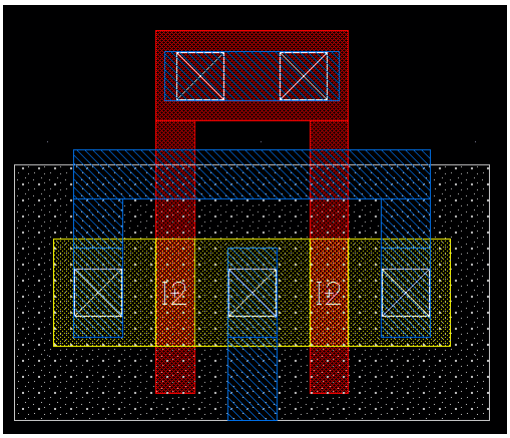
Top View of PMOS



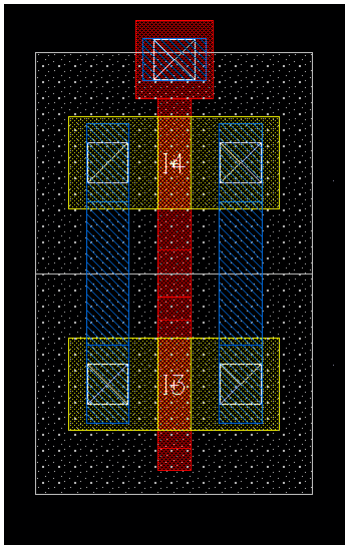


Cross sectional view of PMOS

NMOS
Total width = (0.5um) x 2 fingers = 1um
Length= 0.18 um

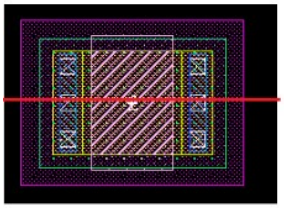


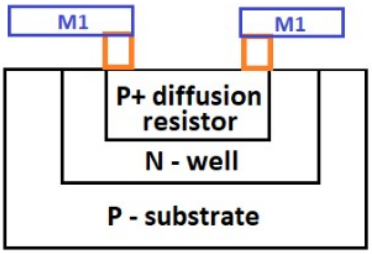
NMOS
Total width = (0.5um) x 2 multiples = 1um
Length= 0.18 um



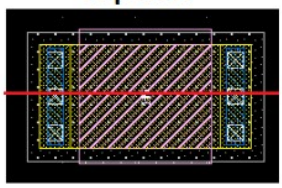
Diffusion resistors

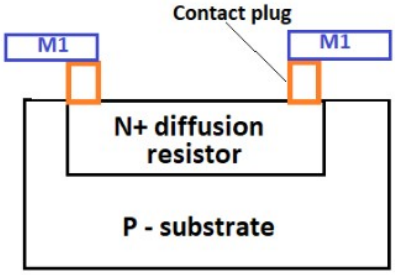
Top view



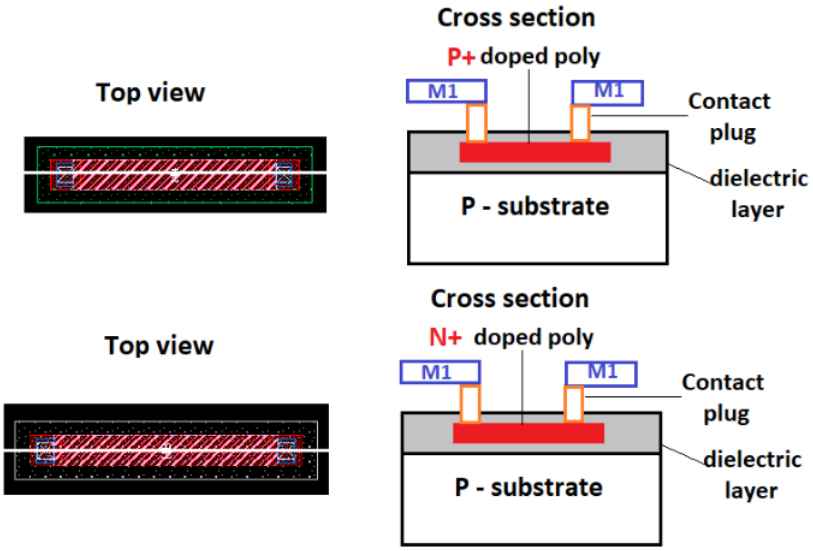


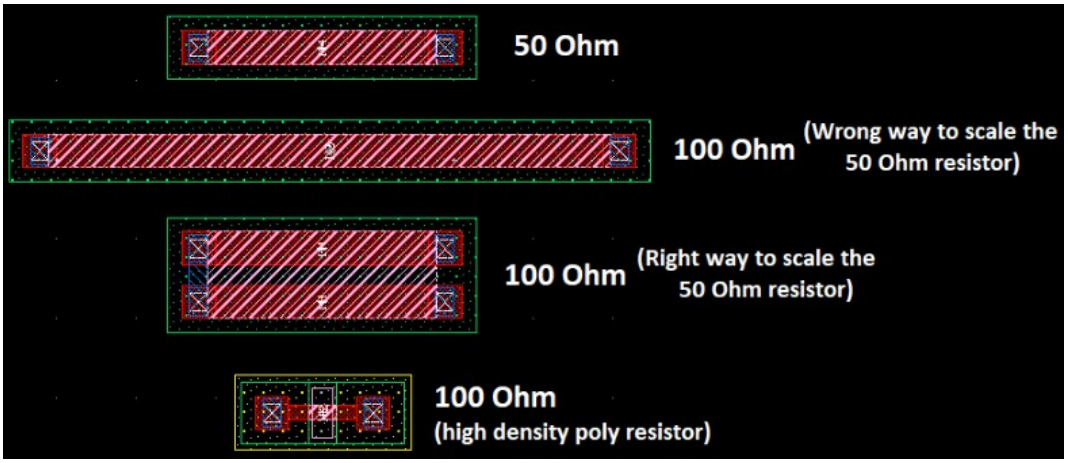
Top view



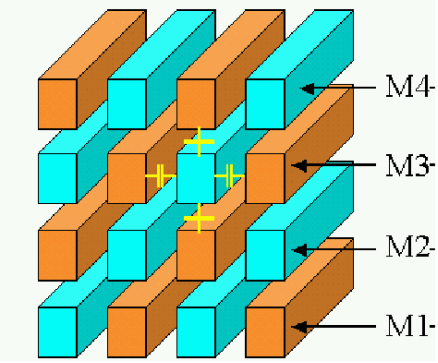


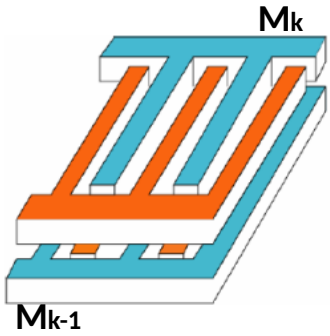
Poly resistors



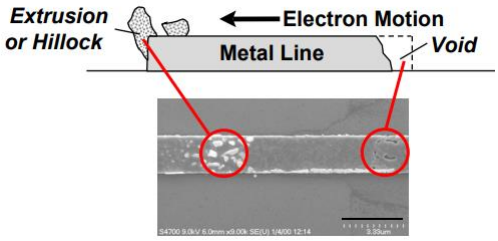

50 Ohm
100 Ohm
(Wrong way to scale the 50 Ohm resistor)
100 Ohm
(Right way to scale the 50 Ohm resistor)
100 Ohm
(high density poly resistor)

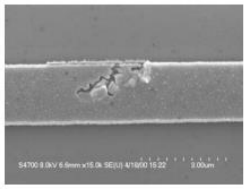
MOM Capacitors

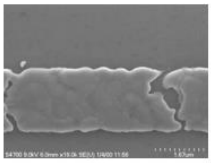


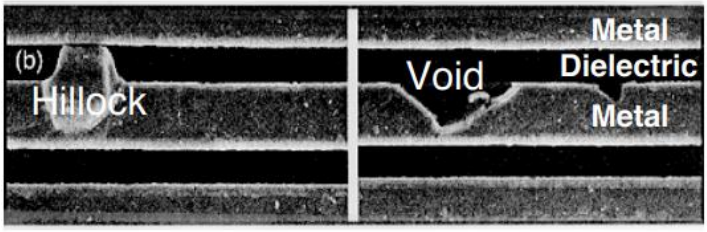


Electromigration failure



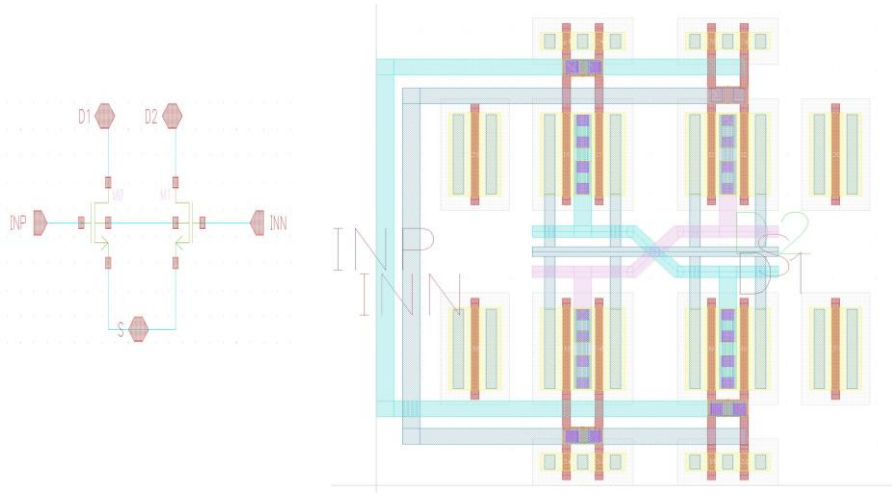




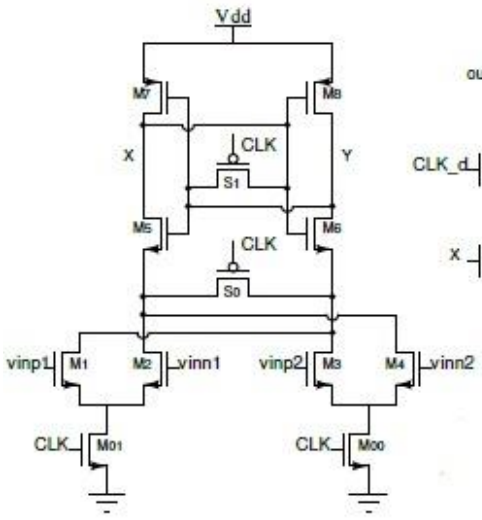


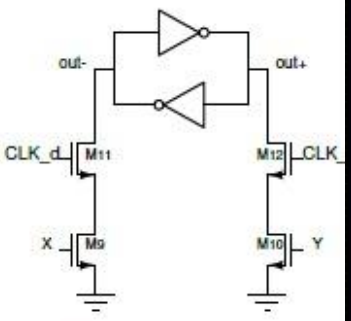
https://web.stanford.edu/class/ee311/NOTES/Interconnect_Al.pdf

Layout of the Input Pair of OpAmp using Common-Centroid

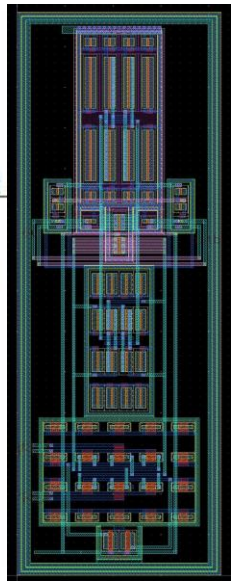


Comparator Schematic



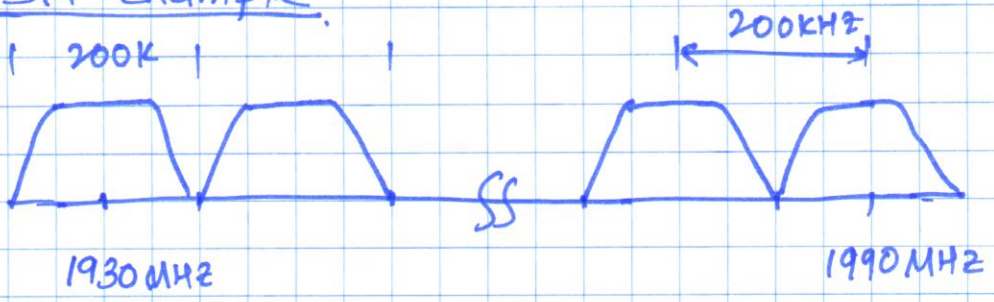


Layout



CONTINUOUS TIME FILTERS

GSM Example



AM, FM Radios – Common Medium Shared between multiple users.

Filters are used to provide frequency selectivity.

→ Keep desired spectrum (channel)
→ Attenuate undesired channels.

→ Wireline Communication Example

Filters used to compensate for Channel loss (frequency dependant)

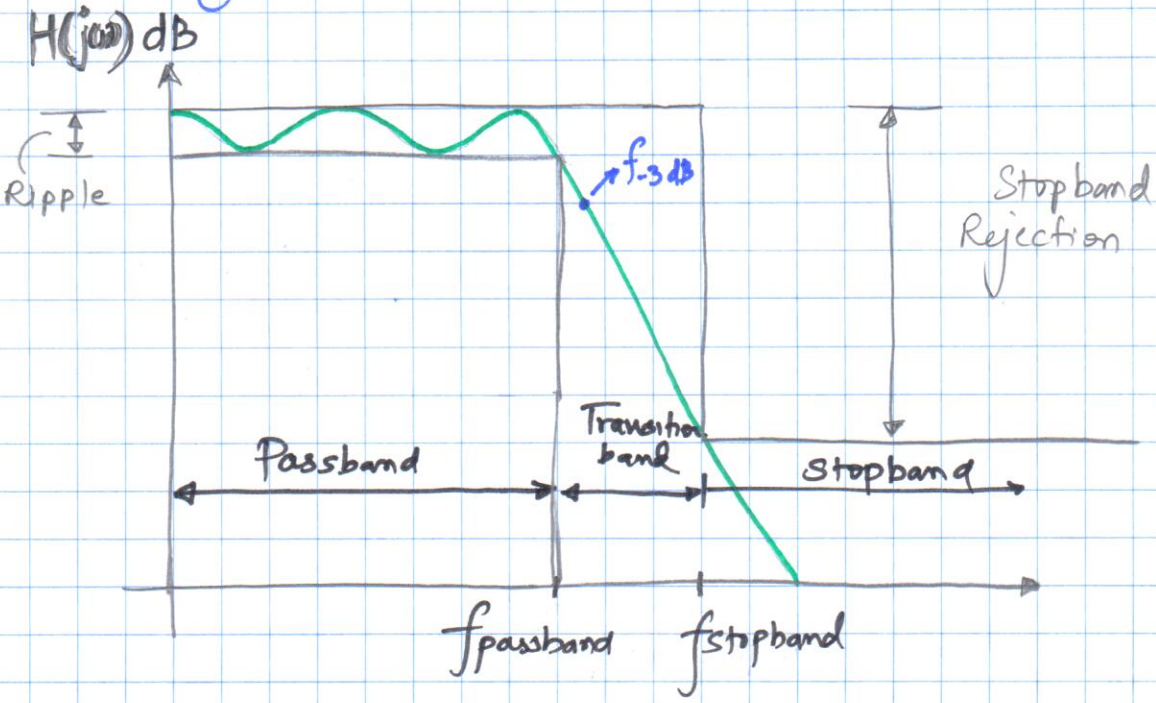
→ Equalization & pulse shaping.

→ Antialiasing filters for ADC

→ Smoothing filters for DAC.

Filter Specifications

Study Low Pass filters first – Then Xform to diff types.



Filter with transfer function H(s)

$$H(j\omega) = |H(j\omega)|\, e^{j\theta(\omega)}$$

Phase Delay $= \tau_{PD} = -\dfrac{\theta(\omega)}{\omega}$ (time units)

Group Delay $= \tau_{GR} = -\dfrac{d\theta(\omega)}{d\omega}$ (time units)

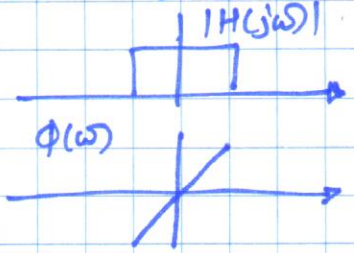
$\theta(\omega) = K\omega$ ← Constant — No phase distortion.

$\tau_{PD} = \tau_{GR} = -K$

Constant group delay.

→ This property is important for pulse-shaping in Wireline applications

Filter Approximations (Ideal Brickwall)



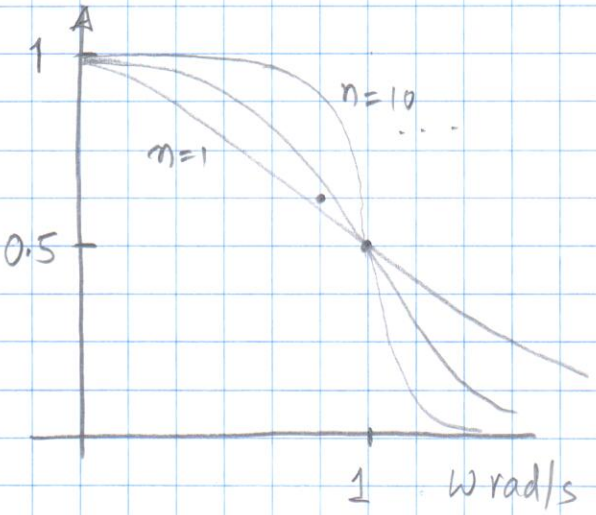
1. Butterworth Approximation

$$|H(j\omega)|^2 = \frac{1}{1+\omega^{2n}}$$

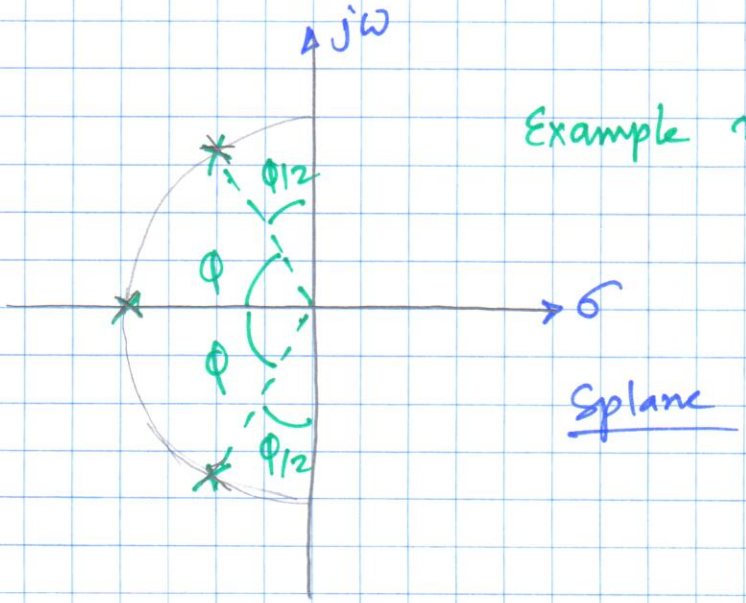
$|H(j0)|^2 = 1$; ~~$H(j0.5) =$~~

$|H(j1)|^2 = 0.5$

$|H(j\infty)|^2 = 0$

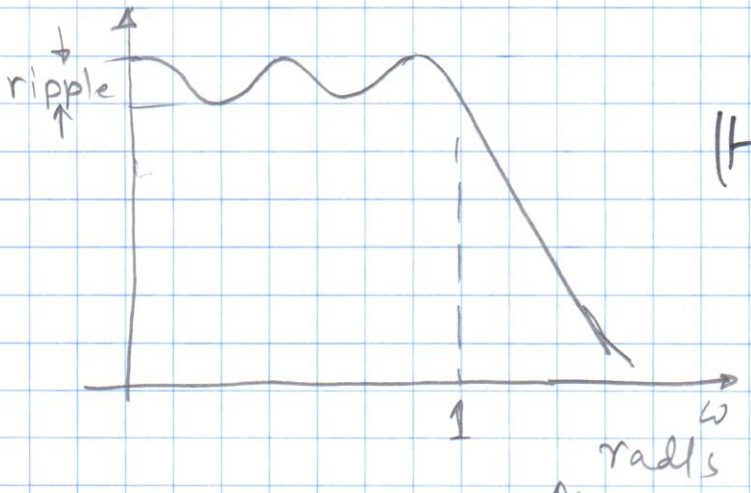


* Maximally flat passband @ $\omega = 0$.
* Moderate phase distortion. (Group delay)
* Poles located on unit circle



2. Chebyshev Approximation

→ keep attenuation in passband minimal
→ within Ripple spec.
→ Sharper transition band (compared to Butterw)
→ Poorer group delay distortion.
→ All poles located on Ellipse.

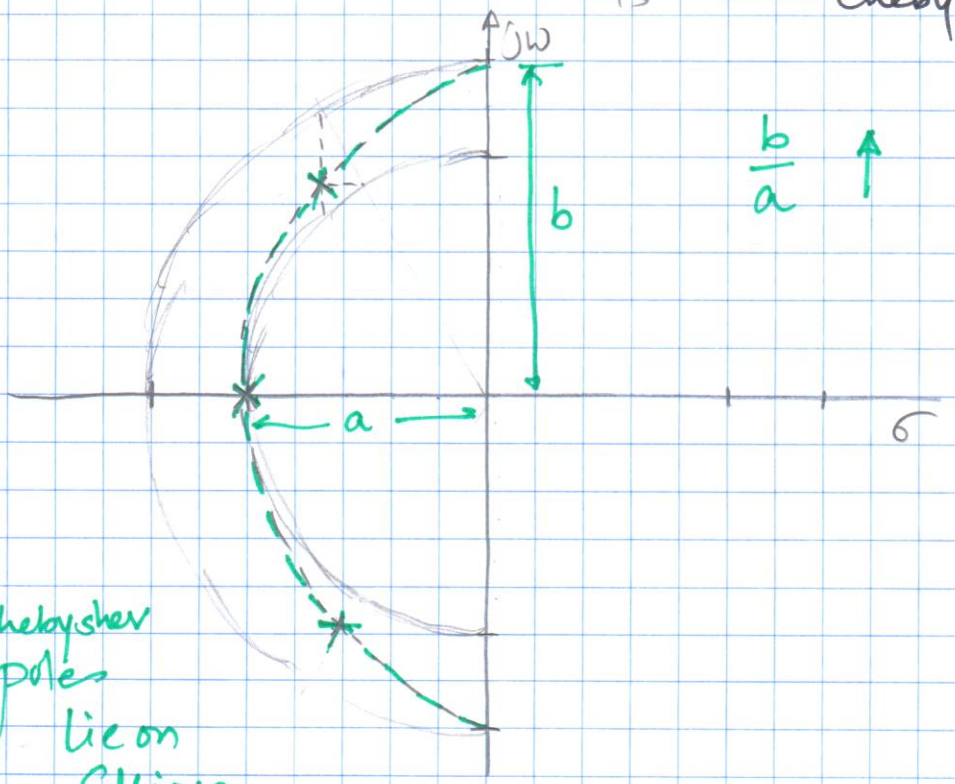


$$|H(j\omega)|^2 = \frac{1}{1+\epsilon^2 T_n^2(\omega)}$$

→ $T_n(\omega) = \cos(n\cos^{-1}\omega)$

ϵ - sets ripple amplitud

— Chebyshev polynomial (nth order)



$\frac{b}{a}$ ↑ ripple ↑

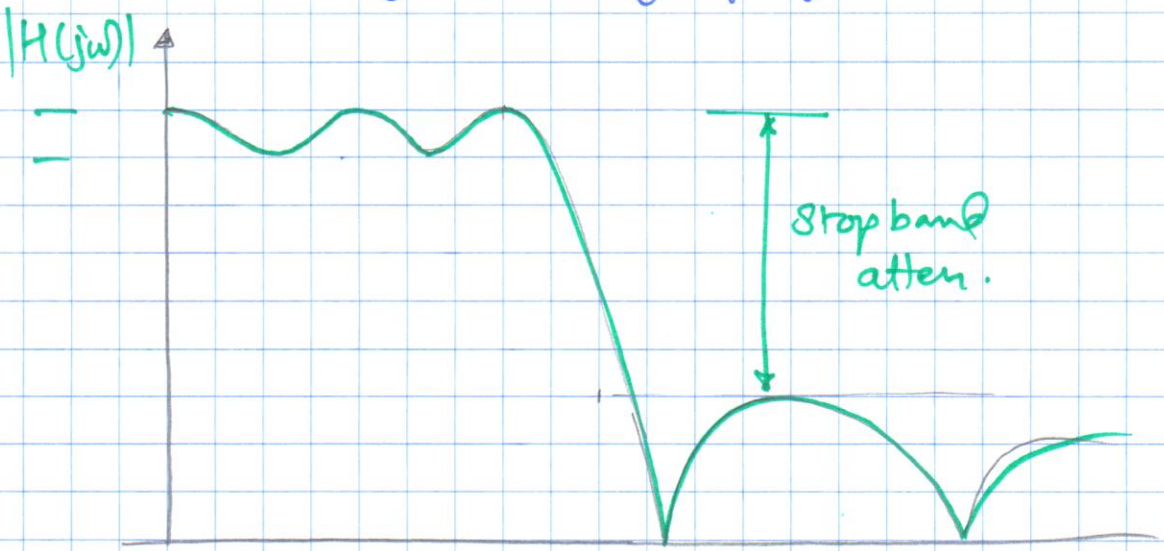
Chebyshev poles lie on Ellipse

3. Elliptic filters (Cauer filters)

→ Zeros in stopband, create nulls.

→ Very sharp transition band - highest atten with lowest order

→ poorest group delay performance.

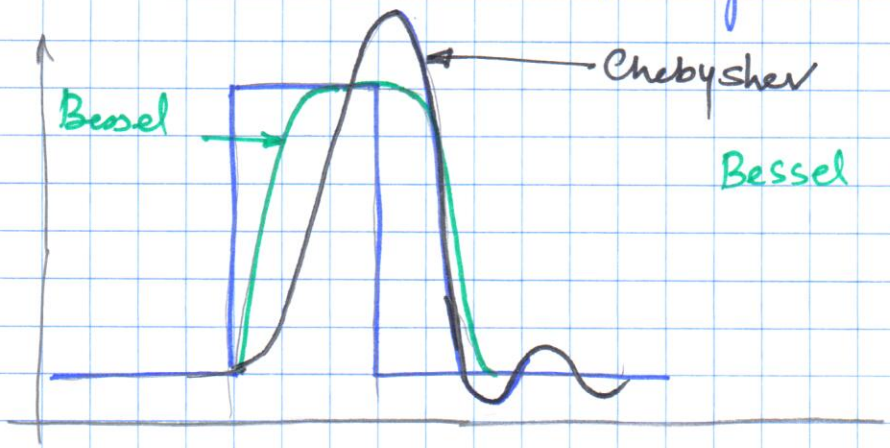


④ Bessel Approximation

→ Poles ~~on~~ outside unit circle (low Q)

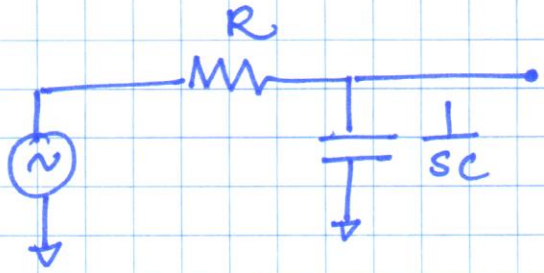
→ Maximally flat group delay

→ attenuation ∿ Not great.



Bessel - minimizes [S]

RC filter - 1st order Example

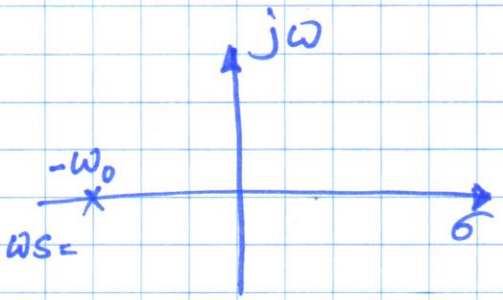


$$V_{out} = \frac{1/sC}{R + 1/sC} = \frac{1}{\left(1 + \frac{s}{1/RC}\right)}$$

$$\text{pole @ } -\omega_0 = -\frac{1}{RC}$$

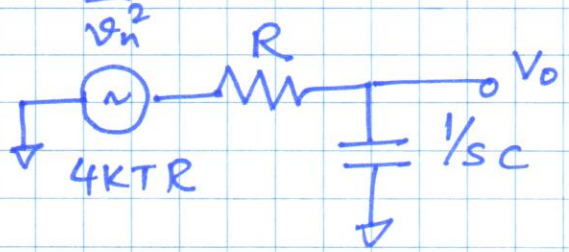
$$@\ s = j\omega_0 \quad |H(j\omega)| = \frac{1}{\sqrt{2}}$$

→ 3dB frequency



Note: parasitics across R will limit high freq. atten.

Noise Analysis



$$S_{out}(f) = 4KTR \cdot \frac{1}{4\pi^2 R^2 C^2 f^2 + 1}$$

Total integrated o/p noise

$$= \int_0^\infty \frac{4KTR}{4\pi^2 R^2 C^2 f^2 + 1}\, df$$

$$= \frac{kT}{C} \quad \text{indep of } R$$

Example 1pF cap → 64 μVrms @ 300°K

for complex filter (higher order)

$$\text{o/p noise} = x \frac{kT}{C}$$

x ↑ depends on order

Also - assumption - active circuits - lower noise.

$$\text{Filter Dynamic Range} = \frac{\text{Max Voltage Swing}}{\text{Min. discernible signal}}$$

Max Voltage Swing ← V_{DD}, Linearity

Min. discernible signal ↑ Noise

$$\text{Max Voltage Swing} = \frac{1}{\sqrt{2}} \frac{V_{DD}}{2} \quad \text{(Rms Voltage)}$$

$$\text{Min Voltage Swing} = \sqrt{x \frac{kT}{C}} \quad \text{(Rms Noise)}$$

$$DR = \frac{V_{DD}/2\sqrt{2}}{\sqrt{x \frac{kT}{C}}} = V_{DD} \sqrt{\frac{C}{8x kT}}$$

$$DR_{dB} = 20 \log_{10} \left(V_{DD} \sqrt{\frac{C}{8x kT}} \right)$$

$$= 20 \log_{10} \left(V_{DD} \sqrt{\frac{C}{x}} \right) + 75 \text{ dB}$$

(C in pF)

For $V_{DD} = 1V$ $C = 1pF$ $x = 1$

$$DR_{dB} = 75 \text{ dB} = (1.76 + 6.02N)$$

↑ # of bits

$N = 12$ bits Best possible

Reference - Haideh Khorramabadi classnotes.

FILTER DESIGN EXAMPLE

Design a Chebyshev filter to meet following req.

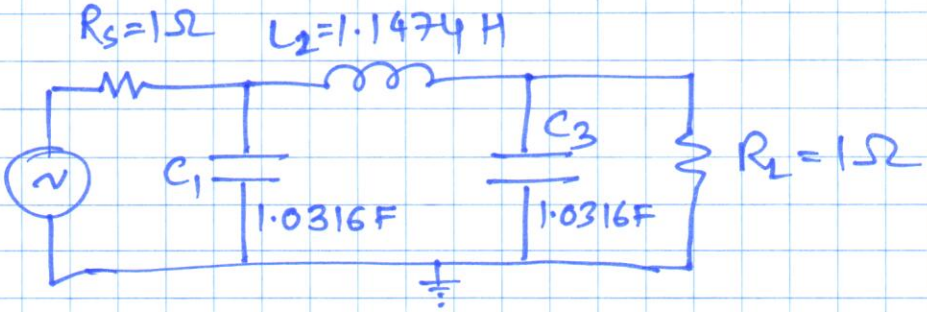
* 0.1dB ripple * 10MHz ripple BW.
* Stopband atten 40dB * Stopband 60MHz

→ Ripple BW/Stopband = 1/6

→ from 0.1dB ripple Chebyshev Atten chara. (Fig 8.15) for n=3 atten @ 6 rad/s = 42dB.

→ 3rd order filter

From Table 8-2

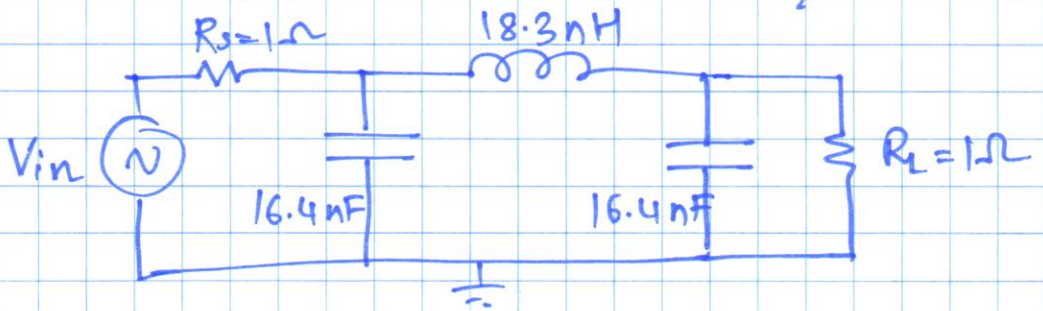


$\omega_{ripple\ BW}$ = 1 rad/s Desired $\omega_{ripple\ B}$ = 2π × 10 MHz = 62.8 M rad/s

$$C_1 = C_3 = \frac{1.0316\,F}{62.8\,M} = 16.4\,nF$$

$$L_2 = \frac{1.1474\,H}{62.8\,M} = 18.3\,nH$$

Impractical for IC implementation



ANALOG AND DIGITAL FILTERS: DESIGN AND REALIZATION

HARRY Y-F. LAM

Bell Telephone Laboratories, Inc.

Formerly with University of California, Berkeley

100680 Lam, Harry Y-F

Analog and digital filters : design

100680

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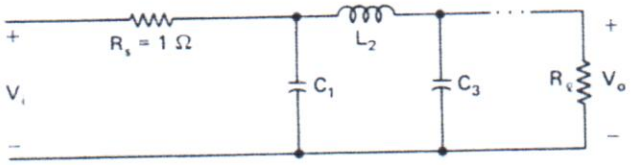
BUTTERWORTH FILTER



(c) $R_L = R_s$

Fig. 8-9 Circuit structures of low-pass Butterworth filters.

FILTER ORDER

TABLE 8-1 Element Values for the Circuit in Fig. 8-9(c)

n	C_1	L_2	C_3	L_4	C_5	L_6	C_7	L_8	C_9
1	2.0000								
2	1.4142	1.4142							
3	1.0000	2.0000	1.0000						
4	0.7654	1.8478	1.8478	0.7654					
5	0.6180	1.6180	2.0000	1.6180	0.6180				
6	0.5176	1.4142	1.9319	1.9319	1.4142	0.5176			
7	0.4450	1.2470	1.8019	2.0000	1.8019	1.2470	0.4450		
8	0.3902	1.1111	1.6629	1.9616	1.9616	1.6629	1.1111	0.3902	
9	0.3473	1.0000	1.5321	1.8794	2.0000	1.8794	1.5321	1.0000	0.3473

Chebyshev Filter

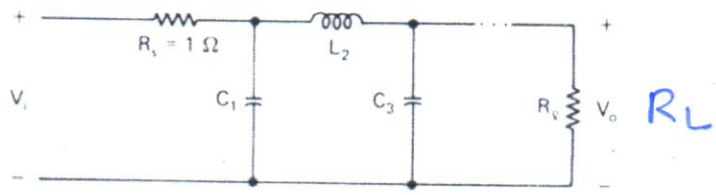


Fig. 8-17 Circuit structure of low-pass Chebyshev filters.

Ripple 0.1dB

TABLE 8-2 Values of Circuit Elements in Chebyshev Filters when $A_{max} = 0.1$ dB (R_L)

n	R_ℓ	C_1	L_2	C_3	L_4	C_5	L_6	C_7	L_8	C_9
1	1.0	0.3052								
2	0.5	1.5715	0.2880							
3	1.0	1.0316	1.1474	1.0316						
4	0.5	2.3545	0.7973	2.6600	0.3626					
5	1.0	1.1468	1.3712	1.9750	1.3712	1.1468				
6	0.5	2.5561	0.8962	3.3962	0.8761	2.8071	0.3785			
7	1.0	1.1812	1.4228	2.0967	1.5734	2.0967	1.4228	1.1812		
8	0.5	2.6324	0.9285	3.5762	0.9619	3.5095	0.8950	2.8547	0.3843	
9	1.0	1.1957	1.4426	2.1346	1.6167	2.2054	1.6167	2.1346	1.4426	1.1957

Ripple 1dB

TABLE 8-3 Values of Circuit Elements in Chebyshev Filters when $A_{max} = 1$ dB (R_L)

n	R_ℓ	C_1	L_2	C_3	L_4	C_5	L_6	C_7	L_8	C_9
1	1.00	1.0177								
2	0.25	3.7779	0.3001							
3	1.00	2.0236	0.9941	2.0236						
4	0.25	4.5699	0.5428	5.3680	0.3406					
5	1.00	2.1349	1.0911	3.0009	1.0911	2.1349				
6	0.25	4.7366	0.5716	6.0240	0.5764	5.5353	0.3486			
7	1.00	2.1666	1.1115	3.0936	1.1735	3.0936	1.1115	2.1666		
8	0.25	4.7966	0.5803	6.1592	0.6005	6.1501	0.5836	5.5869	0.3515	
9	1.00	2.1797	1.1192	3.1214	1.1897	3.1746	1.1897	3.1214	1.1192	2.1797

Bessel Filter

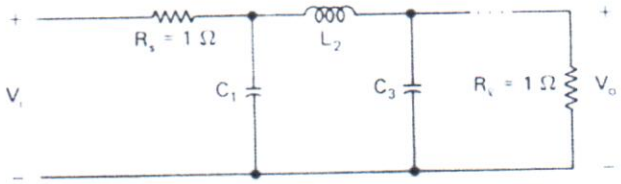


Fig. 8-23 A basic circuit structure for low-pass Bessel filters.

Filter order

TABLE 8-4 Values of Circuit Elements in Bessel Filters

n	C_1	L_2	C_3	L_4	C_5	L_6	C_7	L_8	C_9
1	2.0000								
2	1.5774	0.4226							
3	1.2550	0.5528	0.1922						
4	1.0598	0.5116	0.3181	0.1104					
5	0.9303	0.4577	0.3312	0.2090	0.0718				
6	0.8377	0.4116	0.3158	0.2364	0.1480	0.0505			
7	0.7677	0.3744	0.2944	0.2378	0.1778	0.1104	0.0375		
8	0.7125	0.3446	0.2735	0.2297	0.1867	0.1387	0.0855	0.0289	
9	0.6678	0.3203	0.2547	0.2184	0.1859	0.1506	0.1111	0.0682	0.0230

FILTER TRANSFORMATIONS

TABLE 8-5 Frequency and Element Transformations

From Normalized Low-pass Filter to:	Frequency Transformations	$R\ \Omega$	L H.	C F.
A low-pass filter with cutoff frequency ω_c	$s \longrightarrow \frac{s}{\omega_c}$	$R\ \Omega$	$\frac{L}{\omega_c}$ H.	$\frac{C}{\omega_c}$ F.
A bandpass filter with center frequency ω_0 and bandwith B	$s \longrightarrow \frac{s^2 + \omega_0^2}{Bs}$	$R\ \Omega$	$\frac{L}{B}$ H $\frac{B}{\omega_0^2 L}$ F.	$\frac{C}{B}$ F. $\frac{B}{\omega_0^2 C}$
A band-reject filter with center frequency ω_0 and rejection bandwidth B	$s \longrightarrow \frac{Bs}{s^2 + \omega_0^2}$	$R\ \Omega$	$\frac{1}{BL}$ F. $\frac{BL}{\omega_0^2}$ H.	$\frac{1}{BC}$ H. $\frac{BC}{\omega_0^2}$ F.
A high-pass filter with cutoff frequency ω_c	$s \longrightarrow \frac{\omega_c}{s}$	$R\ \Omega$	$\frac{1}{L\omega_c}$ F.	$\frac{1}{C\omega_c}$ H.
Impedance scaling by A	No change	$AR\ \Omega$	AL H.	$\frac{C}{A}$ F.

Selected Plots from

ANALOG AND DIGITAL FILTERS: DESIGN AND REALIZATION -- Harry Y-F. LAM

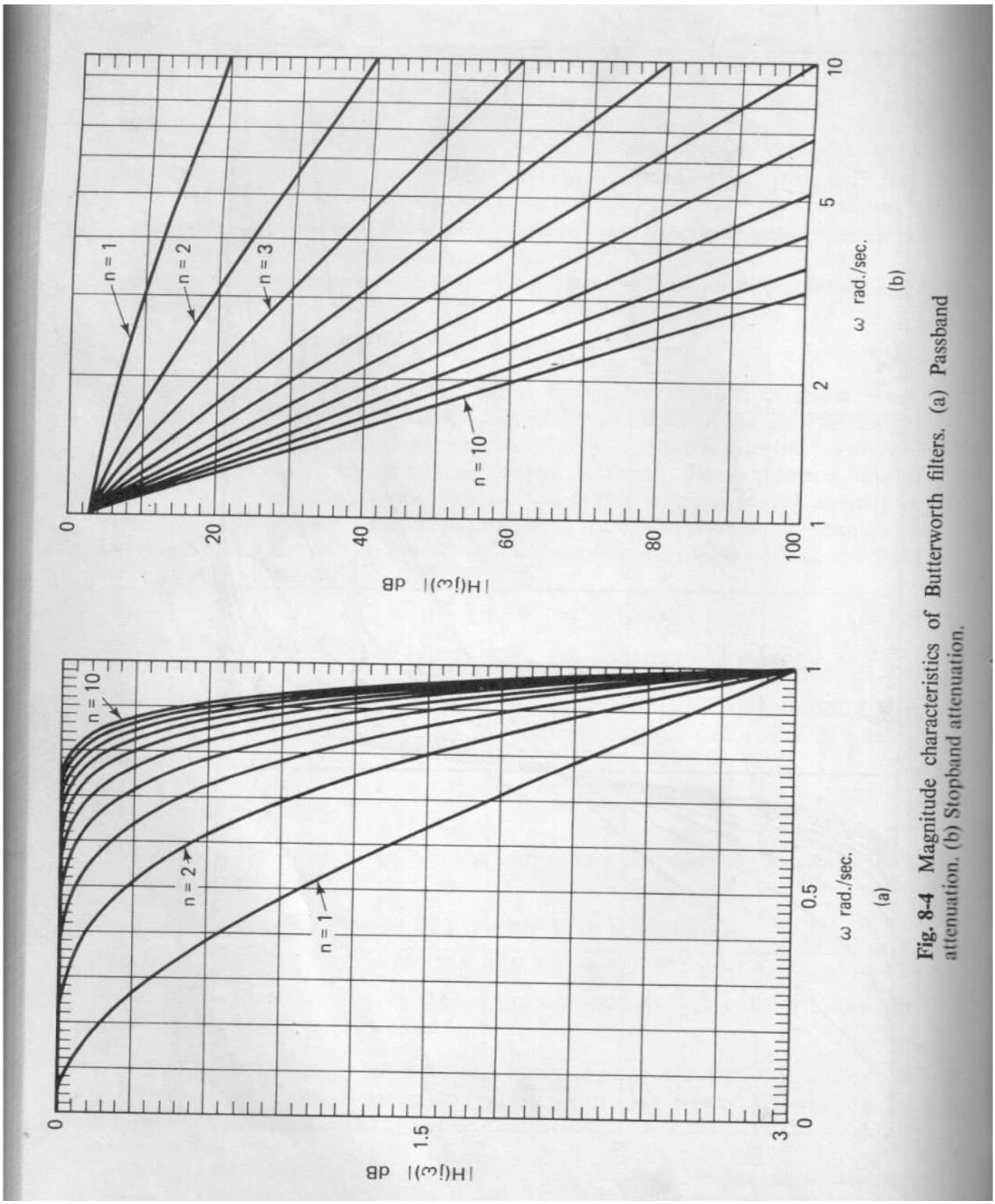


Fig. 8-4 Magnitude characteristics of Butterworth filters. (a) Passband attenuation. (b) Stopband attenuation.

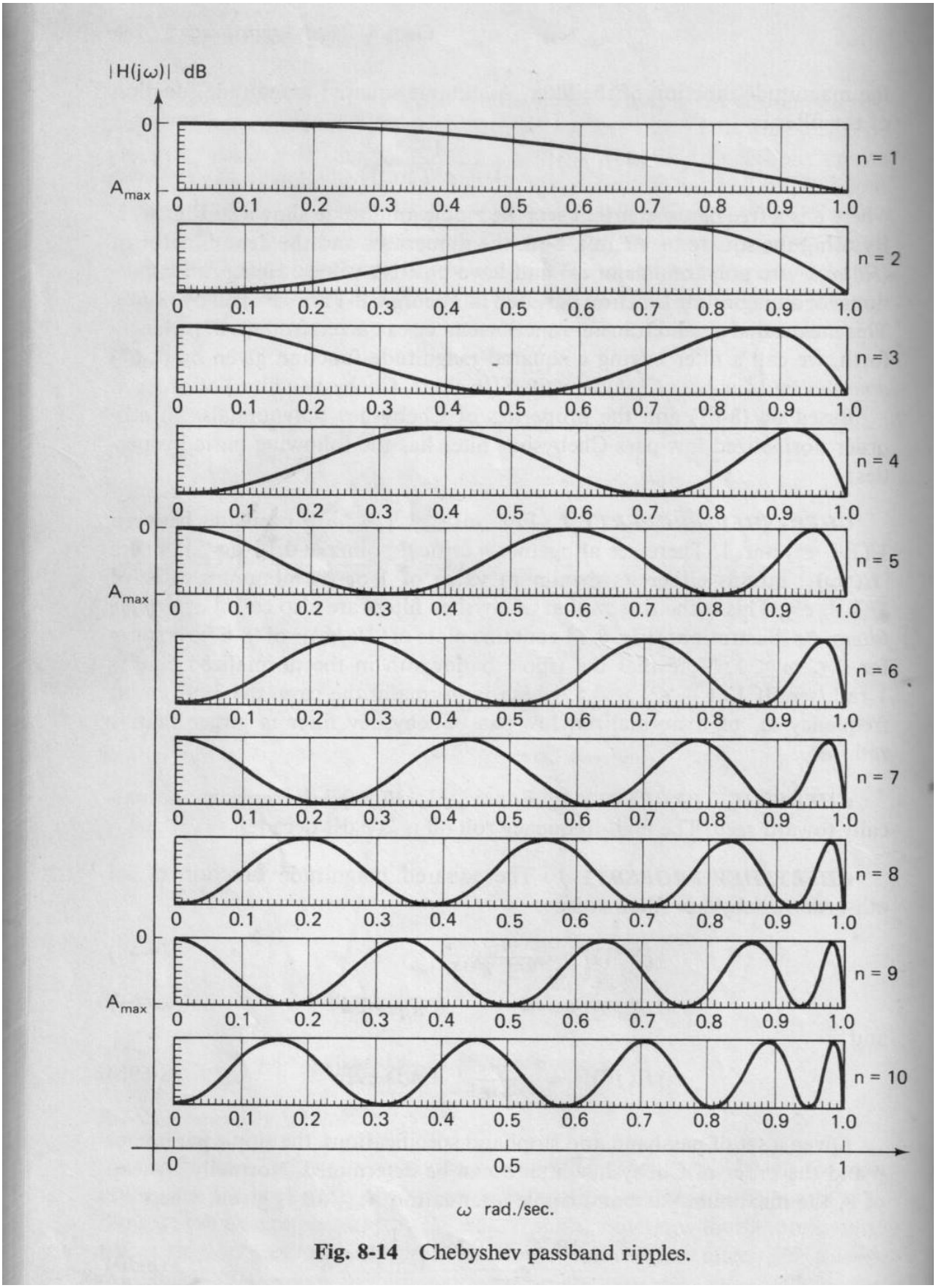


Fig. 8-14 Chebyshev passband ripples.

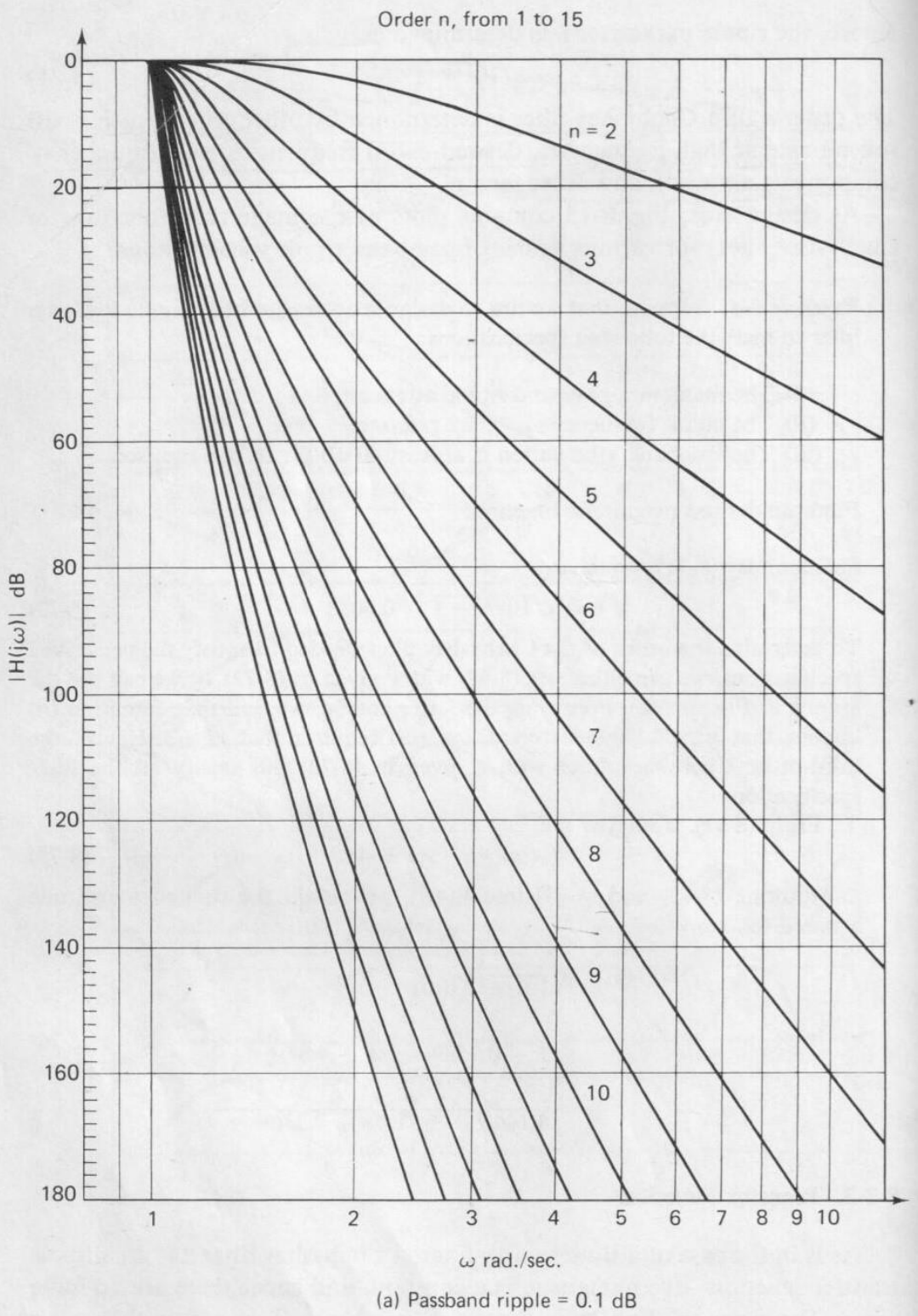
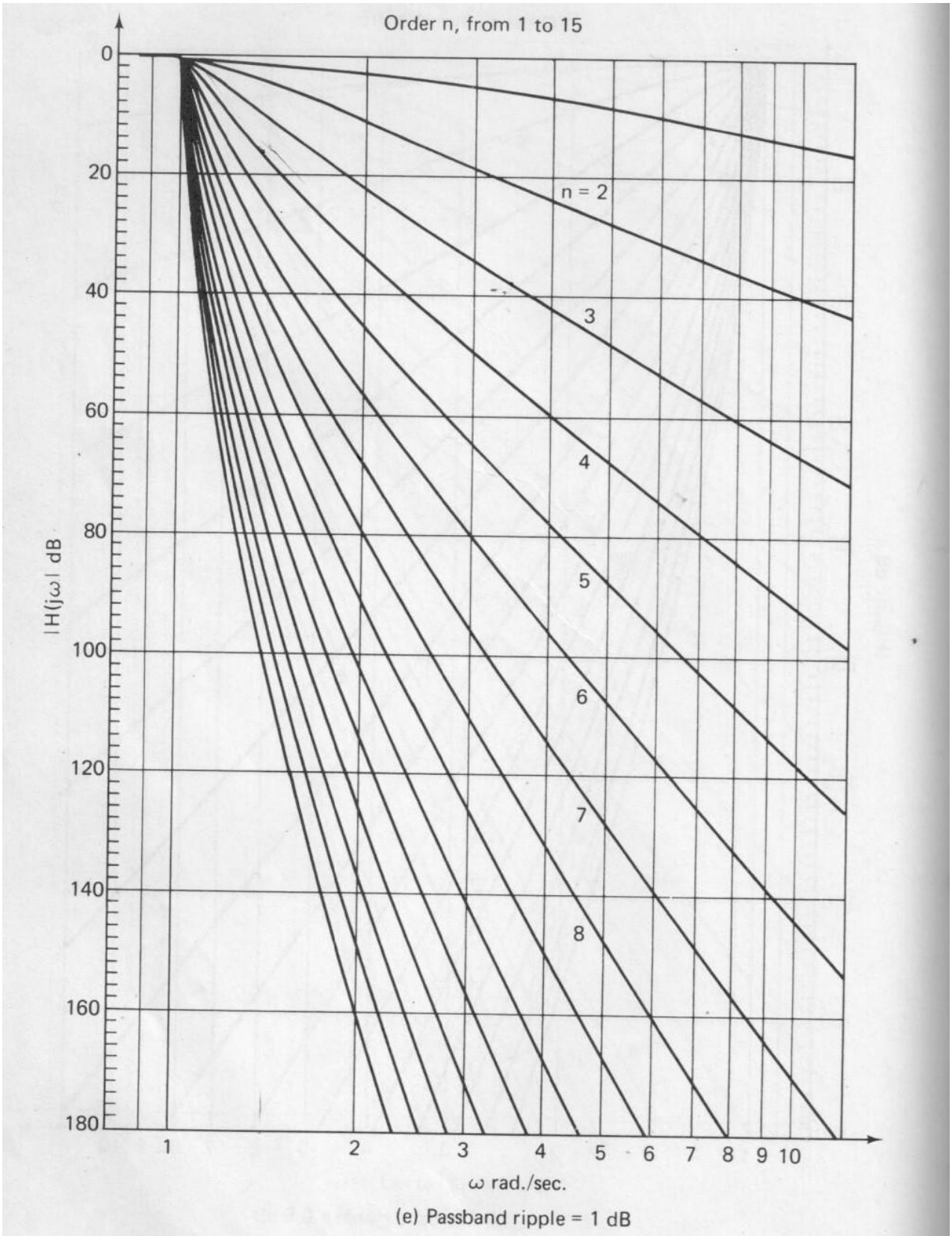


Fig. 8-15 Attenuation characteristics of Chebyshev filters.



(e) Passband ripple = 1 dB

Fig. 8-15 (continued)

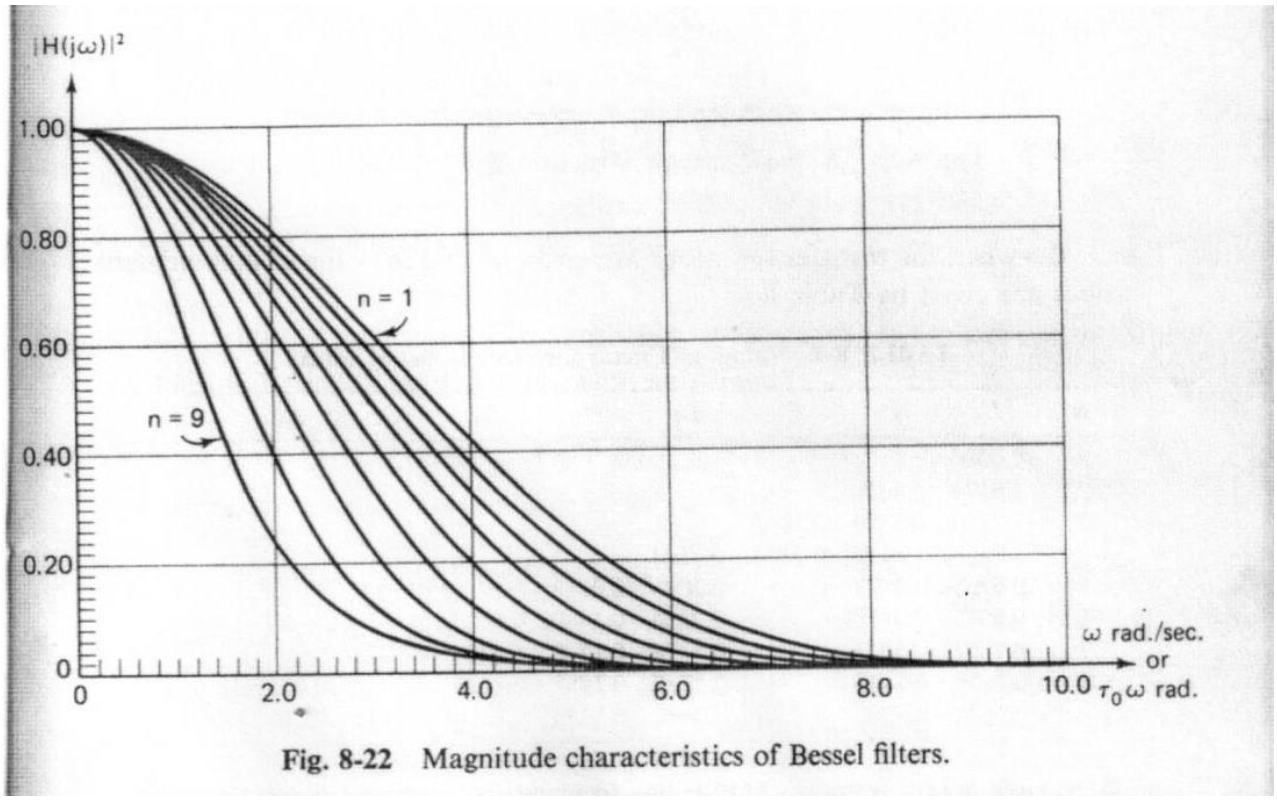


Fig. 8-22 Magnitude characteristics of Bessel filters.

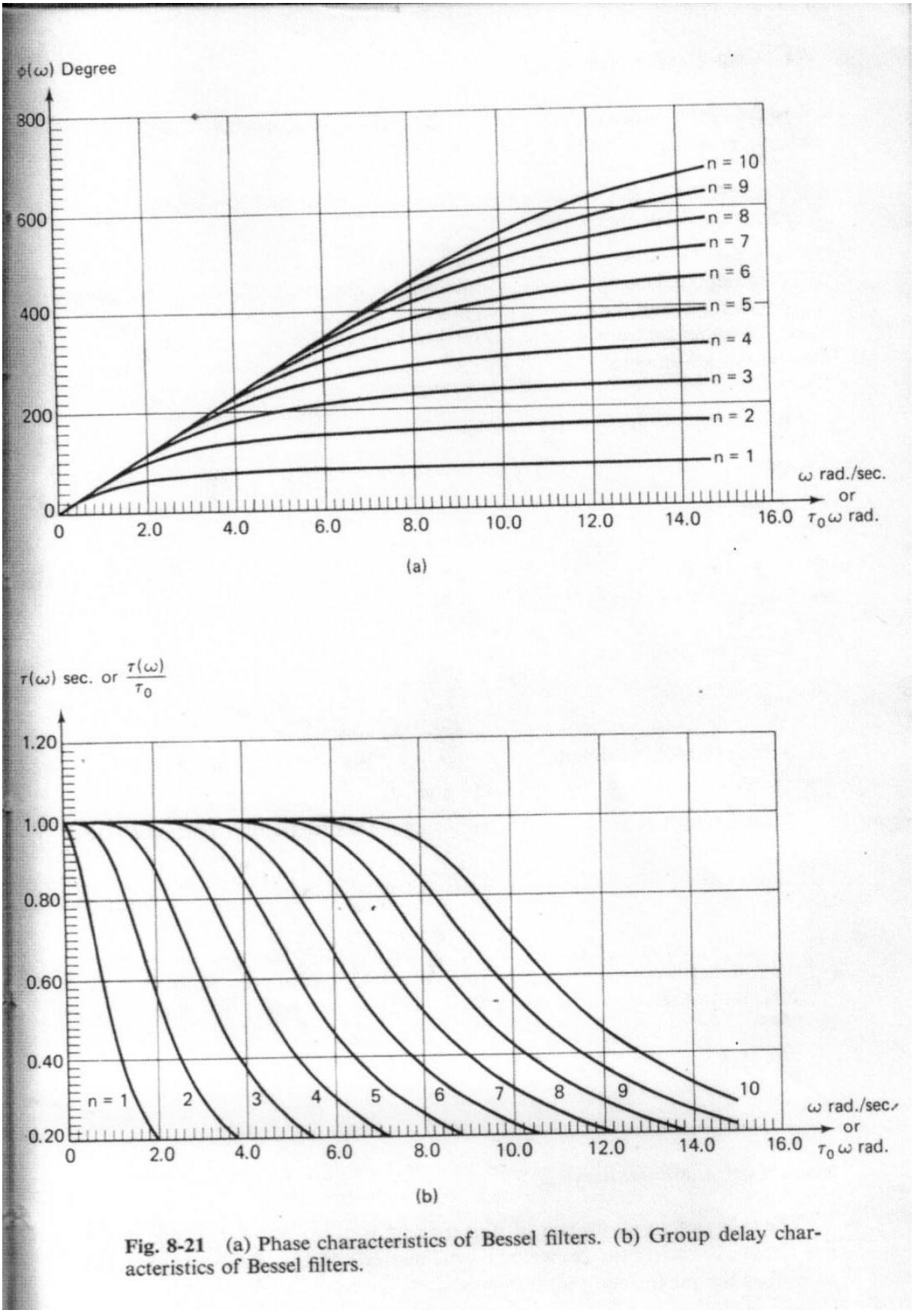
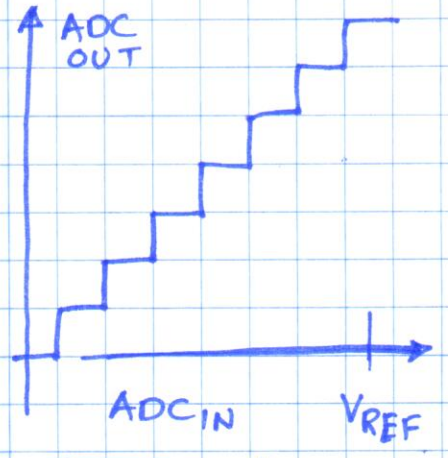
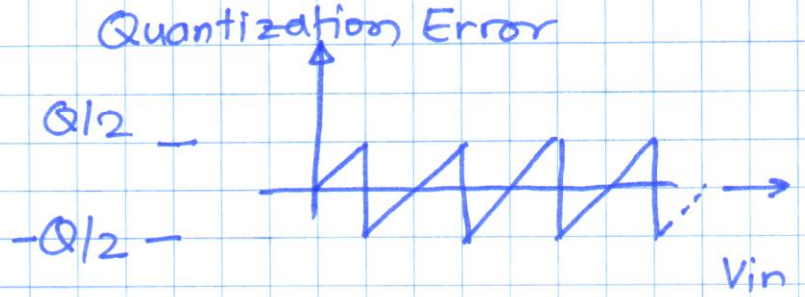


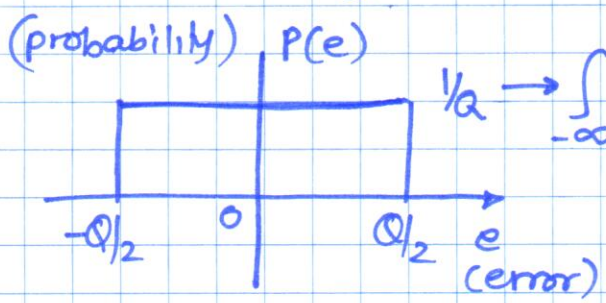
Fig. 8-21 (a) Phase characteristics of Bessel filters. (b) Group delay characteristics of Bessel filters.

SNR - QUANTIZATION NOISE DERIVATION.



$\Rightarrow$

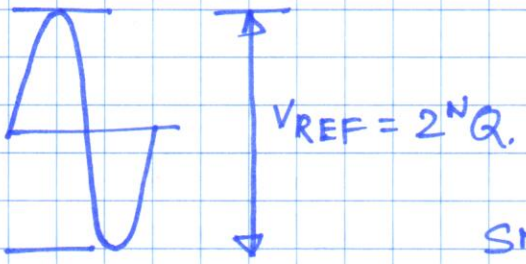




$$\int_{-\infty}^{\infty} P(e)\,de = 1$$

σ^2 = Quantization Noise power = $\int_{-Q/2}^{Q/2} e^2 \cdot P(e)\,de$

$$= \frac{1}{Q}\int_{-Q/2}^{Q/2} e^2 de = \frac{1}{Q}\left[\frac{e^3}{3}\right]_{-Q/2}^{Q/2} = \frac{Q^2}{12} = \overline{V_n}^2_{rms}$$



$$V_{sig_{rms}} = \frac{2^N Q}{\sqrt{2}\cdot 2}$$

$$SNR = 20\log\left(\frac{V_{sig\,rms}}{V_{n\,rms}}\right)$$

$$= 20\log\left(\frac{2^N Q}{2\sqrt{2}} \cdot \frac{\sqrt{12}}{Q}\right)$$

$$SNR = 20\log 2^N + 20\log\left(\sqrt{\frac{3}{2}}\right) = 6.02N + 1.76$$

Filter Approximations

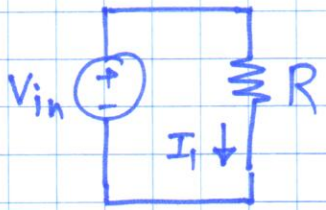
	Butterw	Chebyshev	Elliptic Cauer	Bessel
Passband	✡ ✡ ✡	✡ ✡ ✡ ✡	✡ ✡ ✡ ✡	✡ ✡
Stopband Atten	✡ ✡ ✡	✡ ✡ ✡ ✡	✡ ✡ ✡ ✡ ✡	✡ ✡
Group Delay	✡ ✡ ✡	✡ ✡	✡	✡ ✡ ✡ ✡ ✡

Filter Design Process

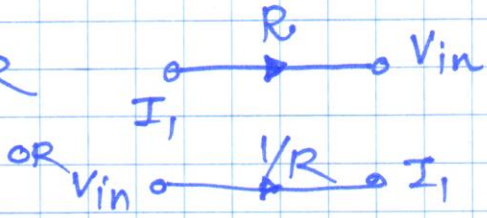
1. Choose Filter Approx based on desired filter characteristics
2. For Normalized $f_{stopband}$, use filter curves to determine order of filter.
3. Use filter tables to find out component values.

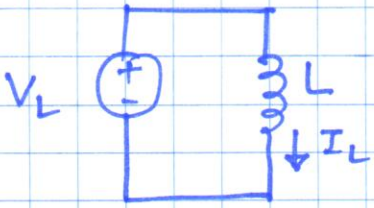
Signal flow Graph Technique SFG

Basics

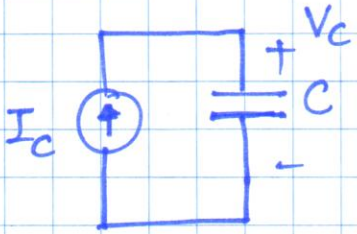


$V_{in} = I_1 R$

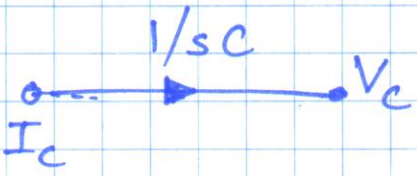


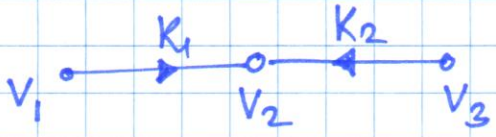


$I_L = \frac{V_L}{sL}$

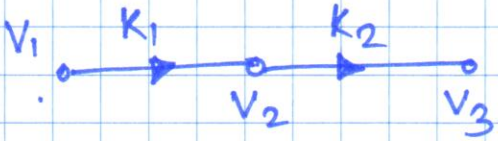


$V_C = \frac{1}{sC} I_C$





$\Rightarrow V_2 = K_1 V_1 + K_2 V_3$



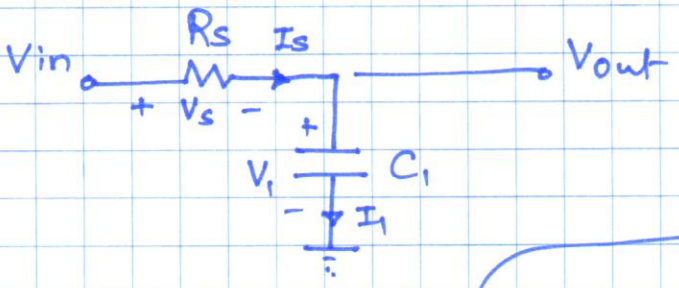
$\Rightarrow V_3 = K_1 K_2 V_1$

$\Rightarrow V_3 = \frac{K_1}{K} \cdot K K_2 V_1$

$= K_1 K_2 V_1$ equivalent

Signal Flow Graph Technique simulates voltage-current relationship in passive network.

Example : One pole RC Lowpass filter



Equations for this ckt-

$V_s = (V_{in} - V_1)$

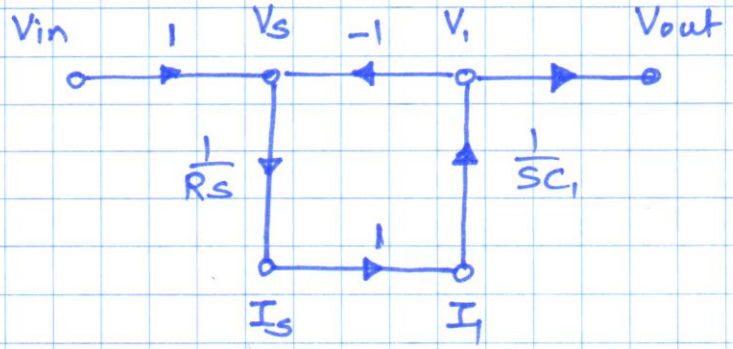
$V_{out} = V_1$

$V_1 = \frac{1}{sC_1} I_1$ (Integrator)

$I_s = I_1$

$I_s = \frac{V_s}{R_s}$

Modeling in SFG Technique



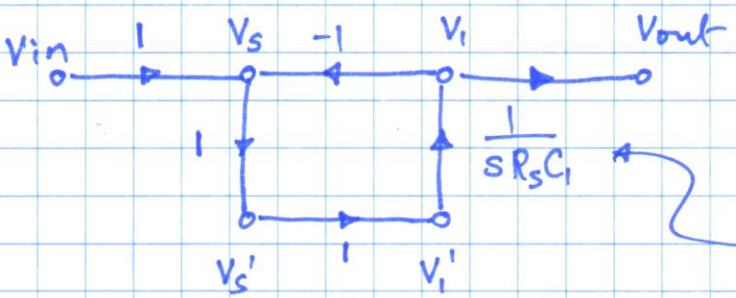
* More $\frac{1}{R_s}$ around loop

* scaling resistance R

$V_s' = R I_s$

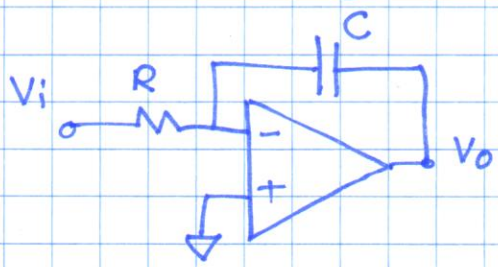
$V_1' = R I_1$

Choosing R = 1 (convenience)

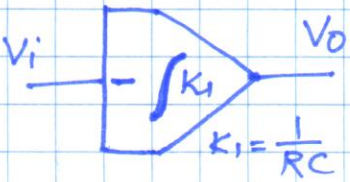


Integrator

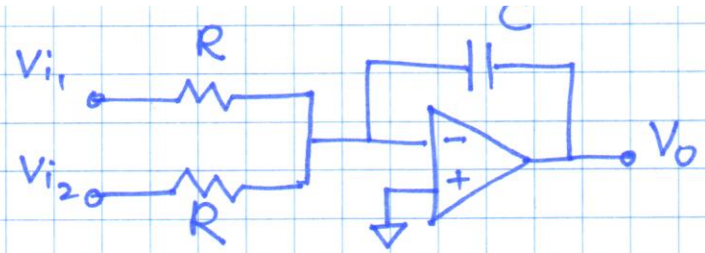
Implementing Integrator

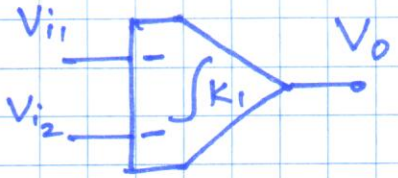


$\frac{V_i}{R} = \frac{-V_o}{1/sC} \Rightarrow V_o = -\frac{V_i}{sRC}$

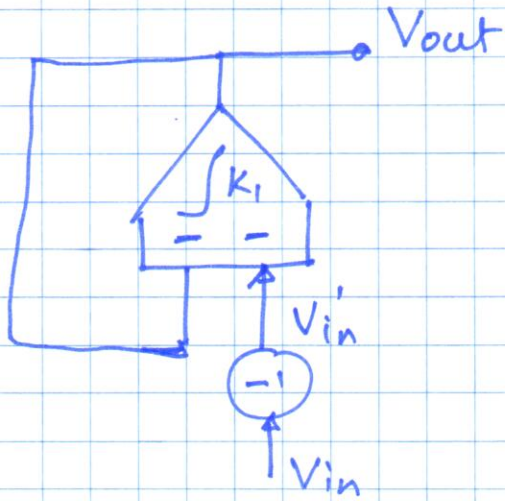


Note: i/p & o/p both voltages.

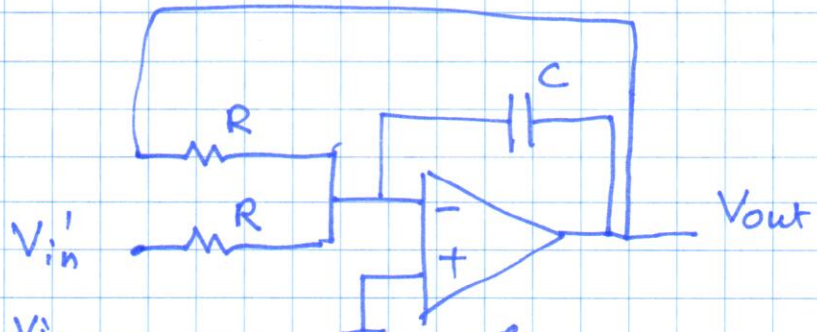




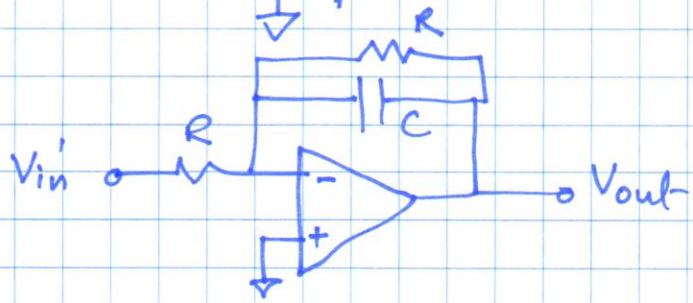
Pushing this in SFG



$$K_1 = \frac{1}{R_s C_1}$$



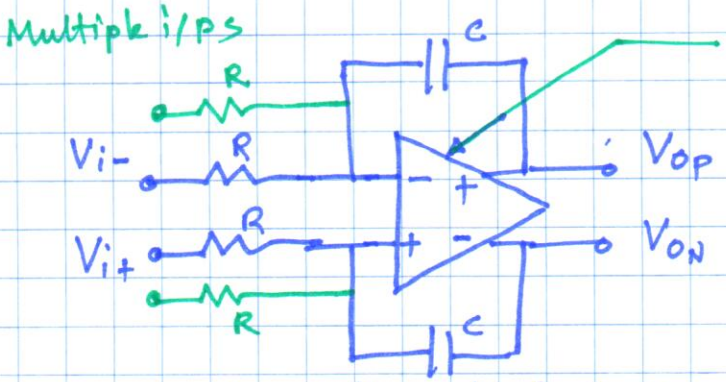
$= -V_{in}$



$$\frac{V_{out}}{V_{in}'} = \frac{-1}{1+RCs}$$

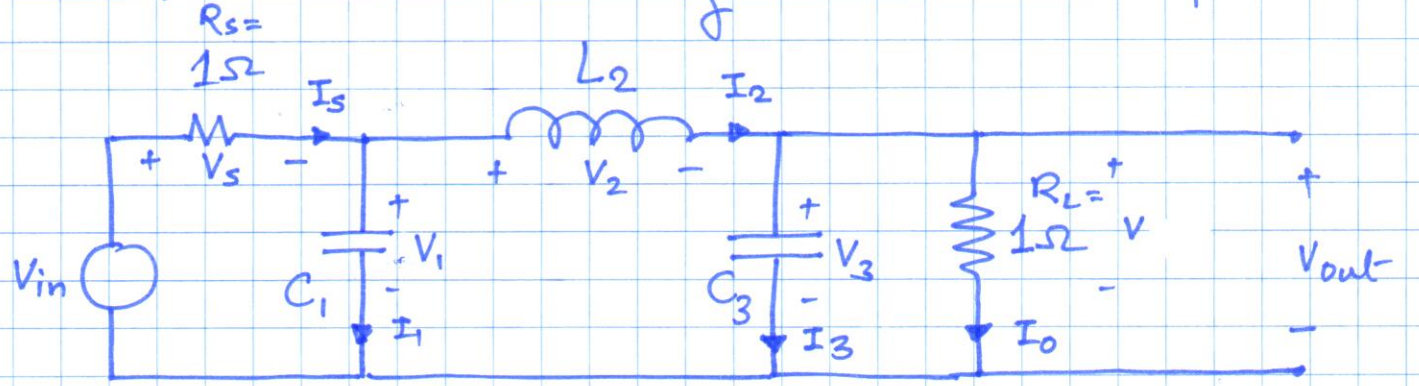
NOTES

* Active RC (or OPAMP RC) integrator has inverting i/p only.
* Other integrators we will study have both +/- i/p.
* Active RC integrator can be used in fully differential configuration with both + & -ve i/p.
  - will study fully differential circuits later.



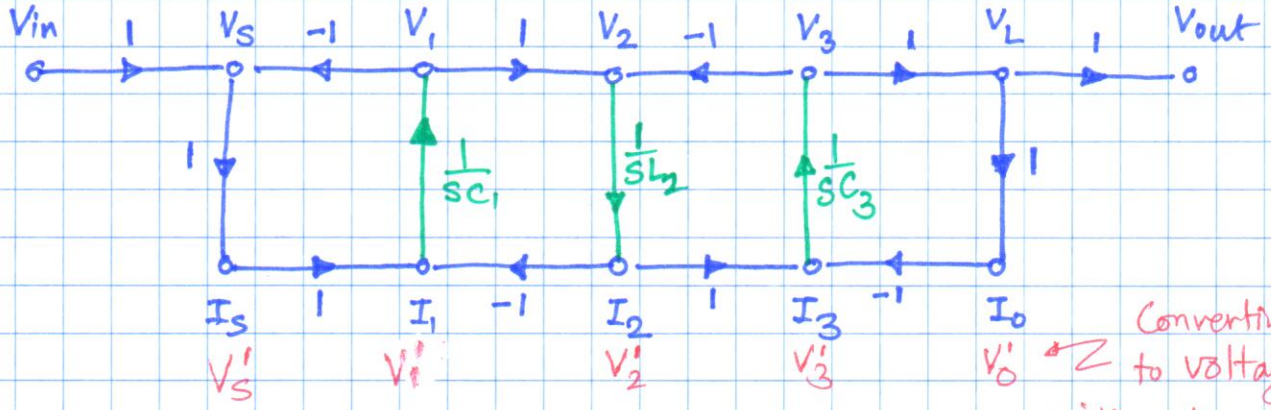
Fully differential Active RC integrator

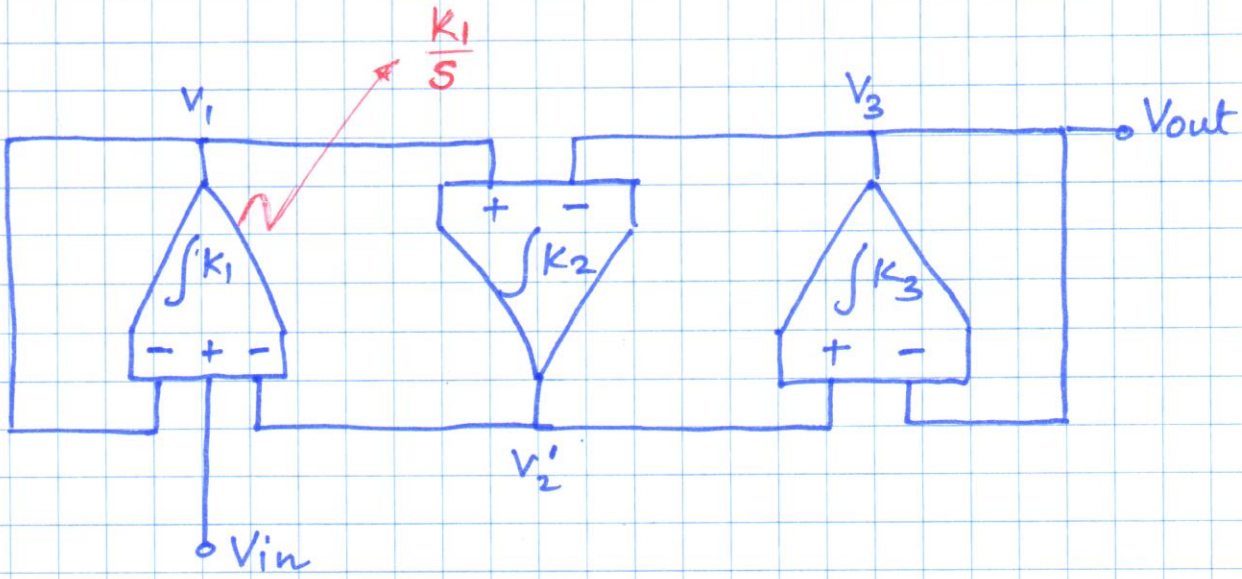
Example 2. Implementing Third Order Chebyshev filter



SFG. Steps

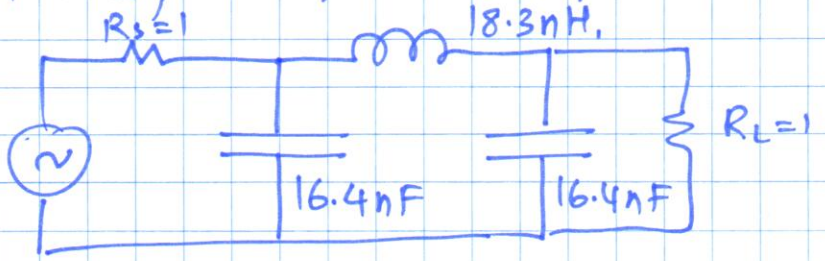
1. Lable all branch currents & voltages.
2. Draw voltage as "node" on top & current as "node" on bottom.
3. Represent Integrator relationships first
4. Complete SFG with Rest of KVL & KCL equations.





$$K_1 = \frac{1}{C_1} \qquad K_2 = \frac{1}{L_2} \qquad K_3 = \frac{1}{C_3}$$

For Chebyshev filter example



Implementing each integrator with fully diff. active RC integrator.

$$K_3 = K_1 = \frac{1}{16.4n} = \frac{1}{R_1 C_1} \Rightarrow$$

Choosing $C_1 = 1pF$, $R_1 = 16.4K\Omega$

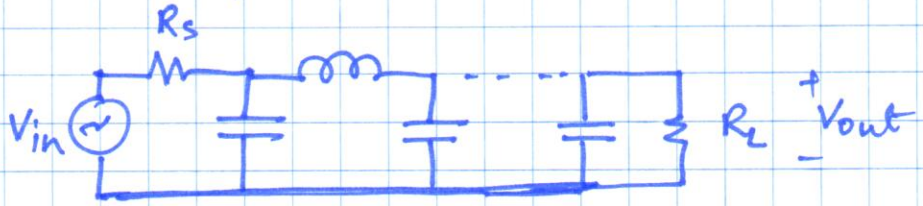
$$K_2 = \frac{1}{18.3n} = \frac{1}{R_2 C_2} \Rightarrow$$

Choosing $C_2 = 1pF$, $R_2 = 18.3K\Omega$

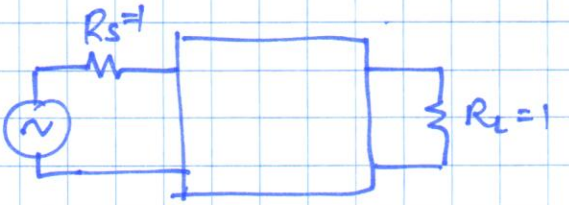
Values compact realizable on chip.

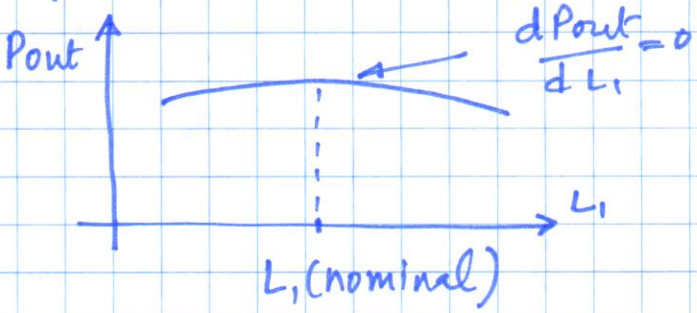
Few comments on filter implementation.

1. Doubly-Terminated Ladder filter



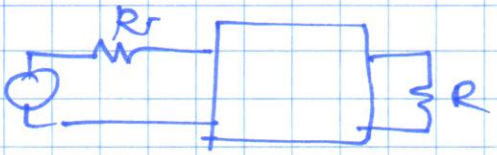
Low sensitivity due to component variation.





→ Component variation insensitivity in passband.

2. Attenuation of 6dB due to double-termination



→ Can be corrected by adding gain @ i/p.

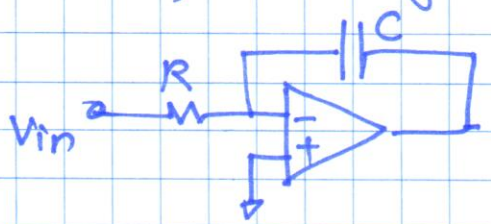
Next Lecture:

→ Various ways of implementing Integrators.

→ Trade-offs.

* Key Element in filter design (ladder) → Integrator

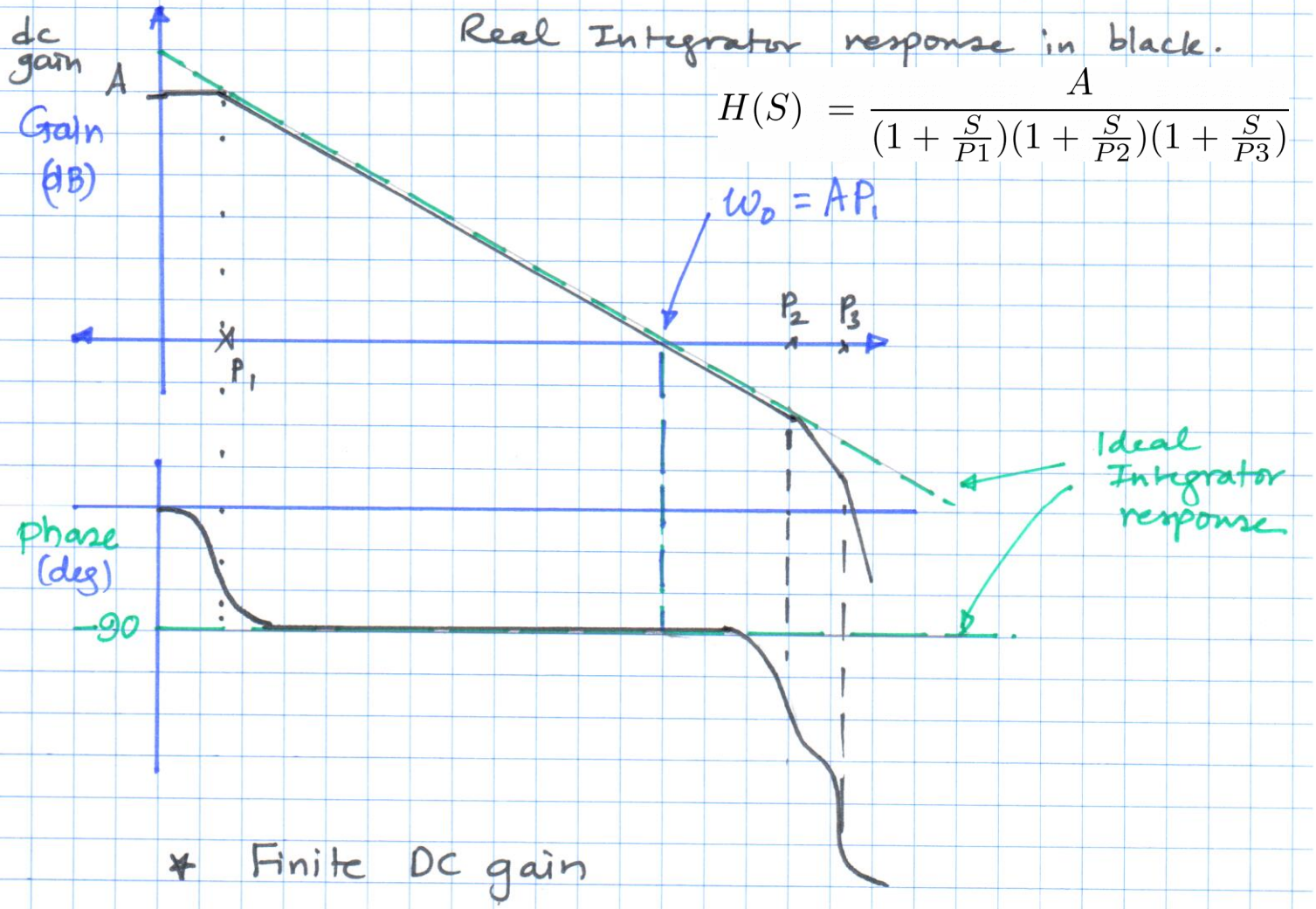
Example



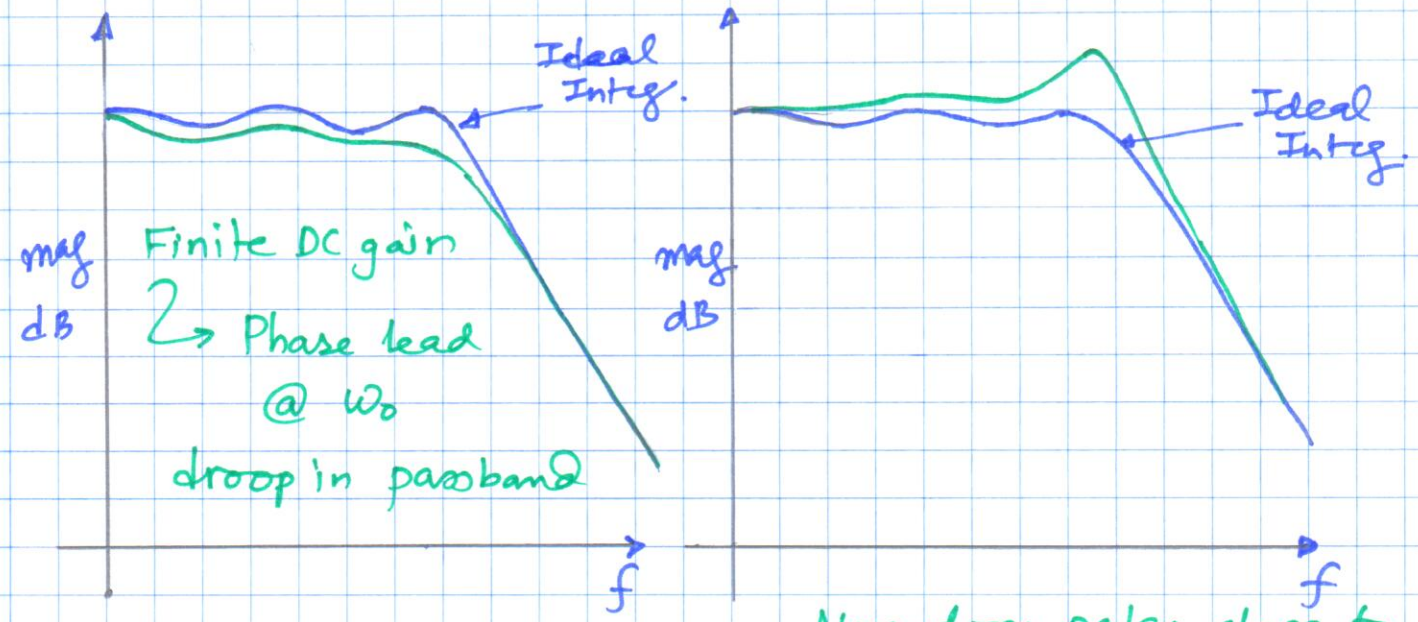
Ideal Integrator Response shown in green. $H(S) = \frac{\omega_0}{S}$

Real Integrator response in black.

$$H(S) = \frac{A}{(1+\frac{S}{P1})(1+\frac{S}{P2})(1+\frac{S}{P3})}$$



* Finite DC gain
* Phase shift @ unity gain frequency due to Non-dominant poles P_2, P_3 etc.



Non-dom poles close to integrator UG.F ω_o.
→ phase lag @ ω_o
→ peaking - could be oscillatory. → careful.

Integrator Quality factor

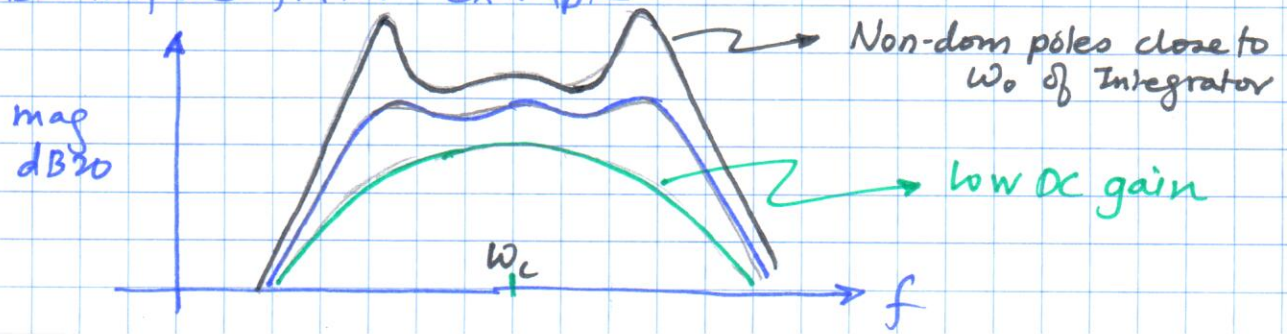
$$\text{Ideal integrator} = \frac{K}{s} = \frac{1}{j\omega RC}$$

$$\text{Non Ideal Integrator} = \frac{1}{(\text{Real}) + j(\text{Imag})}$$

$$Q_{\text{integrator}}(\omega) = \frac{\text{Imaginary}}{\text{Real}}$$

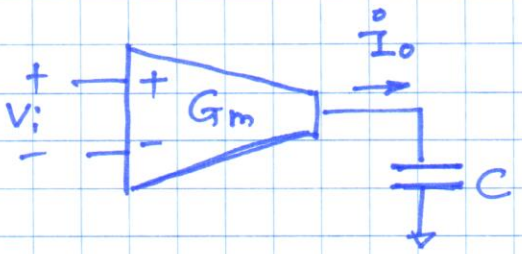
Real → 0 ⇒ $Q = \infty$ @ ω_o

Bandpass filter example



Gm-C Filters

Gm – transconductance

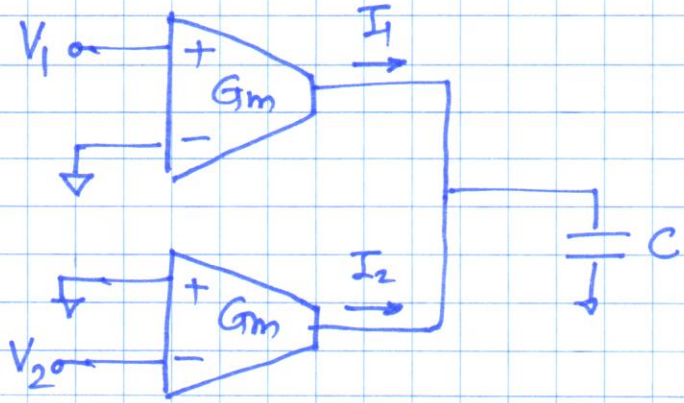


$$i_o = G_m V_i$$

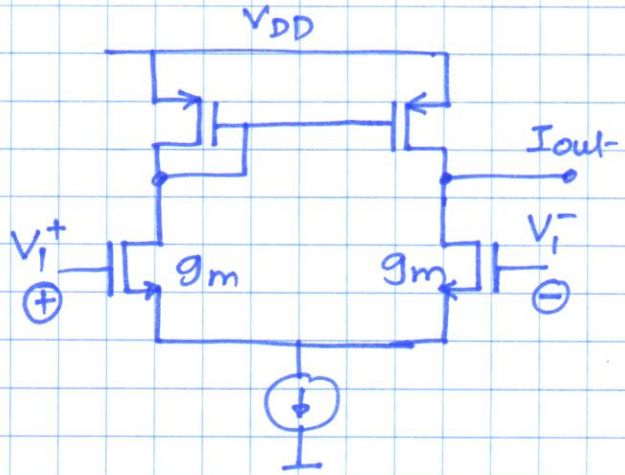
$$V_o = \frac{i_o}{sC} = \frac{G_m V_i}{sC}$$

$$\frac{V_o}{V_i} = \frac{\omega_o}{\omega} \rightarrow \left(\frac{G_m}{C}\right)$$

Multi input integrator / summer



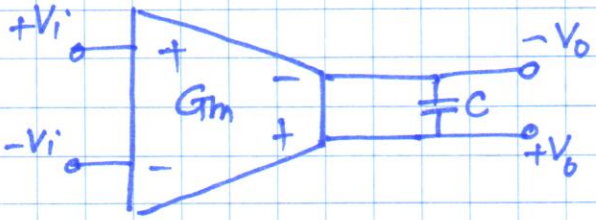
$$V_o = \frac{G_m}{sC}\left(V_1 - V_2\right)$$

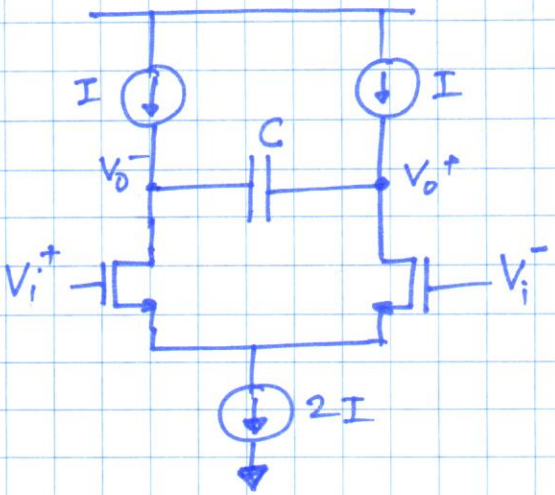


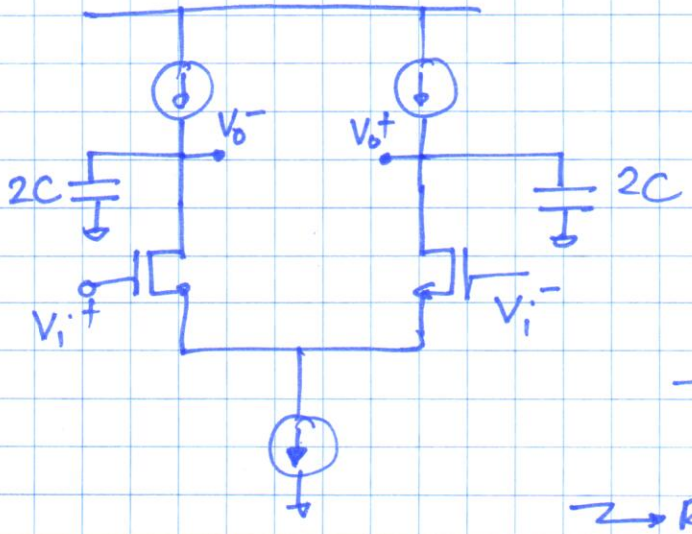
Gm-C filters

+ Simple circuit
+ Lends to high frequency performance
– Linearity.
  → can be improved by source degeneration
– Tuning Required due to Gm variations.

Fully-Differential Gm-C integrator





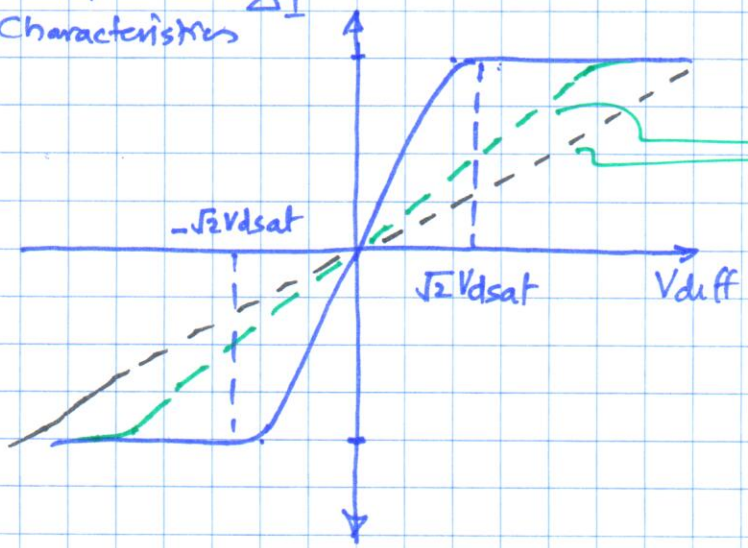


Better since common-mode path also has capacitors.

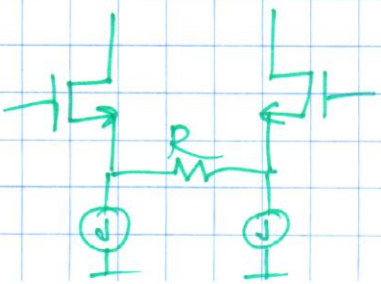
→ Although larger size.

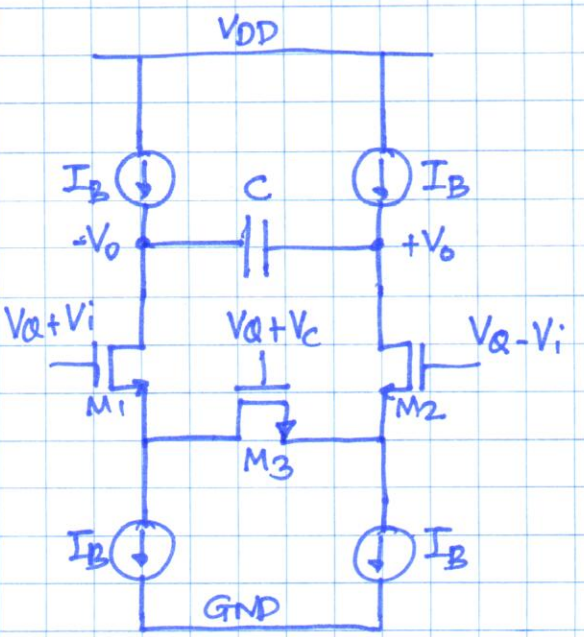
→ Reference H. Khorramabadi "High Freq. CMOS filters" JSSC DEC 84.

Gm Characteristics



Source degeneration to improve linearity of Gm cell.



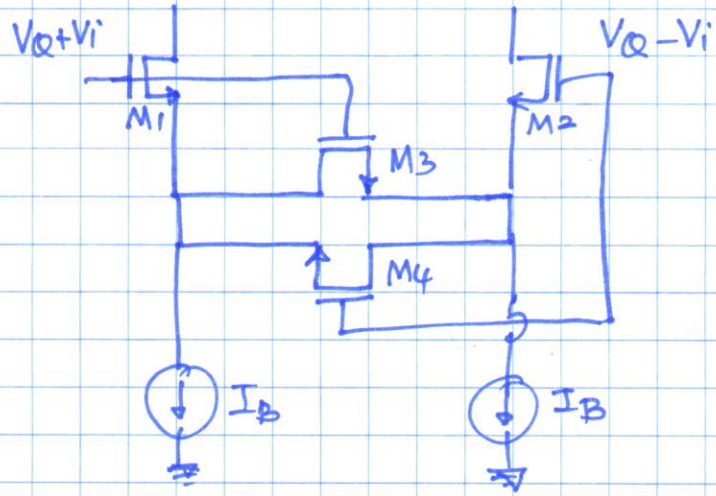


source degeneration using MOS Transistor M3 in Triode region

V_c – used for tuning G_m & filter corner frequency

2 → J. M. Khoury JSSC Dec. 91

Another variation



M3, M4 in triode region

They are biased from i/p signal.

Better distortion performance.

$$G_m = \frac{4 K_1 K_3}{(K_1 + 4K_3)} \sqrt{\frac{2 I_B}{K_1 \mu_n C_{ox}}}$$

$$K_1 = \left(\frac{W}{L}\right)_1 \quad K_3 = \left(\frac{W}{L}\right)_3$$

2 → Reference F. KRUMMENACHER.

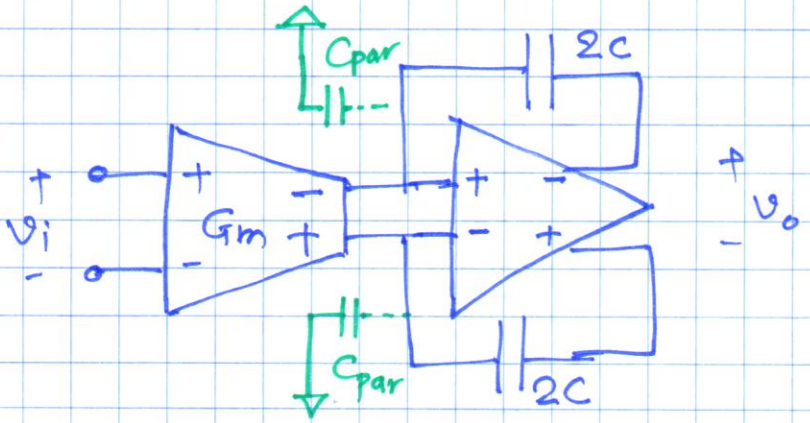
A 4MHz CMOS. Cont. time filter with on-chip Automatic tuning. JSSC – JUNE 1988.

Key issue in design of High Frequency Gm-C filter

* Parasitic caps. (top plate parasitics, interconnect caps, Next stage loading)
  - → appear in parallel with integration cap. affecting frequency response accuracy.
  - → can't be compensated & matched.

Goal – Parasitic Insensitive topology.

* Gm-C OPAMP Filters



* Parasitic caps @ o/p of Gm – connected to virtual gnd.
* Gm o/p doesn't handle large swings
* Higher Integrator gain
* wideband OTA can be used instead of OPAMP.

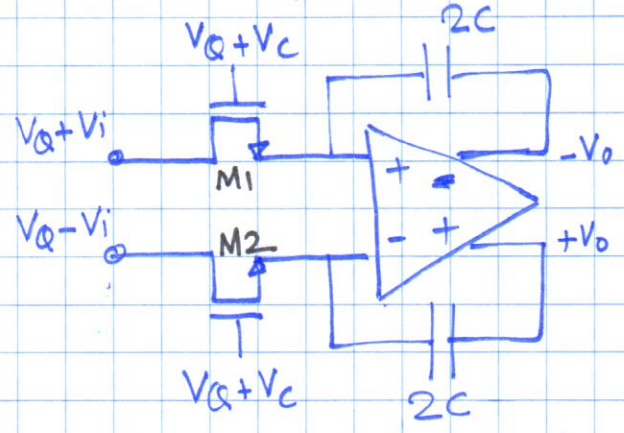
Ref: 1. K.S.TAN & P.GRAY JSSC DEC 78

2. C. Laber & P. GRAY JSSC April 93

- Overall higher power

MOSFET-C Filters

→ Replace Gm transconductor with MOS in triode region.
→ Lower power.



M1 & M2 in triode region.

$\omega_o = \frac{1}{RC}$ UGF of Integrator.

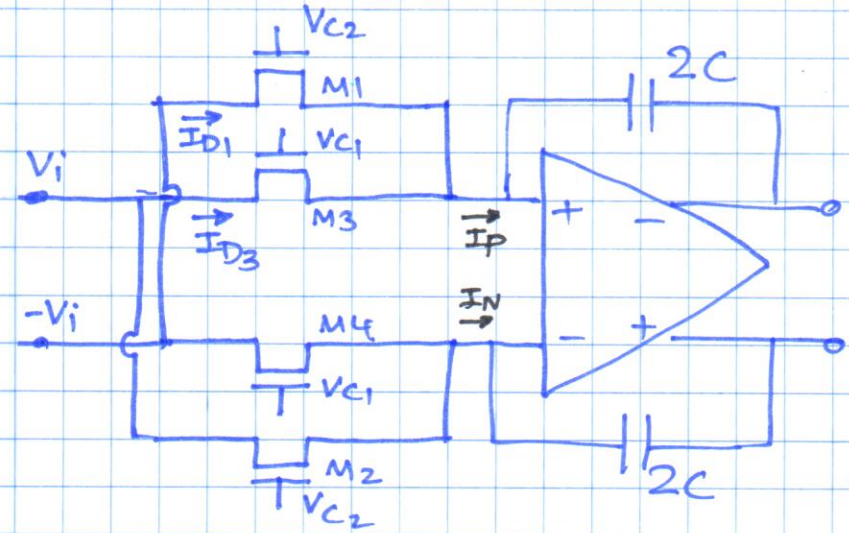
$$R = \frac{1}{\mu C_{ox}\left(\frac{W}{L}\right)(V_C - V_T)}$$

* Fully-balanced operation - MOS even-order non-linearities are cancelled.
* Third order (odd) non-linearities - keep signal amplitude low

Ref: Fully Integrated Active RC filters in MOS tech"
M. Banu, Y. Tsividis - JSSC Dec 1983.

Improving linearity further

TRIODE EQ. $I_D = K\left(V_{gs} - V_T - \frac{V_{ds}}{2}\right)V_{ds}$ $\quad K = \mu_n C_{ox}\left(\frac{W}{L}\right)$



$$I_{D1} = K\left(V_{gs1} - V_T + \frac{V_i}{2}\right)V_i$$

$$I_{D3} = K\left(V_{gs3} - V_T - \frac{V_i}{2}\right)V_i$$

$$I_P = I_{D1} + I_{D3} = KV_i\left(V_{gs3} - V_{gs1} - V_i\right)$$

$$I_N = KV_i\left(V_{gs1} - V_{gs3} - V_i\right)$$

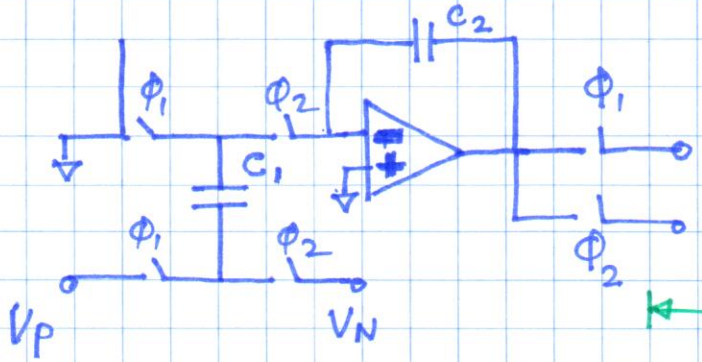
$$I_P - I_N = 2KV_i\left(V_{gs3} - V_{gs1}\right)$$

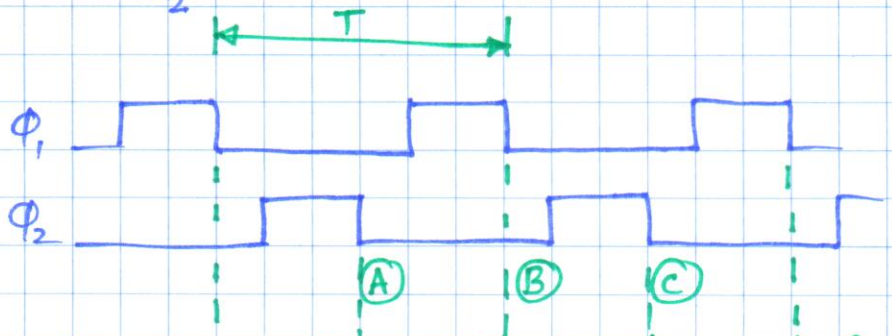
$$G_{meff} = \frac{\partial(I_P - I_n)}{\partial(2V_i)} = \mu_n C_{ox}\left(\frac{W}{L}\right)\underbrace{(V_{C1} - V_{C2})}_{\text{Const}}$$

Ref: Z. Czarnul IEEE. Tran CAS JULY 1986.
M. Ismail JSSC Feb 88.

Large Signal Linear behavior
→ : 50-70dB linearity.

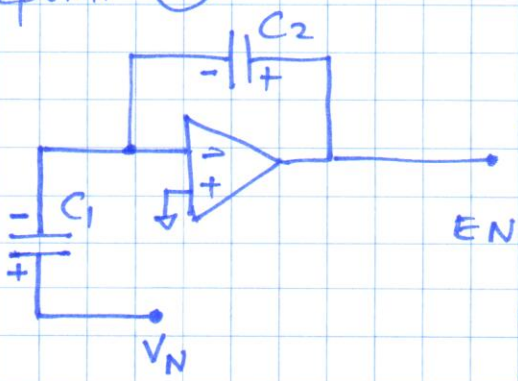
Parasitic Insensitive Switched-Capacitor Integrator





Lets figure out $V_{out_2}(t)$ first.

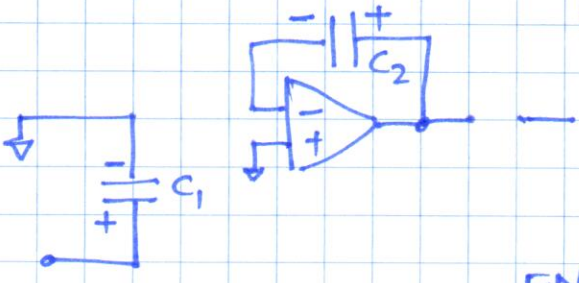
@ Timepoint (A)



END OF Φ_2

$$Q_{C_1-} = -C_1 V_N(t-T)$$
$$Q_{C_2-} = -C_2 V_{out_2}(t-T)$$

@ Timepoint (B)



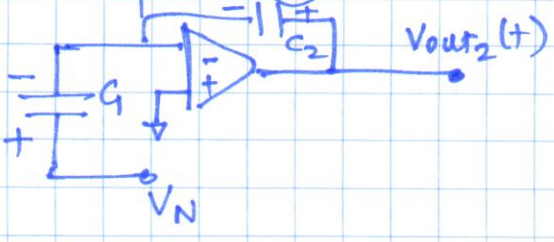
END OF Φ_1

$$Q_{C_1-} = -C_1 V_P(t-\tfrac{T}{2})$$
$$Q_{C_2-} = -C_2 V_{out_2}(t-T)$$

END OF Φ_2 - charge redistribution

$$Q_{C_1-} = -C_1 V_N(t)$$
$$Q_{C_2-} = -C_2 V_{out_2}(t)$$

@ Timepoint (C)



From (B) to (C) – charge conserved on capacitor plates connected to OPAMP. -ve i/p

$$\underbrace{Q_{C_1-} + Q_{C_2-}}_{(B)} = \underbrace{Q_{C_1-} + Q_{C_2-}}_{(C)}$$

$$-C_1 V_p\left(t-\tfrac{I}{2}\right) - C_2 V_{out_2}(t-T) = -C_1 V_N(t) - C_2 V_{out_2}(t)$$

Div by $-C_2$

$$\frac{C_1}{C_2} V_p\left(t-\tfrac{I}{2}\right) + V_{out_2}(t-T) = \frac{C_1}{C_2} V_N(t) + V_{out_2}(t)$$

Z - X form

$$\frac{C_1}{C_2} z^{-1/2} V_p(z) + z^{-1} V_{out_2}(z) = \frac{C_1}{C_2} V_N(z) + V_{out_2}(z)$$

$$V_{out_2}(z) = \underbrace{\frac{\left(\frac{C_1}{C_2}\right) z^{-1/2}}{1-z^{-1}} V_p(z)}_{\text{(Half Delay)}} - \underbrace{\frac{\left(\frac{C_1}{C_2}\right)}{1-z^{-1}} V_N(z)}_{\text{(Zero Delay)}}$$

$$V_{out_1}(z) = z^{-1/2} V_{out_2}(z)$$

$$V_{out_1}(z) = \underbrace{\frac{\left(\frac{C_1}{C_2}\right) z^{-1}}{1-z^{-1}} V_p(z)}_{\text{(Unit Delay)}} - \underbrace{\frac{\left(\frac{C_1}{C_2}\right) z^{-1/2}}{1-z^{-1}} V_N(z)}_{\text{(Half Delay)}}$$

$\left(\frac{C_1}{C_2}\right)$ → Integrator constant

$\frac{1}{1-z^{-1}}$ → Integrator function

{ Both (+ve) & (-ve) i/ps. achieved

Recap Integrator XF $H(s) = -\frac{1}{sCR} = -\frac{\omega_0}{s}$

$|H(j\omega)| = \omega_0/\omega \qquad \angle H(j\omega) = 90°$

Lets compare with discrete-time integrators.

$z = e^{j\omega T}$

Zero delay Integrator

$$\frac{\left(\frac{C_1}{C_2}\right)}{1 - z^{-1}} = \frac{\left(\frac{C_1}{C_2}\right)}{1 - e^{-j\omega T}} \left(\cdot \frac{e^{j\omega T/2}}{e^{j\omega T/2}} \right)$$

$$\frac{\left(\frac{C_1}{C_2}\right)}{1 - z^{-1}} = \frac{\left(\frac{C_1}{C_2}\right) e^{j\omega T/2}}{e^{j\omega T/2} - e^{-j\omega T/2}}$$

$$= \frac{\left(\frac{C_1}{C_2}\right) e^{j\omega T/2}}{2j \sin\left(\frac{\omega T}{2}\right)} \cdot \left(\cdot \frac{\omega T}{\omega T} \right)$$

$$= \underbrace{\frac{1}{j\omega}}_{1/s} \cdot \underbrace{\left(\frac{C_1}{C_2 \cdot T}\right)}_{\omega_0 = f_s\left(\frac{C_1}{C_2}\right)} \underbrace{\frac{(\omega T/2)}{\sin(\omega T/2)}}_{\text{Magnitude Error}} \underbrace{e^{j\omega T/2}}_{\text{phase error}}$$

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$$\text{Half Delay Integrator} = \frac{\left(\frac{C_1}{C_2}\right) z^{-1/2}}{1 - z^{-1}}$$

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Half-Delay Integrator — Lossless Discrete Integrator

Quality $Q \to \infty$ [Since expression is imaginary) No real part.

Zero Delay $\frac{1}{1 - z^{-1}} = \frac{1}{1 - e^{-j\omega T}} = \frac{1}{(1 - \cos\omega T) + j \sin\omega T}$

Quality $Q = \frac{\text{Imag}}{\text{Real}} = \frac{\sin\omega T}{1 - \cos\omega T}$ (+ve) Q

One Delay $= \frac{z^{-1}}{1 - z^{-1}} = \frac{e^{-j\omega T}}{1 - e^{-j\omega T}} = \frac{1}{e^{j\omega T} - 1} = \frac{1}{(\cos\omega T - 1) + j \sin\omega T}$

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Reference Design Tech. for MOS SC ladder filters. G. M. Jacobs et.al. CAS Dec 1978

$$\text{Magnitude Error} = \frac{\left(\frac{\omega T}{2}\right)}{\sin\left(\frac{\omega T}{2}\right)}$$

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$f \rightarrow$ max freq of interest in ρ filter

$(f/f_s)^{-1}$	Mag Error
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Better than cap matching error of 0.1%

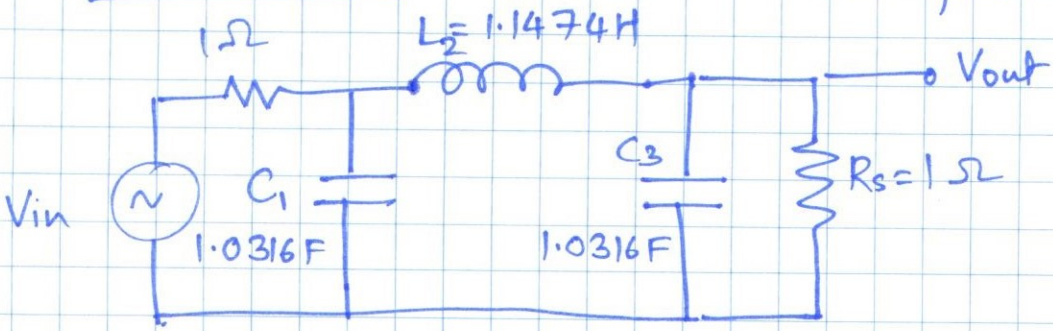
S.C. Filter Design Example.

Design a Chebyshev filter to meet following requirement

* 0.1dB ripple
* 10MHz ripple BW
* Stopband Atten. 40dB
* Stopband 60MHz

3rd order

RLC filter based on tables provided in lect 19



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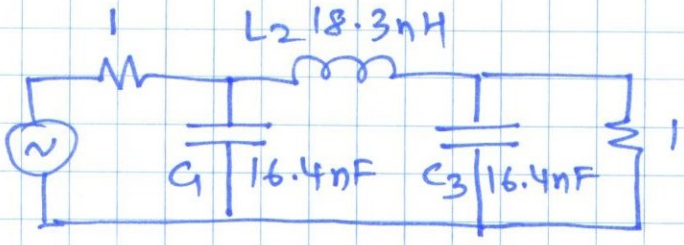

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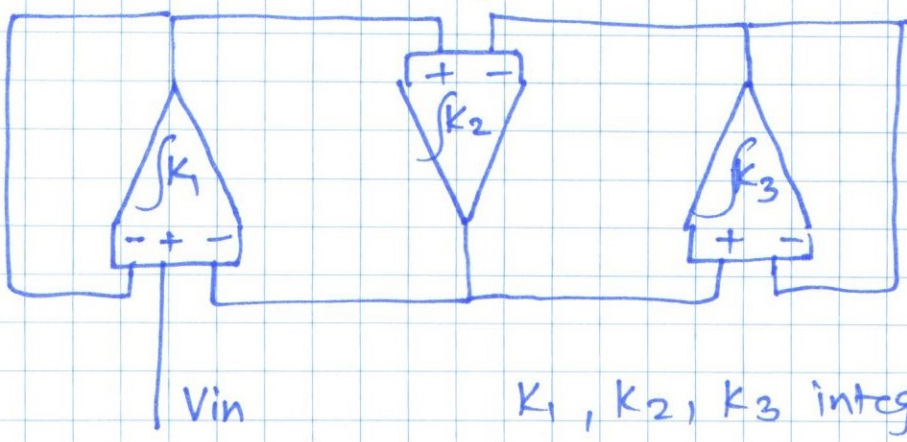


$K_1 = \frac{1}{C_1}$

$K_2 = \frac{1}{L_2}$

$K_3 = \frac{1}{C_3}$

K_1, K_2, K_3 integrator UGF

Connecting to switched-cap integrators

* 10MHz ripple BW → 200MHz = f_s (20x)

$$\boxed{\omega_0 = f_s \cdot \left(\frac{C_1}{C_2}\right)}$$

For integrator 1 & 3.

$$\omega_0 = f_s\left(\frac{C_1}{C_2}\right) = \frac{1}{16.4n}$$

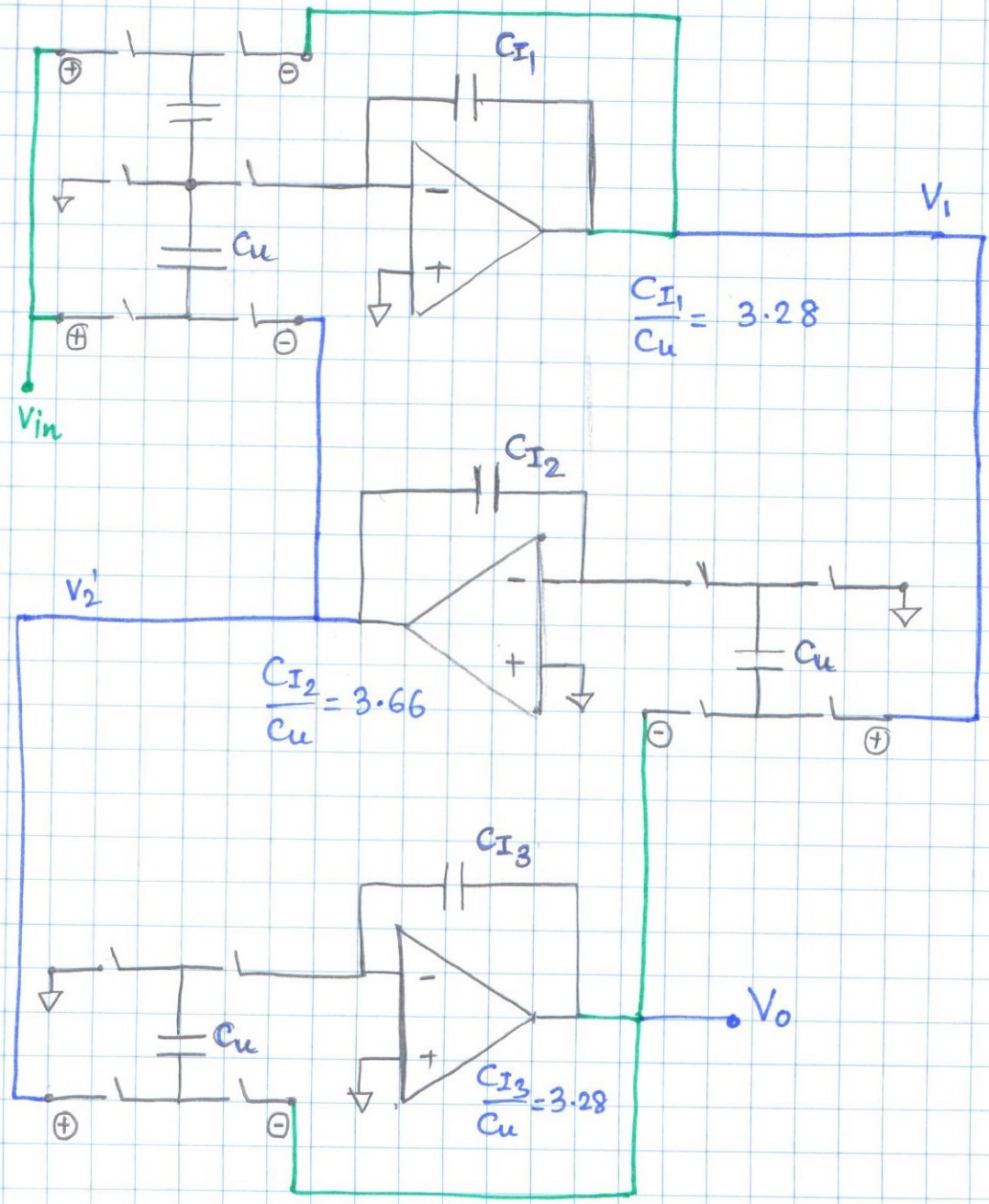
$$\frac{C_2}{C_1} = f_s \times 16.4n = 200 \times 10^6 \times 16.4 \times 10^{-9}$$

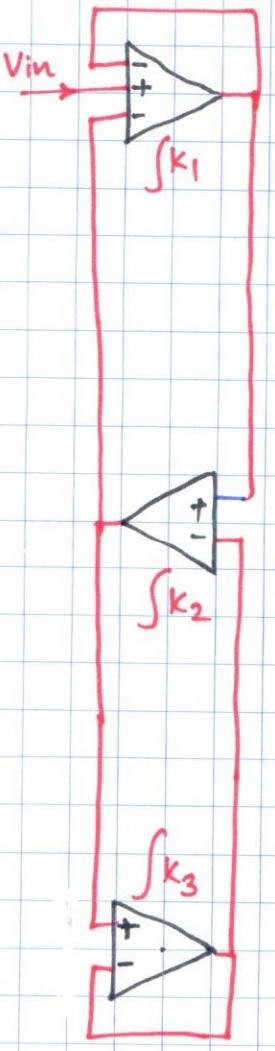
$$\boxed{= 3.28}$$

For integrator 2

$$\omega_0 = f_s\left(\frac{C_1}{C_2}\right) = \frac{1}{18.3n}$$

$$\boxed{\frac{C_2}{C_1} = 3.66}$$





clocking – To avoid phase errors (from integrator)
→ half delay from each integrator.
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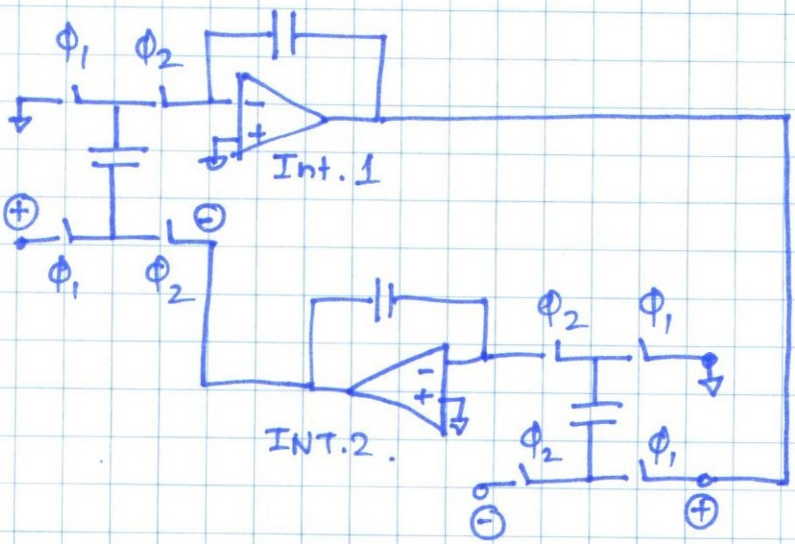
→ LDI (Lossless Discrete Integrator) clocking.

LDI Clocking — ① Same Phase Clocking



INT 1 – half delay

INT 2 – half delay.

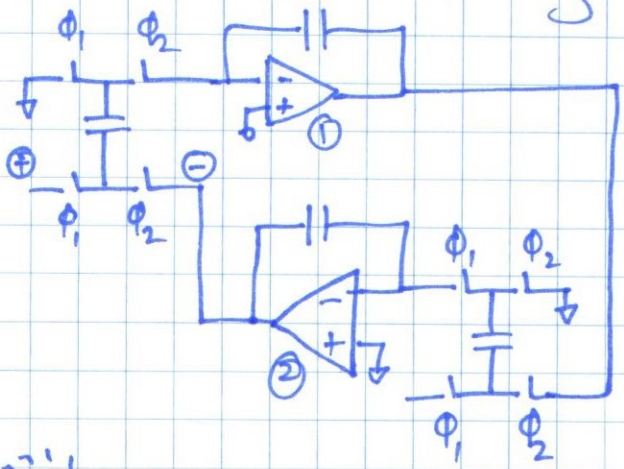
→ One clock period delay around the loop

→ LDI clocking

→ Opamp 1 & 2 both settle in ϕ_2
— idling in phase ϕ_1

→ Series setting of two opamps – BW shrinkage effect

② Alternate Phase Clocking



INT 1 → Zero delay

INT 2 → One delay

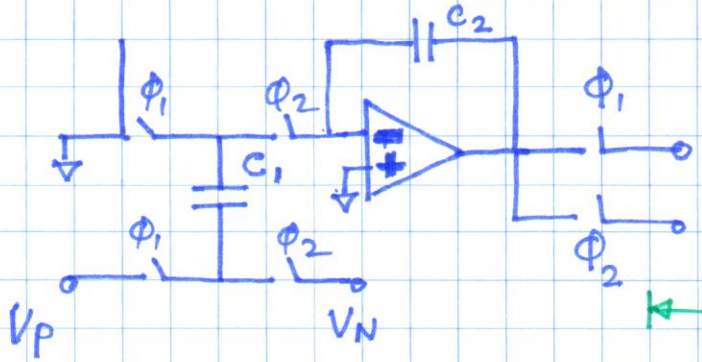
Total One delay around loop

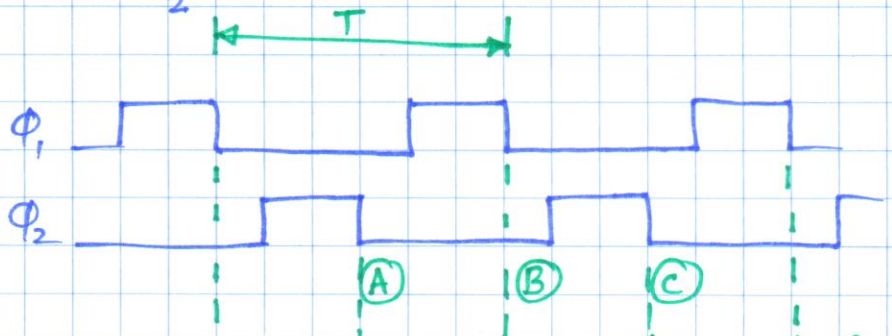
LDI Clocking

Opamp 1 settles during ϕ_2

opamp 2 settles during ϕ_1

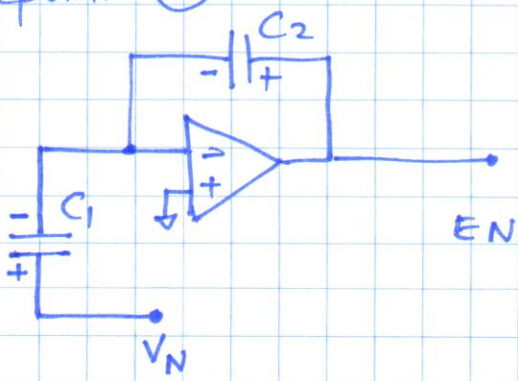
Parasitic Insensitive Switched-Capacitor Integrator





Lets figure out $V_{out_2}(t)$ first.

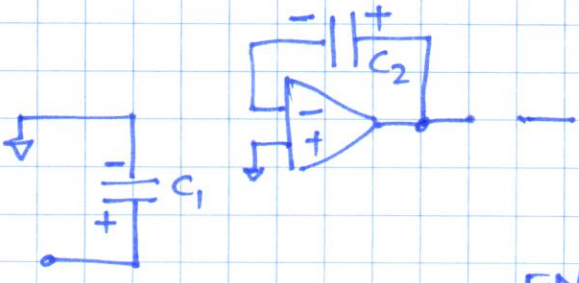
@ Timepoint (A)



END OF Φ_2

$$Q_{C_1-} = -C_1 V_N(t-T)$$
$$Q_{C_2-} = -C_2 V_{out_2}(t-T)$$

@ Timepoint (B)



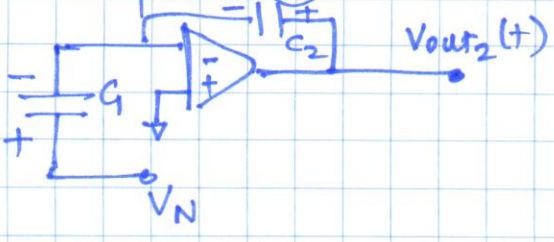
END OF Φ_1

$$Q_{C_1-} = -C_1 V_P(t-\tfrac{T}{2})$$
$$Q_{C_2-} = -C_2 V_{out_2}(t-T)$$

END OF Φ_2 - charge redistribution

$$Q_{C_1-} = -C_1 V_N(t)$$
$$Q_{C_2-} = -C_2 V_{out_2}(t)$$

@ Timepoint (C)



From (B) to (C) – charge conserved on capacitor plates connected to OPAMP. -ve i/p

$$\underbrace{Q_{C_1-} + Q_{C_2-}}_{(B)} = \underbrace{Q_{C_1-} + Q_{C_2-}}_{(C)}$$

$$-C_1 V_p\left(t-\tfrac{I}{2}\right) - C_2 V_{out_2}(t-T) = -C_1 V_N(t) - C_2 V_{out_2}(t)$$

Div by $-C_2$

$$\frac{C_1}{C_2} V_p\left(t-\tfrac{I}{2}\right) + V_{out_2}(t-T) = \frac{C_1}{C_2} V_N(t) + V_{out_2}(t)$$

Z - X form

$$\frac{C_1}{C_2} z^{-1/2} V_p(z) + z^{-1} V_{out_2}(z) = \frac{C_1}{C_2} V_N(z) + V_{out_2}(z)$$

$$V_{out_2}(z) = \underbrace{\frac{\left(\frac{C_1}{C_2}\right) z^{-1/2}}{1-z^{-1}} V_p(z)}_{\text{(Half Delay)}} - \underbrace{\frac{\left(\frac{C_1}{C_2}\right)}{1-z^{-1}} V_N(z)}_{\text{(Zero Delay)}}$$

$$V_{out_1}(z) = z^{-1/2} V_{out_2}(z)$$

$$V_{out_1}(z) = \underbrace{\frac{\left(\frac{C_1}{C_2}\right) z^{-1}}{1-z^{-1}} V_p(z)}_{\text{(Unit Delay)}} - \underbrace{\frac{\left(\frac{C_1}{C_2}\right) z^{-1/2}}{1-z^{-1}} V_N(z)}_{\text{(Half Delay)}}$$

$\left(\frac{C_1}{C_2}\right)$ → Integrator constant

$\frac{1}{1-z^{-1}}$ → Integrator function

{ Both (+ve) & (-ve) i/ps. achieved

Recap Integrator XF $H(s) = -\frac{1}{sCR} = -\frac{\omega_0}{s}$

$|H(j\omega)| = \omega_0/\omega \qquad \angle H(j\omega) = 90°$

Lets compare with discrete-time integrators.

$z = e^{j\omega T}$

Zero delay Integrator

$$\frac{\left(\frac{C_1}{C_2}\right)}{1 - z^{-1}} = \frac{\left(\frac{C_1}{C_2}\right)}{1 - e^{-j\omega T}} \left(\cdot \frac{e^{j\omega T/2}}{e^{j\omega T/2}} \right)$$

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$$= \frac{\left(\frac{C_1}{C_2}\right) e^{j\omega T/2}}{2j \sin\left(\frac{\omega T}{2}\right)} \cdot \left(\cdot \frac{\omega T}{\omega T} \right)$$

$$= \underbrace{\frac{1}{j\omega}}_{1/s} \cdot \underbrace{\left(\frac{C_1}{C_2 \cdot T}\right)}_{\omega_0 = f_s\left(\frac{C_1}{C_2}\right)} \underbrace{\frac{(\omega T/2)}{\sin(\omega T/2)}}_{\text{Magnitude Error}} \underbrace{e^{j\omega T/2}}_{\text{phase error}}$$

Similarly

One Delay Integrator

$$= \frac{\left(\frac{C_1}{C_2}\right) z^{-1}}{1 - z^{-1}}$$

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$$\text{Half Delay Integrator} = \frac{\left(\frac{C_1}{C_2}\right) z^{-1/2}}{1 - z^{-1}}$$

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Half-Delay Integrator — Lossless Discrete Integrator

Quality $Q \to \infty$ [Since expression is imaginary) No real part.

Zero Delay $\frac{1}{1 - z^{-1}} = \frac{1}{1 - e^{-j\omega T}} = \frac{1}{(1 - \cos\omega T) + j \sin\omega T}$

Quality $Q = \frac{\text{Imag}}{\text{Real}} = \frac{\sin\omega T}{1 - \cos\omega T}$ (+ve) Q

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$$\text{Magnitude Error} = \frac{\left(\frac{\omega T}{2}\right)}{\sin\left(\frac{\omega T}{2}\right)}$$

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Design a Chebyshev filter to meet following requirement

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* 10MHz ripple BW
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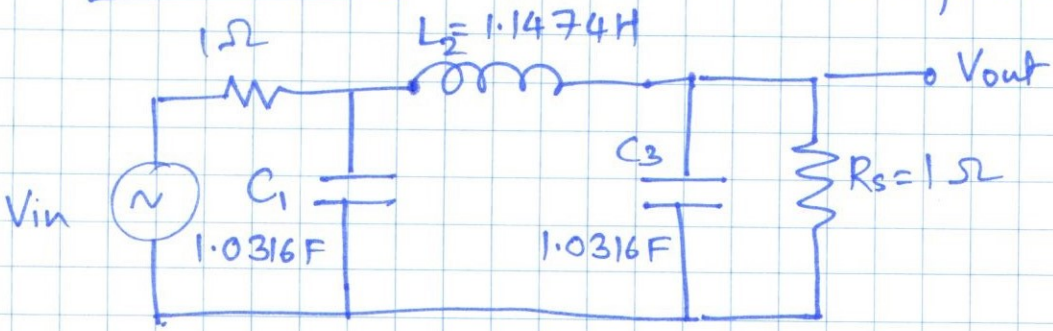
RLC filter based on tables provided in lect 19



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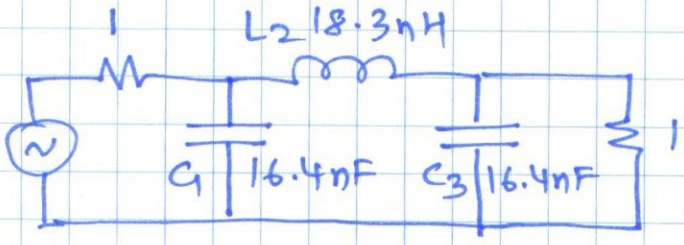

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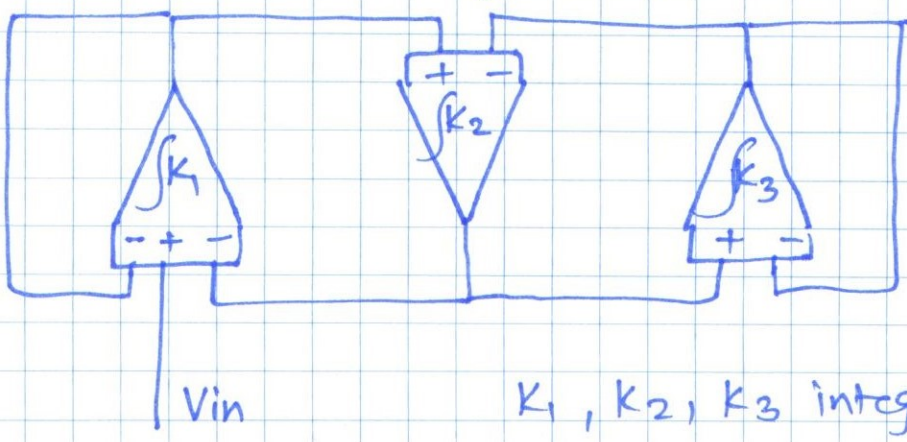

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K_1, K_2, K_3 integrator UGF

Connecting to switched-cap integrators

* 10MHz ripple BW → 200MHz = f_s (20x)

$$\boxed{\omega_0 = f_s \cdot \left(\frac{C_1}{C_2}\right)}$$

For integrator 1 & 3.

$$\omega_0 = f_s\left(\frac{C_1}{C_2}\right) = \frac{1}{16.4n}$$

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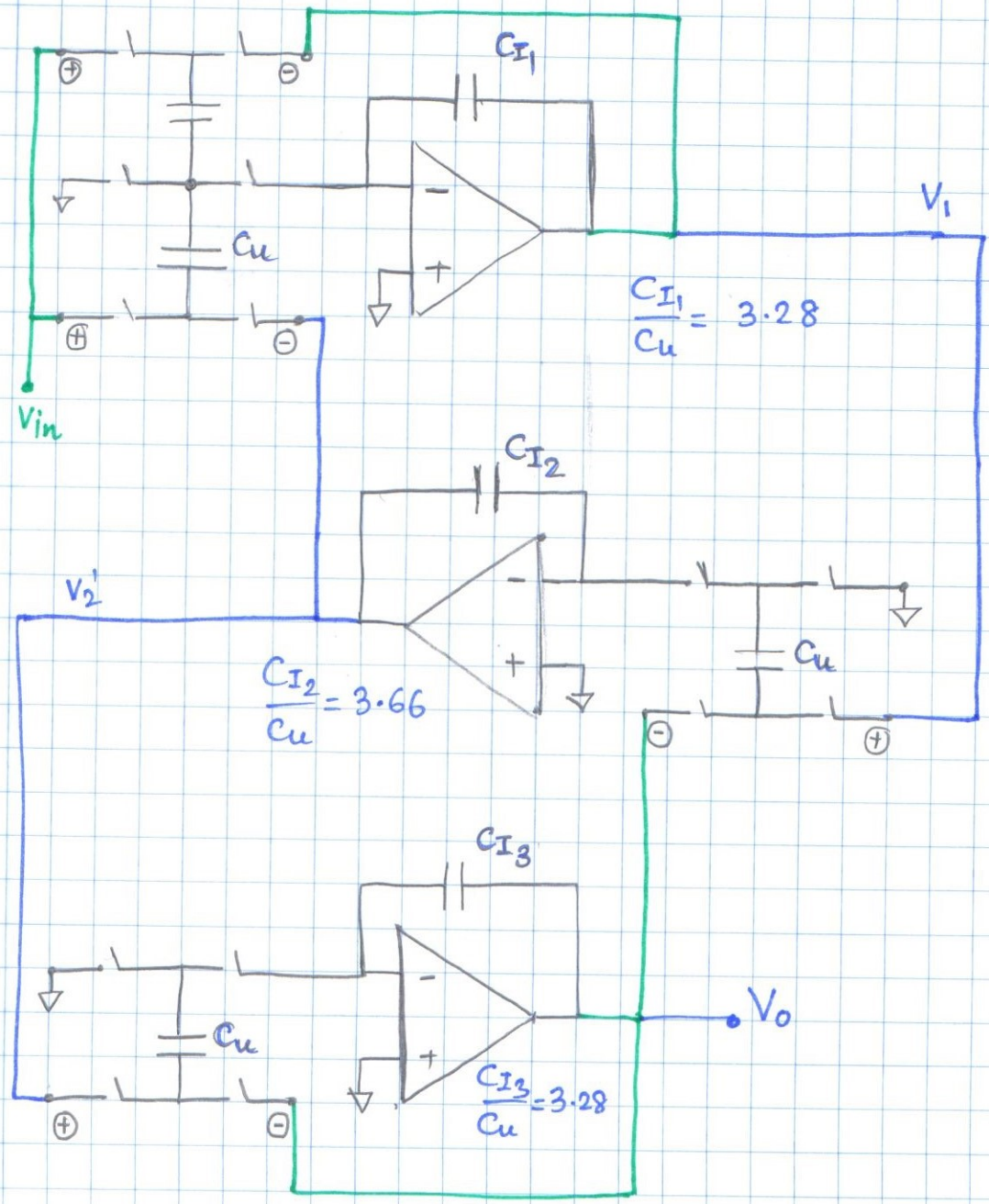

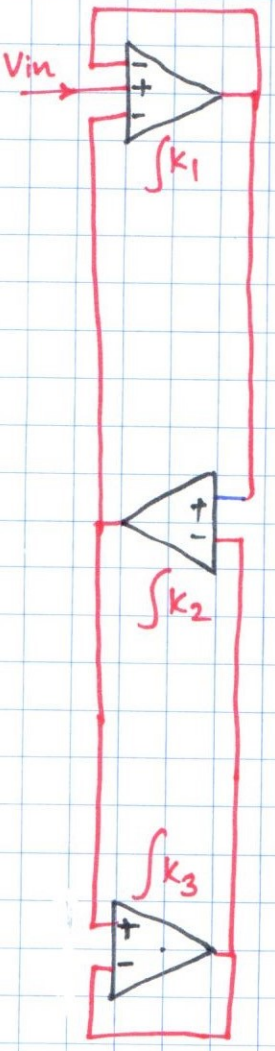

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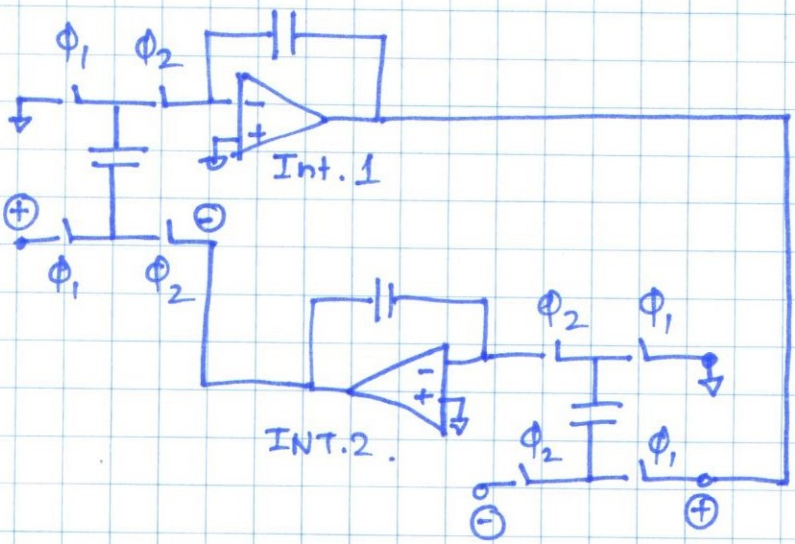
LDI Clocking — ① Same Phase Clocking



INT 1 – half delay

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→ One clock period delay around the loop

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→ Opamp 1 & 2 both settle in ϕ_2
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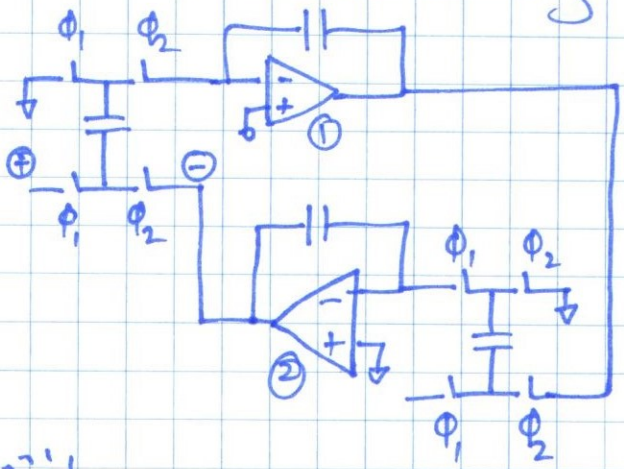
② Alternate Phase Clocking



INT 1 → Zero delay

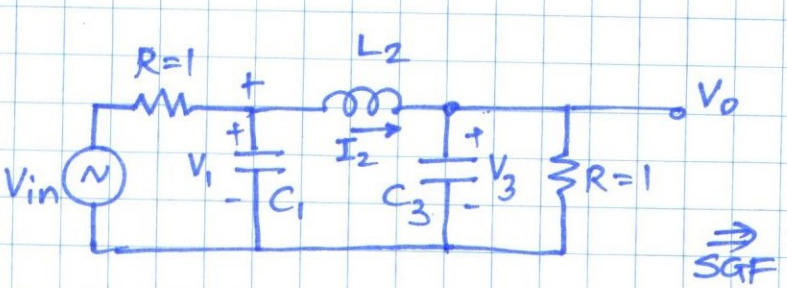
INT 2 → One delay

Total One delay around loop

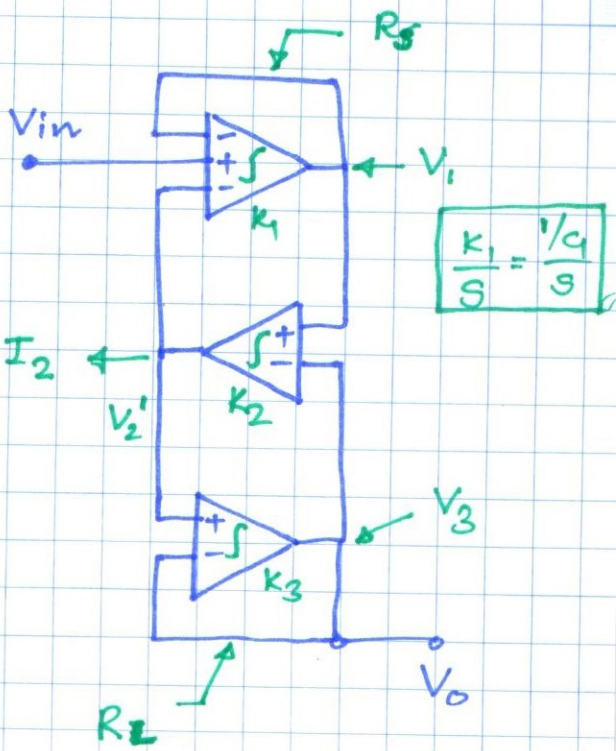
LDI Clocking

Opamp 1 settles during ϕ_2

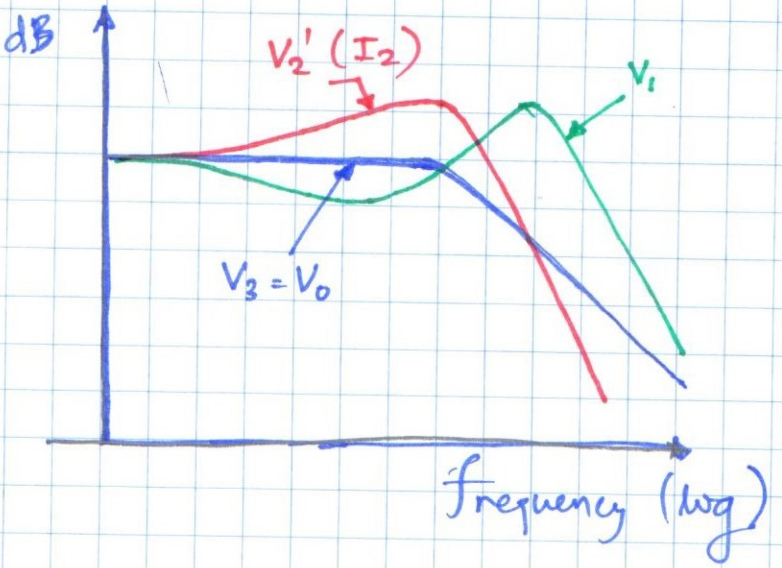
opamp 2 settles during ϕ_1



SGF



$\frac{k_1}{s} = \frac{1/c}{s}$



Observing voltages internally, V_1 & V_2' are about 3.2 dB higher than V_o. (Based on SPICE simulations)

→ Optimal voltage swing @ each integrator output — Depends on V_{DD}.

→ Since V_1 & V_2' are 3.2 dB higher [specific to our current example] max o/p voltage swing is reduced by 3.2 dB.

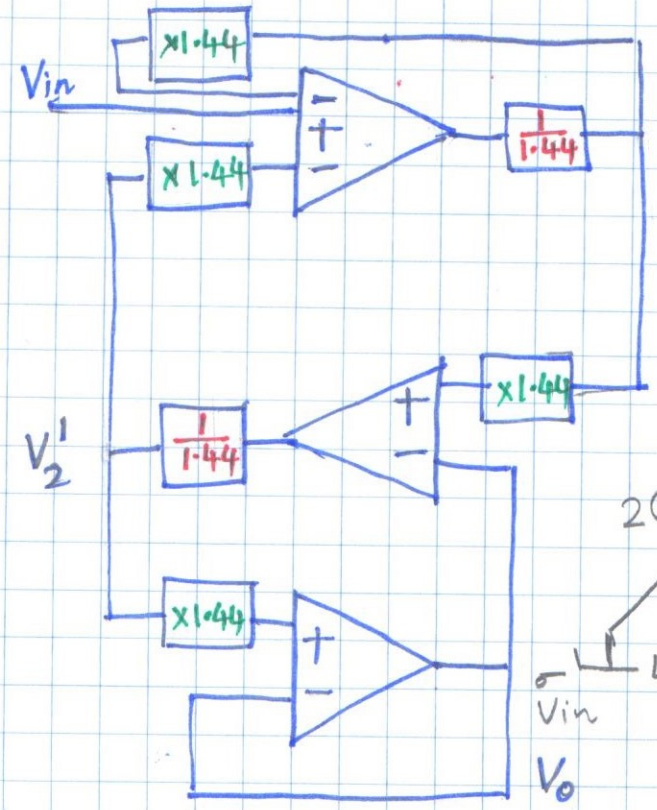
→ Else, Distortion will result.

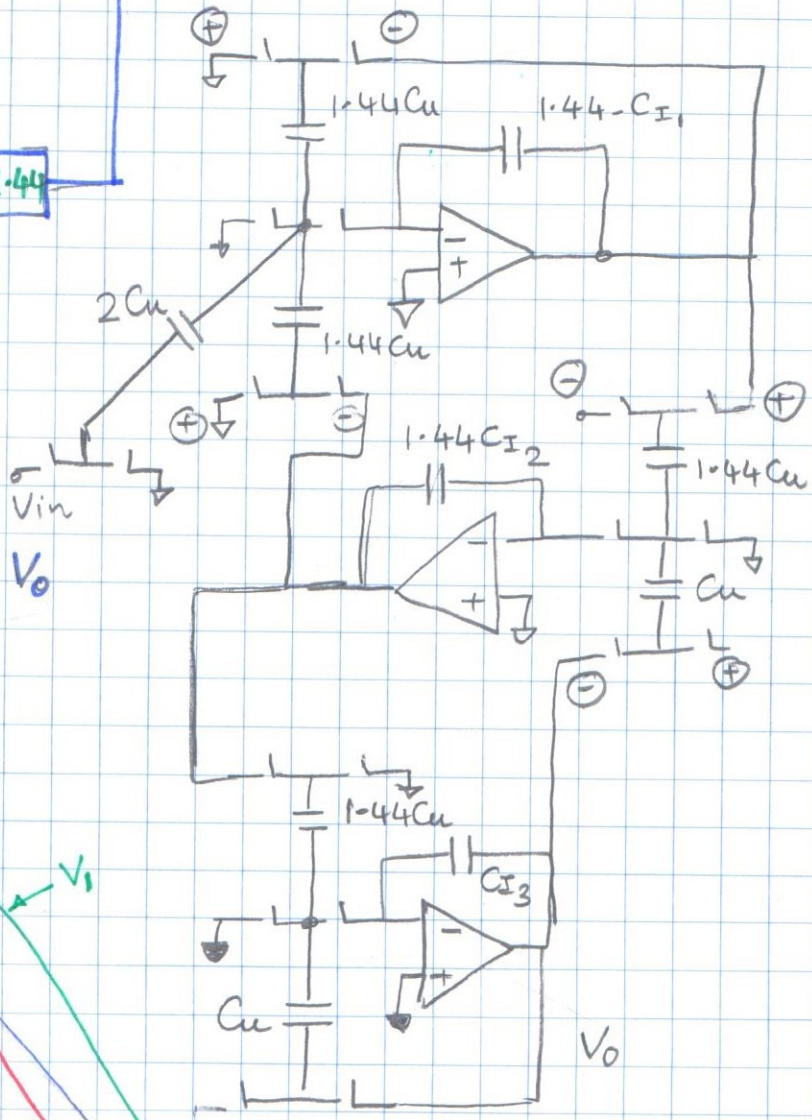
→ Need to do voltage swing equalization at each integrator o/p. { same peak amplitude for each stage

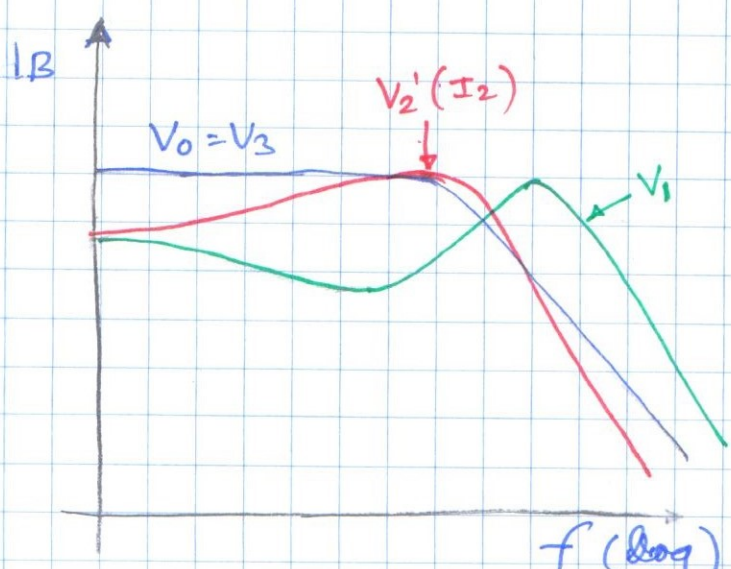
→ Also called Dynamic Range Scaling.

→ Applicable to continuous-time filters also.

- Need to attenuate V_1 & V_2' by 3.2 dB ($\frac{1}{1.44}$) WITHOUT changing overall xfer function.
- How ?





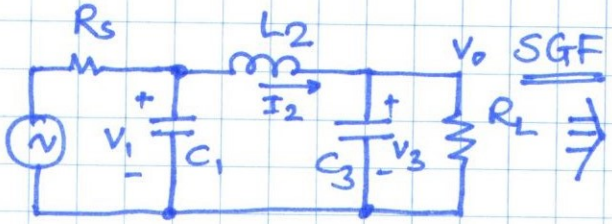


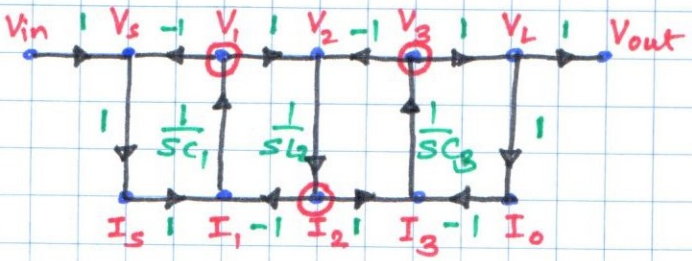
→ peak swings of all integrators equalized.

Another way to explain Voltage Swing Equalization

Start with RLC filter

Refer: L-20 page 6





→ Simulate RLC circuit using SPICE → Determine peak gain for each variable representing INTEGRATOR OUTPUT.

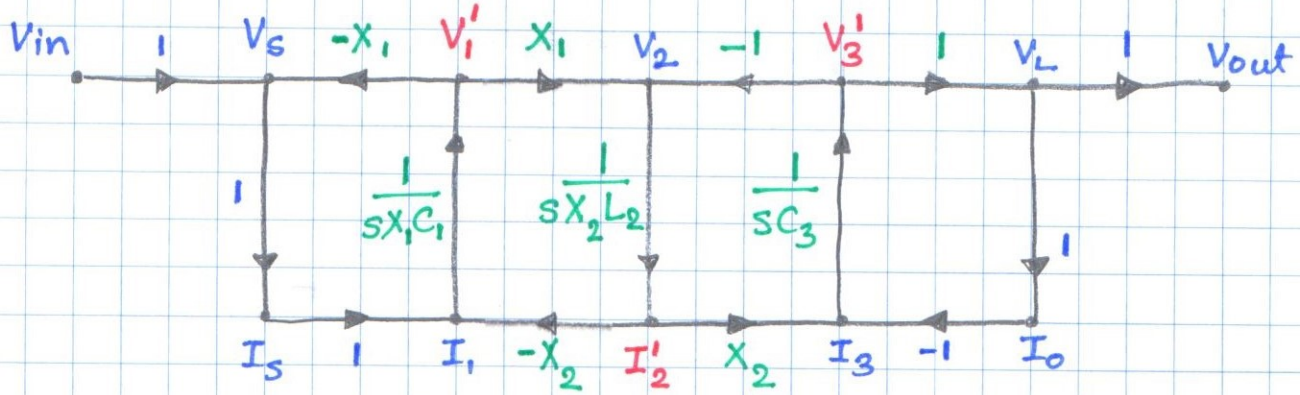
For example: In this case V_1, I_2 & V_3 → (Same as V_o)

$$\frac{V_1}{V_{out}} = X_1 \quad ; \quad \frac{I_2}{V_{out}} = X_2 \quad ; \quad \frac{V_3}{V_{out}} = 1$$

X_1 & X_2 > 1 → Need to scale Integrator 1, 2 so that peak gain for all integrator o/ps is same.

(Represent Peak values)

Modified SGF implementation

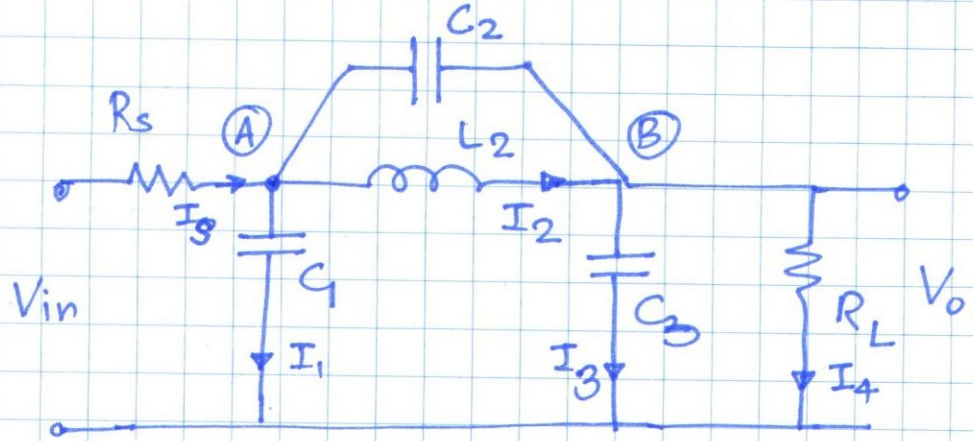


$$V_1' = \frac{V_1}{X_1} \quad ; \quad I_2' = \frac{I_2}{X_2}$$

Now all integrator o/ps will have same peak values (may be at different frequencies) → Optimum dynamic range.

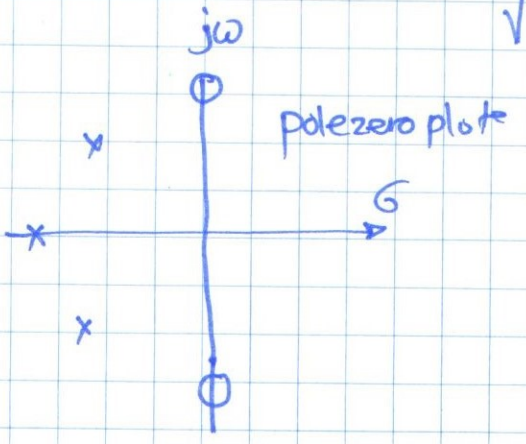
Implementing finite transmission zeros

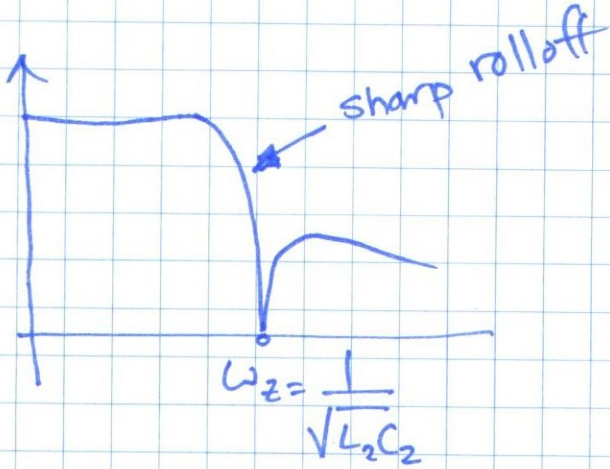
Ref: Allstot "MOS SC Ladder Filters" JSSC- Dec 1978.



Tx zero @ resonance of $L_2 C_2$

$$\omega_{zero} = \frac{1}{\sqrt{L_2 C_2}}$$





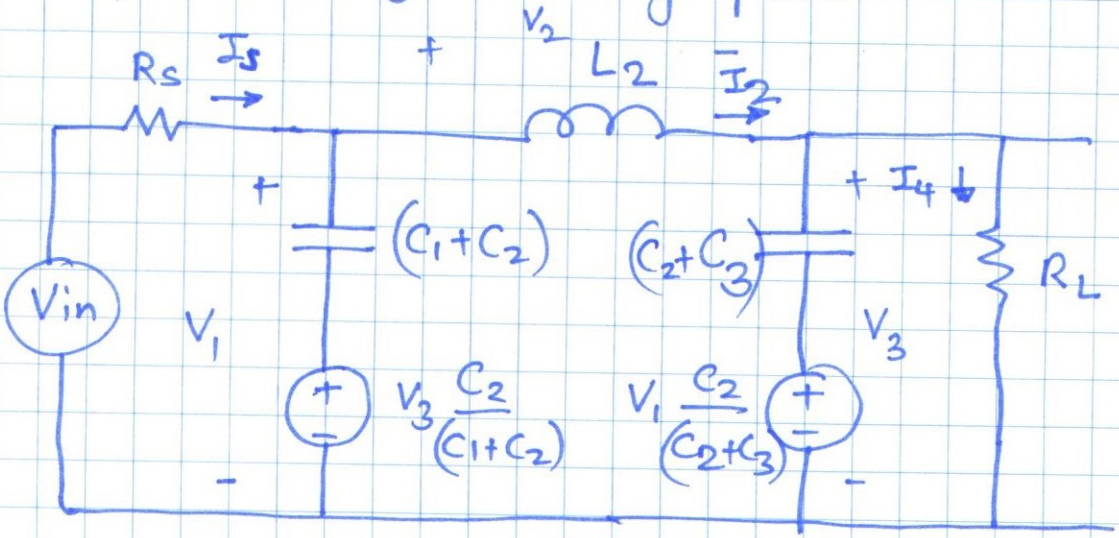
KCL @ (A) $\quad I_g = sC_1V_1 + sC_2(V_1 - V_3) + I_2$

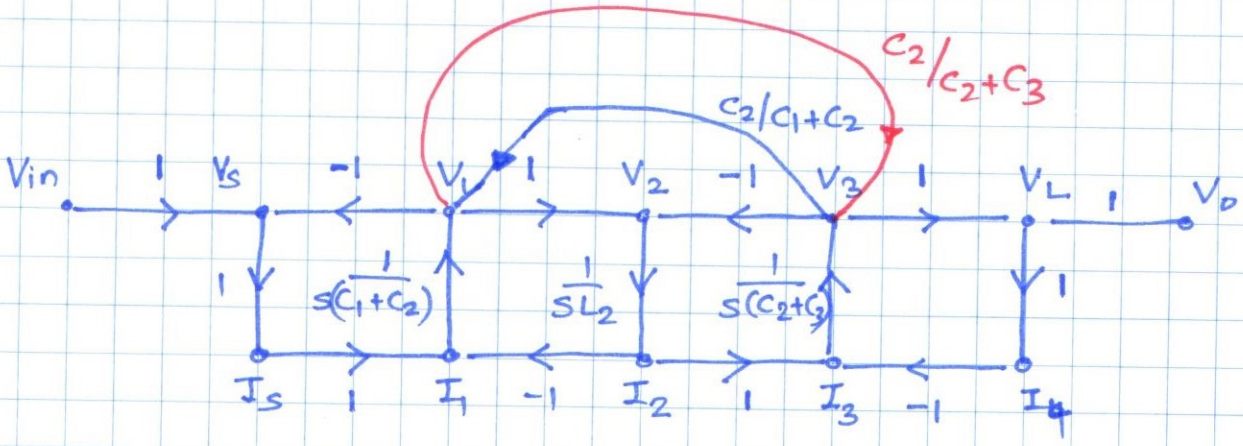
$$V_1 = \underbrace{\frac{I_g - I_2}{s(C_1+C_2)}}_{\text{Integration}} + \underbrace{V_3 \frac{C_2}{(C_1+C_2)}}_{\text{Addition}}$$

KCL @ (B) $\quad I_2 = I_4 + sC_3V_3 + sC_2(V_3 - V_1)$

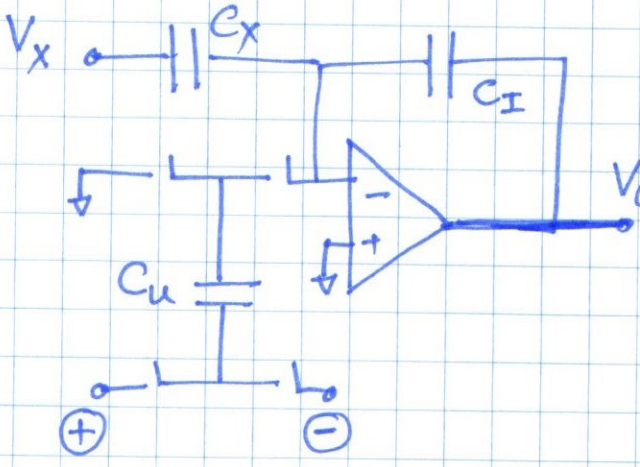
$$V_3 = \frac{I_2 - I_4}{s(C_2+C_3)} + V_1 \frac{C_2}{C_2+C_3}$$

Update Signal flow graph.





How to implement scaled addition in SC?

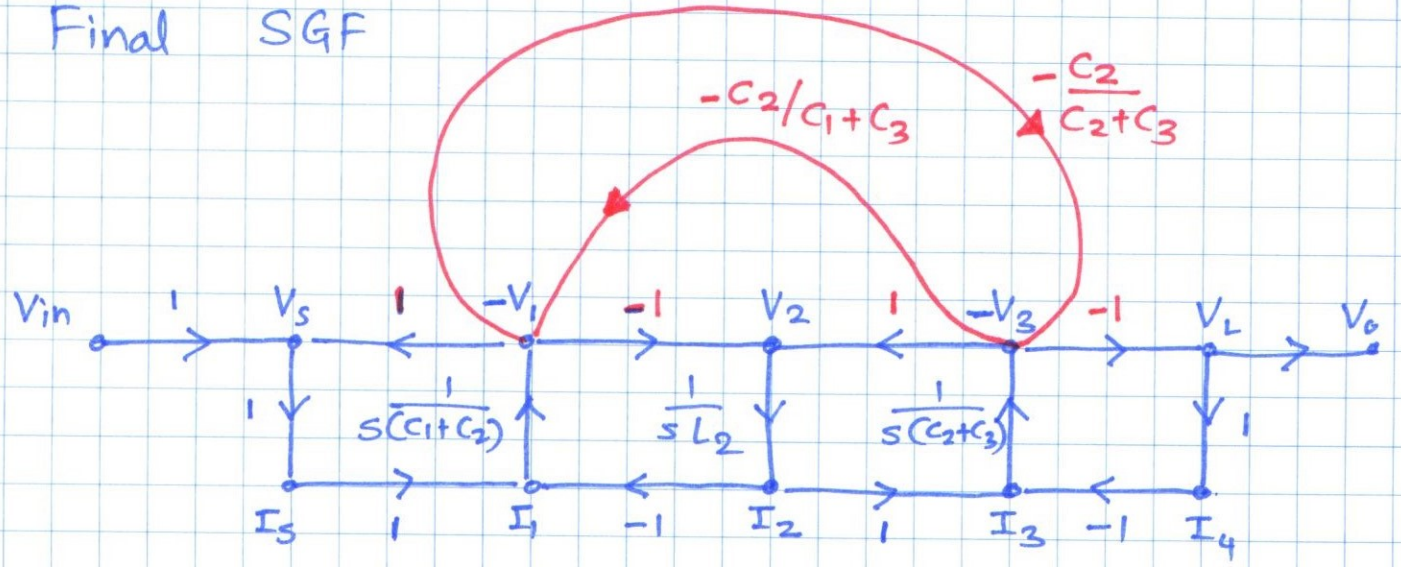


$V_{out} = -\left(\frac{C_x}{C_I}\right)V_x$ + integrator parts.

↑ inverting sign.

→ Modify SGF – Replace V_1 by $(-V_1)$ & Replace V_3 by $(-V_3)$

Final SGF

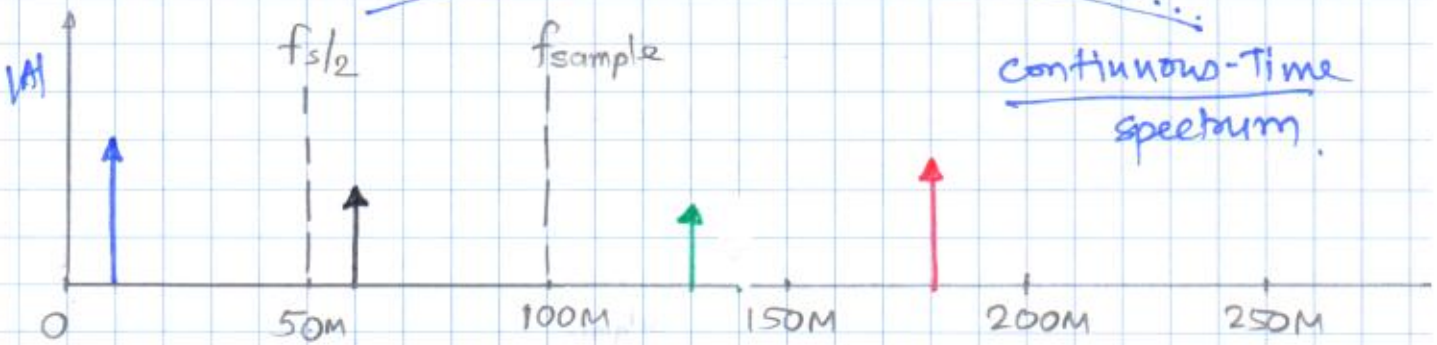


Now this can be implemented using SC integrators & scaled addition units.

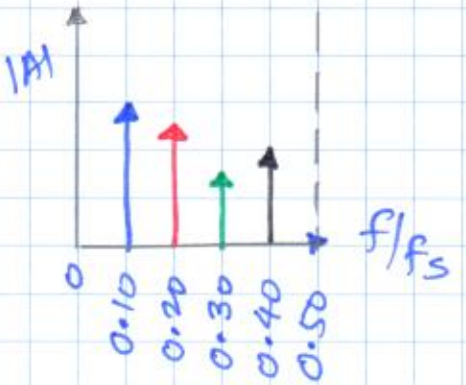
→ HOME EXERCISE -

→ Identical Technique can be applied to Continuous-Time filters for implementing zeros (Eg. Elliptic filters)

ANTIALIASING FILTER



continuous-Time spectrum.



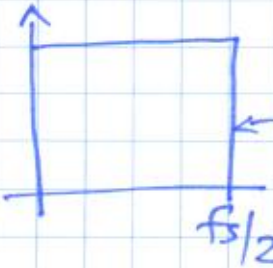
Signals higher than $\frac{fs}{2}$ fold back into the desired band

— Aliasing.

— Corrupt desired signal forever.

- Nyquist sampling Thm : Signal should be bandlimited to $fs/2$.

→ Need to filter out everything above $fs/2$
→ AAF

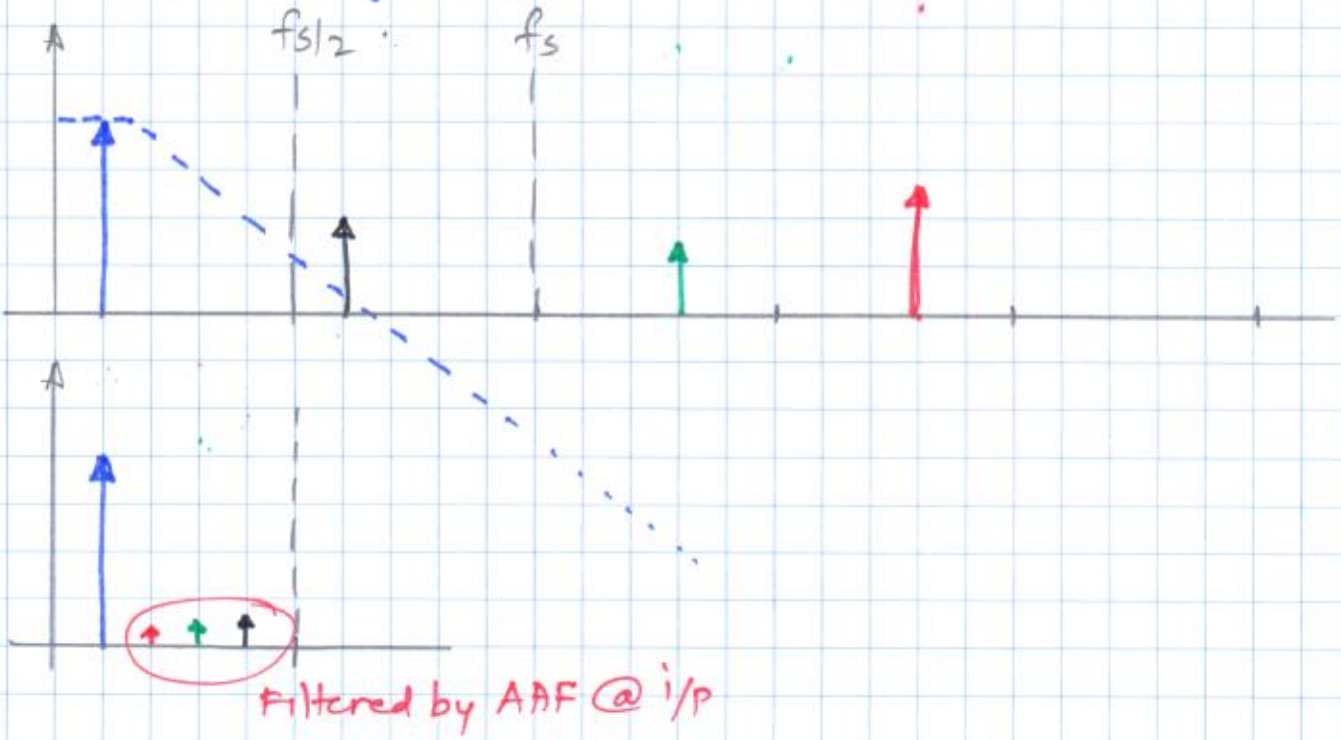


← Done with continuous time. filter.

Brickwall filters very difficult in cont-time.

→ Increase sampling rate - oversample

→ Ease requirement on AAF.

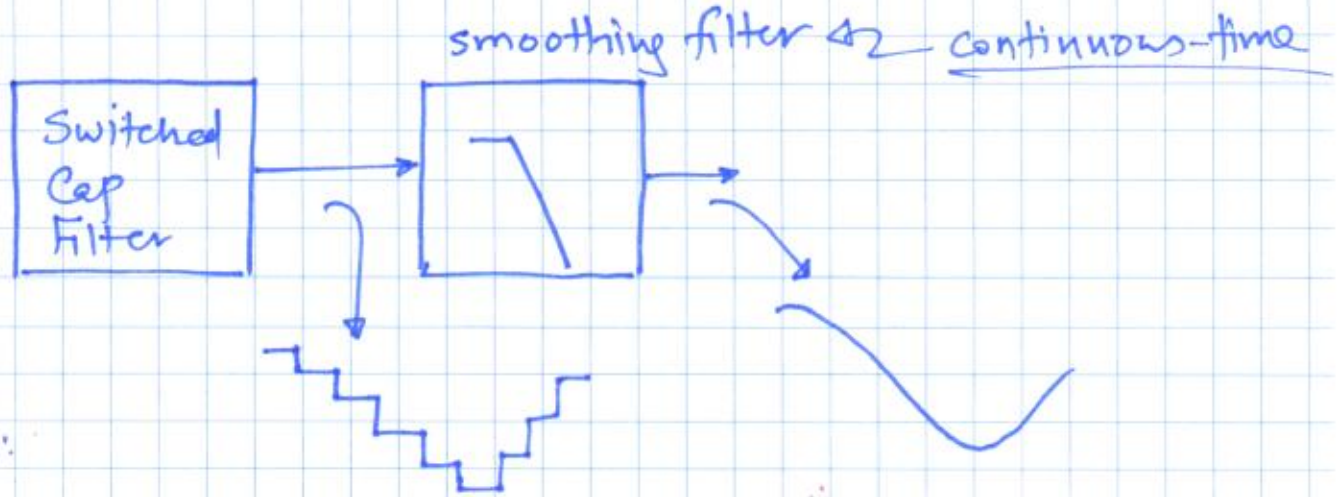


General AAF design guidelines

→ low order design - of course continuous-time filter

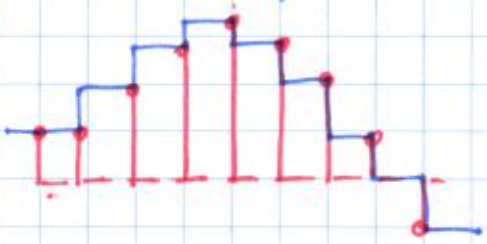
→ Make sure AAF attenuates undesired signals sufficiently with largest PVT variation

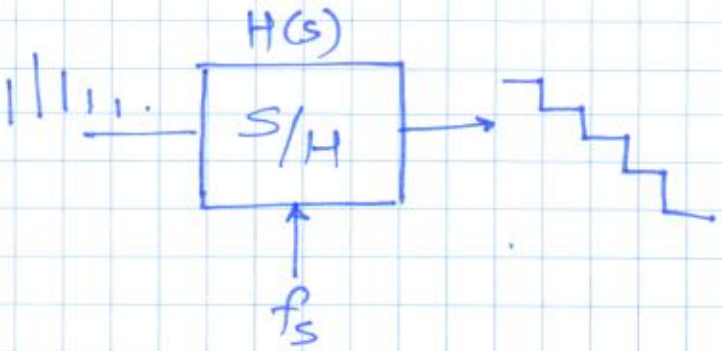
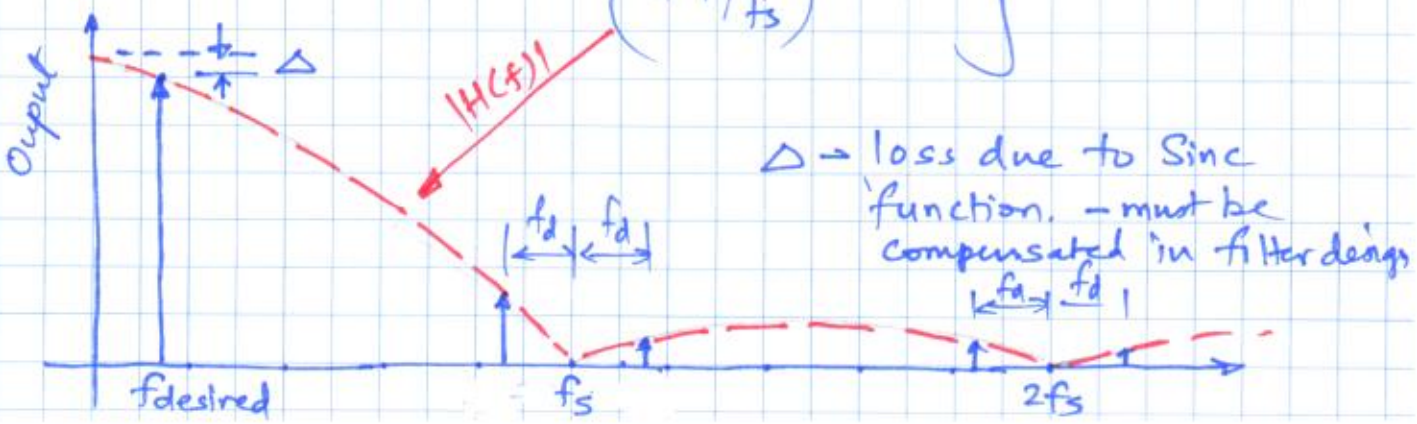
→ No frequency tuning



Smoothing filter – Removes clock & high frequency artifacts.

Switched cap filter o/p – Sampled & held o/p





$$|H(f)| = \frac{\sin(\pi f/f_s)}{(\pi f/f_s)}$$ } Sinc function